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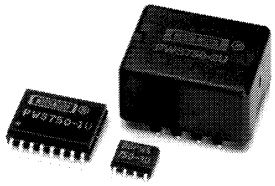


PWS750

Isolated, Unregulated DC/DC CONVERTER COMPONENTS

FEATURES

- 100% TESTED FOR HIGH-VOLTAGE BREAKDOWN
- COMPACT-SURFACE MOUNT
- MULTICHANNEL OPERATION
- 5V OR 15V INPUT OPTIONS
- FLEXIBLE USE WITH PWS740/PWS745 COMPONENTS

APPLICATIONS

- INDUSTRIAL PROCESS CONTROL EQUIPMENT
- GROUND-LOOP ELIMINATION
- PC-BASED DATA ACQUISITION
- VENDING MACHINES

DESCRIPTION

The PWS750 consists of three building blocks for building a low cost DC/DC converter. With them you can optimize DC/DC converter PC board layout or build a multichannel isolated DC/DC converter. All parts are surface mount, requiring minimal space to build the converter. The modular design minimizes the cost of isolated power.

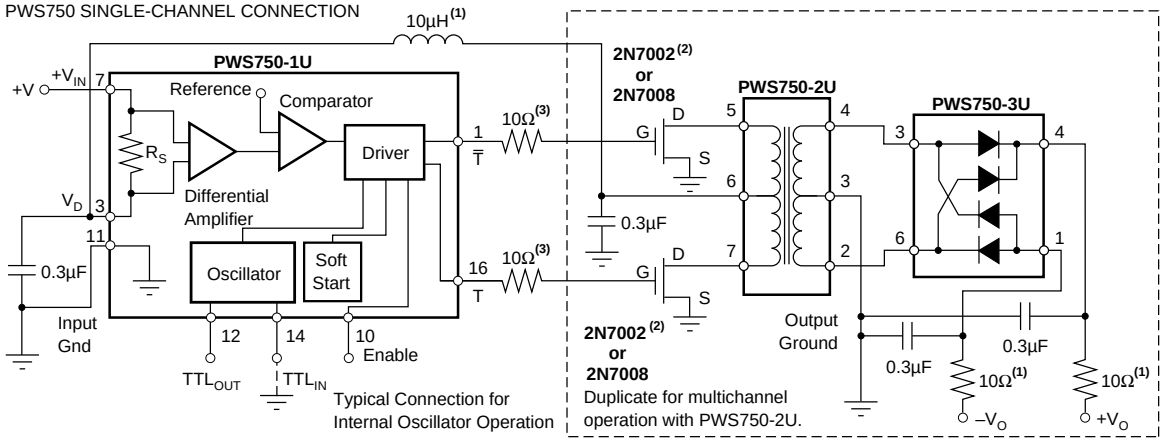
The PWS750-1U is a high-frequency (800kHz nominal) driver that can drive N-channel MOSFETs up to the size of a 1.3A 2N7010. The recommended MOSFET for individual transformer drivers is the 2N7008. The PWS750-1U is supplied in a 16-pin double-wide SO package.

The PWS750-2U and PWS750-4U are split-bobbin wound isolation transformers using a ferrite core. They are encapsulated in plastic packages, allowing a high isolation voltage rating.

The PWS750-3U is a high-speed monolithic diode bridge in a plastic 8-pin SO package.

One PWS750-1U can be used to drive up to four channels (15V nominal operation). One PWS750-2U and PWS750-3U and two 2N7002 (surface mount) or 2N7008 (TO-92) MOSFETs made by Siliconix are used per isolated channel. When a PWS750-4U is used as the transformer (5V input), then two TN0604s made by Supertex must be used, due to the higher currents of the primary (lower RDS on) and the lower V_{GS} threshold. With 5V operation only one channel can be directly driven by the PWS750-1U (a simple FET booster circuit can be used for multichannel operation; see Figure 3).

PWS750 SINGLE-CHANNEL CONNECTION



NOTES: (1) User option. (2) Use TN0604 for 5V to ±15V operation. (3) Multichannel Operation.

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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

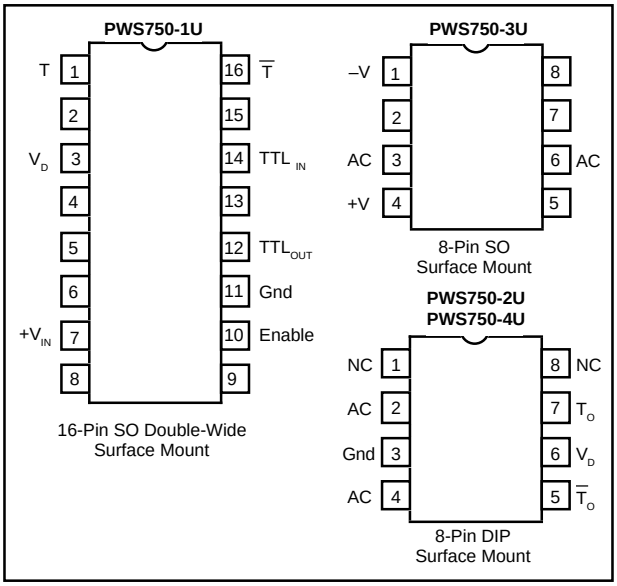
ELECTRICAL

At T_A = 25°C; $+V_{IN}$ = +15V; and I_{OUT} = ±15mA balanced loads, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PWS750-1U OSCILLATOR					
Frequency: Internal OSC	TTL_{IN} = 0V	725	800	875	kHz
External OSC		1		2.5	MHz
Supply: 15V Operation		10	15	18	V
5V Operation		4.5	5	5.5	V
T, $\overline{T}$ Drive Current				50	mApk
T, $\overline{T}$ Drive Voltage, High		3		7	V
Low				0.7	V
TTL_{IN}, I_{IH}			10		nA
I_{IL}			–1		µA
V_{IH}		2			V
V_{IL}				0.8	V
TTL_{OUT}, I_{OL}				15	mA
PWS750-2U +V_{IN} TO ±V_{OUT} ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz		750			Vrms
100% Test (1)	60Hz, 1s, <5pC PD	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1	1.5	µArms
Winding Ratio	Primary/Secondary		48/48		
PWS750-3U DIODE BRIDGE					
Reverse Recovery	$I_F = I_R$ = 50mA		40		ns
Reverse Breakdown	I_R = 100µA	55			V
Reverse Current	V_R = 40V			1.5	µA
Forward Voltage	I_F = 100mA			1.8	V
PWS750-4U +5V_{IN} to ±15V_{OUT} ISOLATION TRANSFORMER					
ISOLATION					
Voltage Rated Continuous AC 60Hz		750			Vrms
100% Test (1)	60Hz, 1s, <5pC PD	1200			Vrms
Barrier Impedance			10^{12} || 8		Ω || pF
Leakage Current at 60Hz	V_{ISO} = 240Vrms		1	1.5	µArms
Winding Ratio	Primary/Secondary		24/70		
TEMPERATURE RANGE					
Specification		0		+70	°C
Operating	Derated performance	–40		+85	°C
Storage		–40		+85	°C

NOTES: (1) Tested at 1.6 x rated, fail on 5pC partial discharge leakage current on five successive pulses at 60Hz.

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	18V
Junction Temperature	150°C
Storage Temperature	–40°C to +85°C
Lead temperature (soldering, SOIC, 3s)	+260°C
Max Load, Sum of Both Outputs (PWS750-2U, 4U)	60mA

ORDERING INFORMATION

PWS750-XU

Basic Model Number

Components

1U : High-Frequency Driver
2U, 4U : Isolation Transformer
3U : High-Speed Monolithic Diode Bridge

PACKAGE INFORMATION

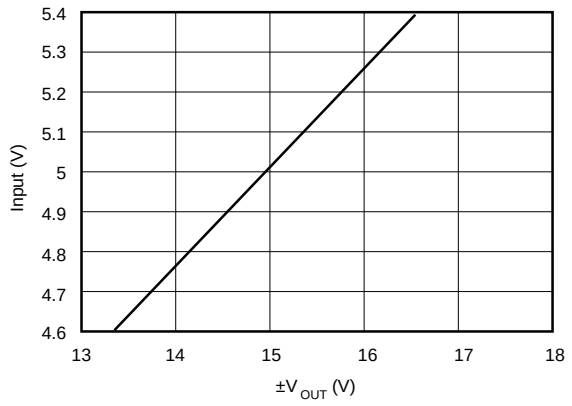
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PWS750-1U	16-Pin SOIC	211
PWS750-2U	8-Pin Plastic	226
PWS750-3U	8-Pin SO	182
PWS750-4U	8-Pin Plastic	226

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

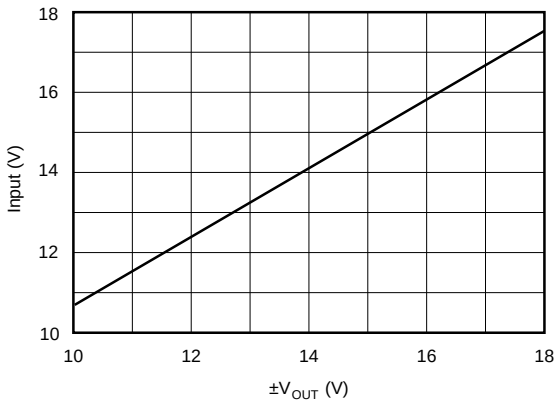
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_{IN} = 15VDC, I_{LOAD} = ±15mA unless otherwise noted.

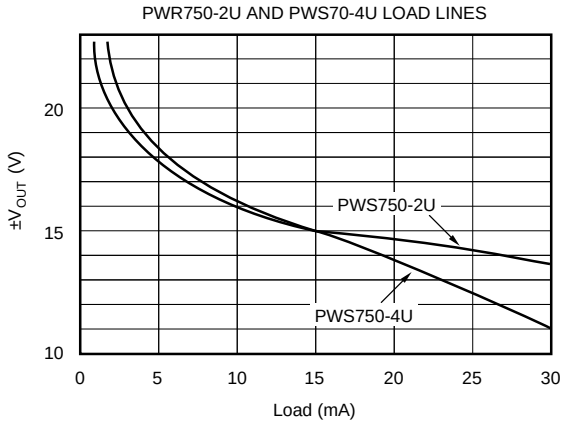
PWS750-4U LINE REGULATION



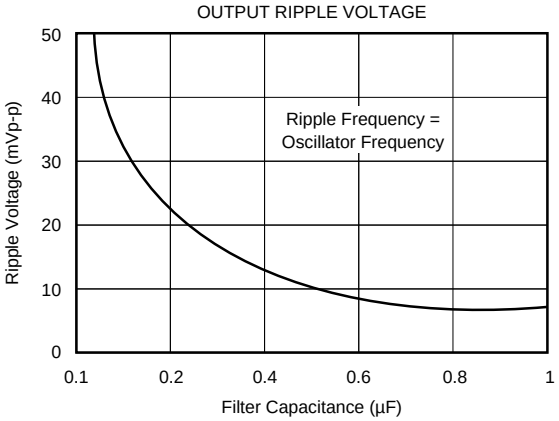
PWR750-2U LINE REGULATION



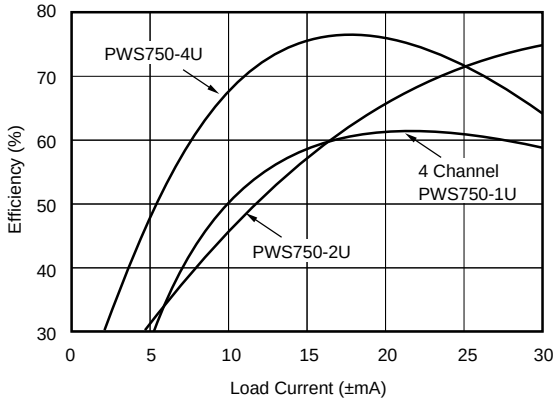
PWR750-2U AND PWS70-4U LOAD LINES



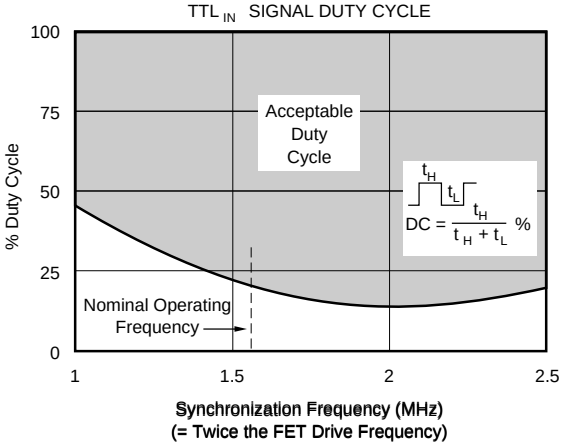
OUTPUT RIPPLE VOLTAGE



EFFICIENCY/LOAD CURVE



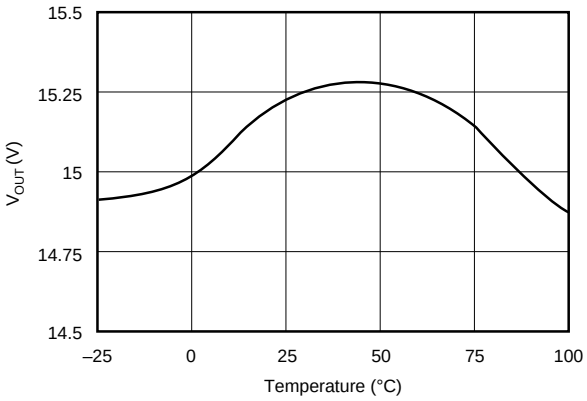
TTL IN SIGNAL DUTY CYCLE



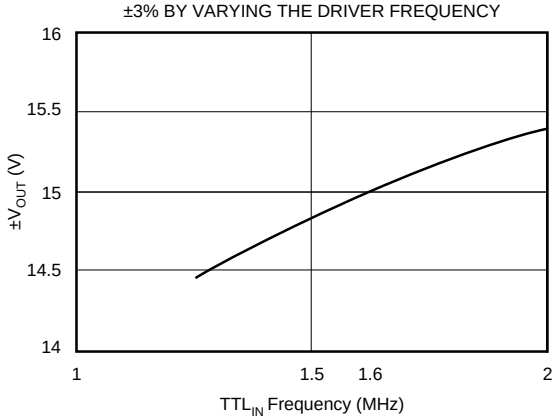
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{IN} = 15VDC, I_{LOAD} = ±15mA unless otherwise noted.

OUTPUT VOLTAGE DRIFT WITH A ±15mA LOAD



THE OUTPUT VOLTAGE CAN BE ADJUSTED ±3% BY VARYING THE DRIVER FREQUENCY



THEORY OF OPERATION

The PWS750 components are basic building blocks to be used with other standard components to build an isolated push-pull DC/DC converter. The oscillator runs at 800kHz nominal, making it possible to reduce the size of the transformer and lower the output ripple voltage.

PWS750-1U OSCILLATOR PIN FUNCTIONS

TTL_{IN} is used to control the driver frequency with an external TTL level frequency source. The input frequency must be twice the desired driver frequency, since there is an internal divide-by-2 circuit to produce a 50% duty cycle output. The input duty cycle can vary from 12% to 95% (see Typical Performance Curves). When in the free running mode, the TTL_{IN} pin must be tied to ground.

TTL_{OUT} is used when it is desired to synchronize the outputs of multiple PWS750-1Us to minimize beat frequency problems. A standard open collector output is provided, therefore a 330Ω to 3.3kΩ pull-up resistor will be necessary depending on stray capacitance on the sync line. A maximum of eight PWS750-1Us can be connected without the use of an external TTL buffer.

An Enable pin is provided so that the driver (T, $\overline{T}$) can be shut down to minimize power use if required. A TTL low applied to the pin will shut down the driver within one cycle. A TTL high will enable the driver within one cycle. The TTL_{OUT} will still have an 800kHz signal when a master driver is disabled, so other synchronized drivers will not be shut down. The pin can be left open for normal operation.

The $+V_{IN}$ pin supplies power to the oscillator. The V_D pin connects the power to the transformer through the internal overcurrent sense resistor. The other end of the overcurrent sense resistor is tied to $+V_{IN}$. A 0.3µF bypass capacitor must be connected to the V_D pin to reduce the ripple current through the shunt resistor; otherwise false current limit conditions can occur due to ripple voltage peaks.

During overload conditions the output drive shuts off for approximately 80µs, then turns back on for 20µs, resulting in a 25% power up duty cycle. If the overload condition still exists, then the output will shut off again. When the fault or the excessive load is removed, the converter resumes normal operation.

The T and $\overline{T}$ pins are the complementary FET drive outputs and are tied directly to the corresponding FET gate. The connection must be as short as possible. For multiple channel operation they cannot be located above any ground or power planes, because capacitive loading will not allow fast enough charging of the FET gate.

PWS750-2U AND PWS750-4U TRANSFORMER PIN FUNCTIONS

On the primary side the V_D pin of the PWS750-2U is tied directly to the V_D pin of the PWS750-1U. Remember to place a 0.1µF capacitor as close to the PWS750-2U V_D pin as possible. The T_O and $\overline{T}_O$ pins are connected to the drains of the corresponding FETs, whose sources are connected to ground. On the secondary side of the transformer, the Gnd pin is tied directly to the isolated ground. AC pins are 800kHz square wave signals at twice the output voltage, and are connected directly to the corresponding pin on the PWS750-3U. Pins 2 and 4 can be interchanged for ease of hook up. The connection to the diode bridge must be as direct as possible to minimize radiated noise.

The winding ratio for the PWS750-2U is 1:1. This means that the output would normally be less than the input due to voltage drops in the FETs, transformer and diode bridge. Since the DC/DC converter is operating at 800kHz, the transformer is starting to operate close to the resonant frequency, which causes the output to increase in magnitude.

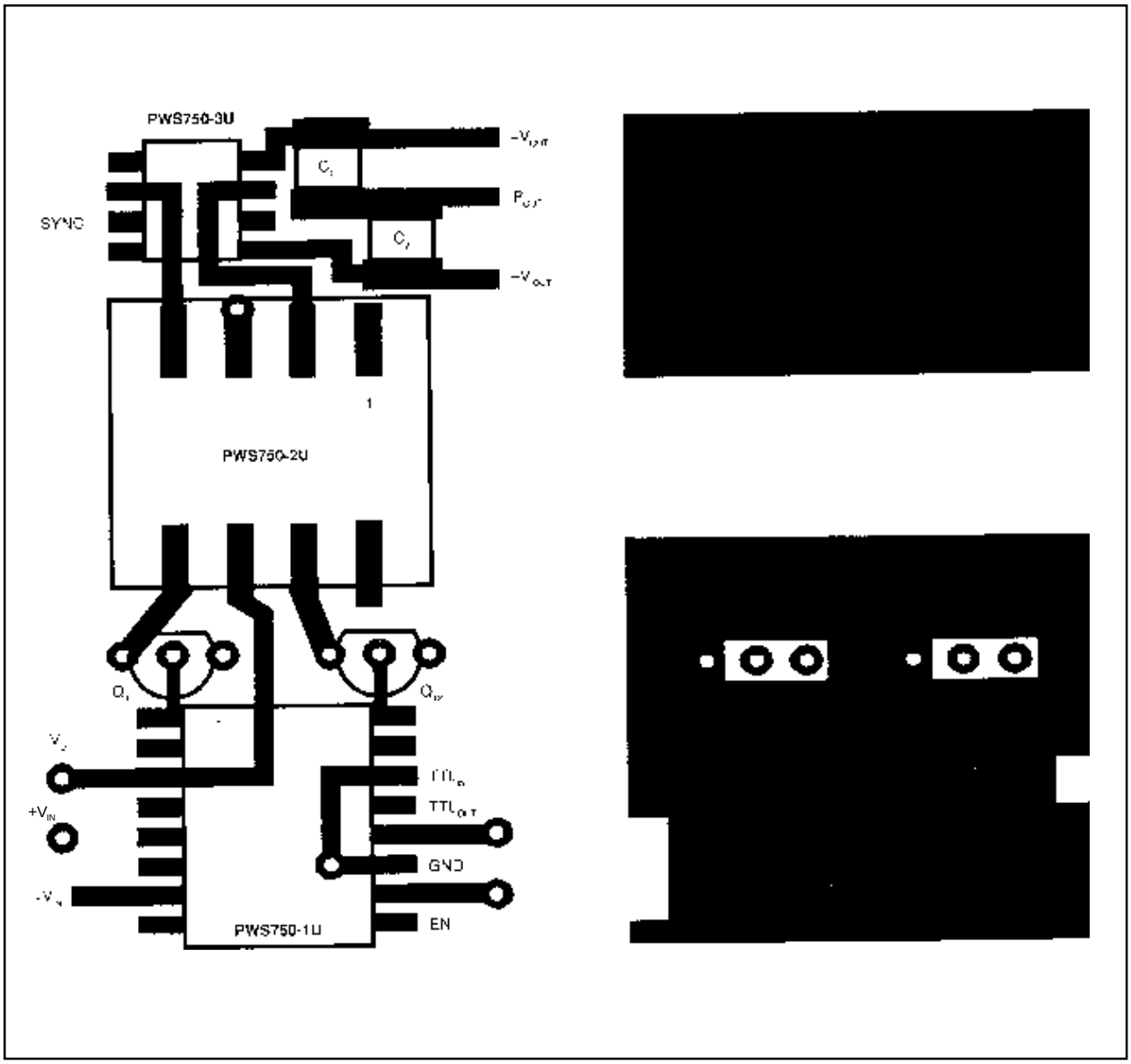


FIGURE 1. Sample PC Board Layout, 4:1.

PWS750-3U HIGH SPEED DIODE BRIDGE PIN FUNCTIONS

The AC pins are tied directly to the AC pins of the PWS750-2U. The +V and –V pins are rectified output voltages. The filter capacitors must be located as close as possible to these pins to minimize series inductance and therefore noise. Bypass capacitors will be needed at each device in the circuit.

BASIC OPERATION

SINGLE CHANNEL OPERATION, PC BOARD LAYOUT CONSIDERATIONS

A simple two-layer board can be used on single channel applications to create a DC/DC converter with low radiated noise. A ground plane should be located directly under both the input and the output components for optimum ground return paths. The surface mount components make it easy to design with a ground plane. The output filter capacitors should be located as close to the PWS750-3U as possible. A sample layout is shown in Figure 1.

For multiple channel applications, T and $\overline{T}$ traces must have minimum capacitive loading. Therefore, there should be no ground plane (or power plane) under these two traces. The driver signal is a 4-6V low current 800kHz signal, which will generate little radiated noise if the traces are kept short.

MULTIPLE CHANNEL OPERATION

The oscillator can drive up to four-channels (eight FETs) directly when operating at 10-18V. A 10Ω resistor must be placed in series with T and $\overline{T}$ to stabilize the FET gate charging. For more than four-channel operation, or 5V-multiple-channel operation, the driver circuit needs a FET booster circuit, as shown in Figure 2. Large gate drive surge currents (>100mA) are needed to turn on the gates.

If the total output current drawn by all the channels exceeds 250mA, then it will be necessary to circumvent the current limit circuit by leaving the V_D pin of the PWS750-1U open, and connect the V_D pin of the PWS750-2U directly to the supply.

5V OPERATION

With 5V operation, the transformer winding current ratio is 3:1, therefore generating much greater currents in the primary. The input ripple voltage will be larger, so an input pi filter will be necessary to isolate the converter noise from the rest of the circuit. For example, when the output is ±15mA the input current will be at least 120mA.

MOSFET	MAX DRIVE CURRENT	PACKAGE	BREAKDOWN
TN0604	4A	TO-92	40V
2N7002	115mA	SO-T23	60V
2N7008	500mA	TO-92	60V
2N7010	1.3A	TO-237	60V
2N7012	1.2A	4-Pin DIP	60V

TABLE I. MOSFET Selector Guide.

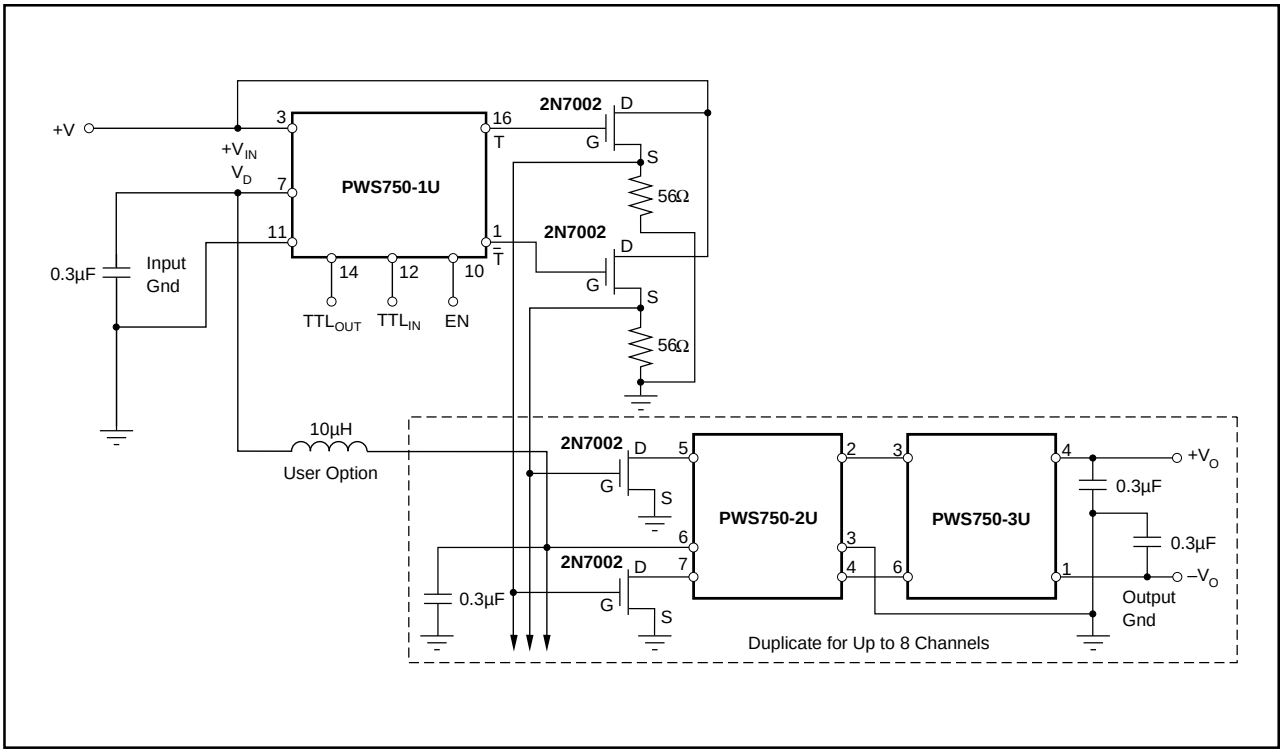


FIGURE 2. MOSFET Driver Booster Circuits.

OUTPUT CURRENT RATING

The PWS750-1U oscillator contains soft start circuitry to protect the FETs from high inrush currents during turn on. The internal input current limit is 250mA peak to prevent thermal overload of the MOSFETs. The maximum output rating is ±30mA. Total current, which can be drawn from each isolation channel, is the total of the power being drawn from both the +V and –V outputs. For example, if one output is not used, then maximum current can be drawn from the other output. In all cases the maximum current that can be drawn from any individual channel is:

$$|+I_{OUT}| + |-I_{OUT}| < 60mA$$

It should be noted that many analog circuit functions do not simultaneously draw equal current from both the positive and negative supplies.

When multiple channel operation is used, the maximum current of all channels must be reduced to prevent the overcurrent limit to trip. Alternately, bypass the overcurrent by leaving the V_D pin of the PWS750-1U open and connecting the V_D pin of the PWS750-2U directly to the supply.

HIGH VOLTAGE TESTING

Burr-Brown Corporation has adopted a partial discharge test criterion that conforms to the German VDE0884 optocoupler standard. This method requires that less than 5pC partial discharge crosses the isolation barrier with 1200Vrms 60Hz applied. This criterion confirms transient overvoltage (1.5 x 750Vrms) protection without damage to the PWS750-2U or PWS750-4U. Life test results verify the absence of high voltage breakdown under continuous rated voltage and maximum temperature.

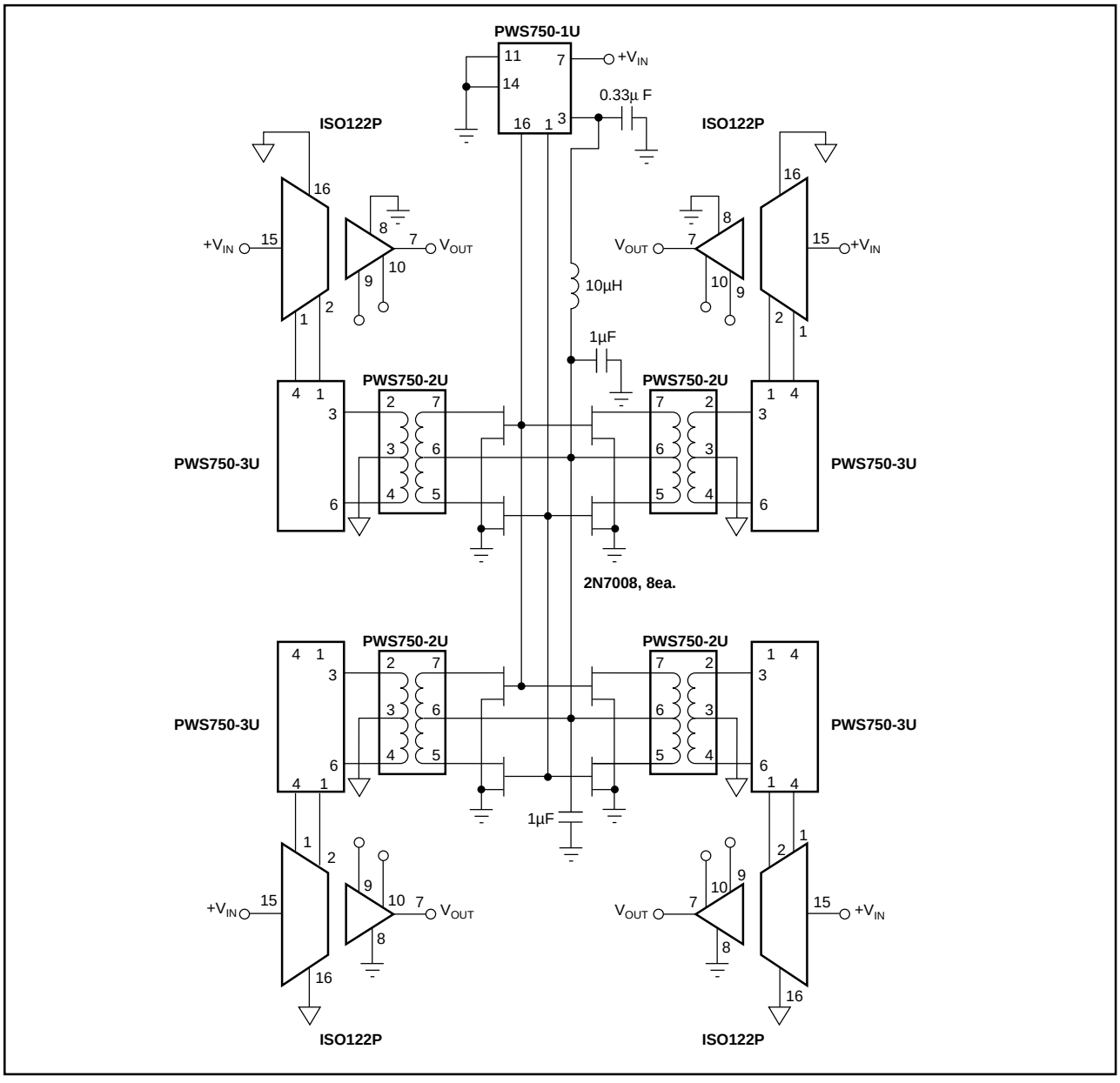


FIGURE 3. Four-Channels of ±10V Signal Isolation with Channel-to-Channel Isolation.

The minimum AC barrier voltage that initiates partial discharge above 5pC is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases; this is known as "extinction voltage." We have developed a package insulation system to yield an inception voltage greater than 1200Vrms so that transient voltages below this level will not damage the isolation barrier. The extinction voltage is above 750Vrms so that even overvoltage-induced partial discharge will cease once the barrier voltage is reduced to the rated value. Previous high voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal units, but not so high as to permanently damage good ones. Our partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

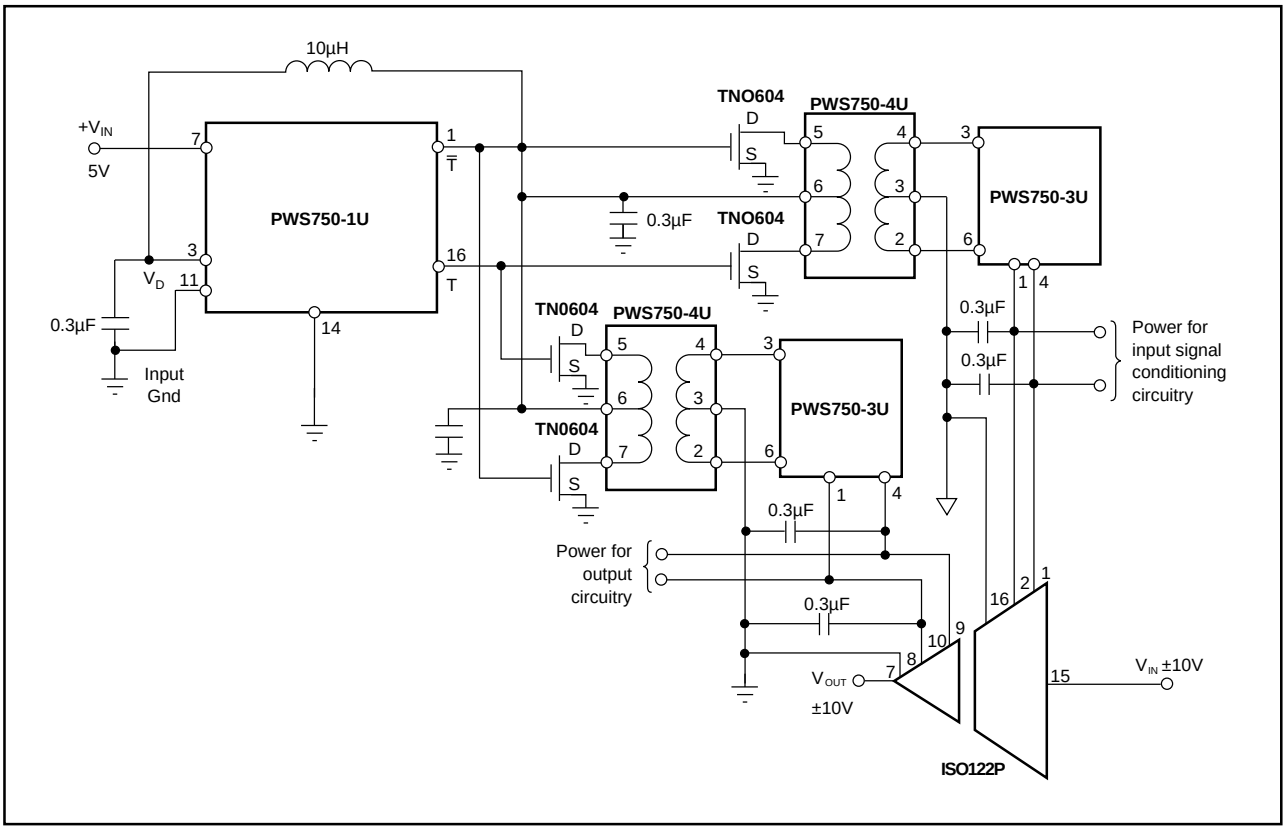


FIGURE 4. A Complete ±10V Signal Acquisition System Operating From a Single 5V Supply.

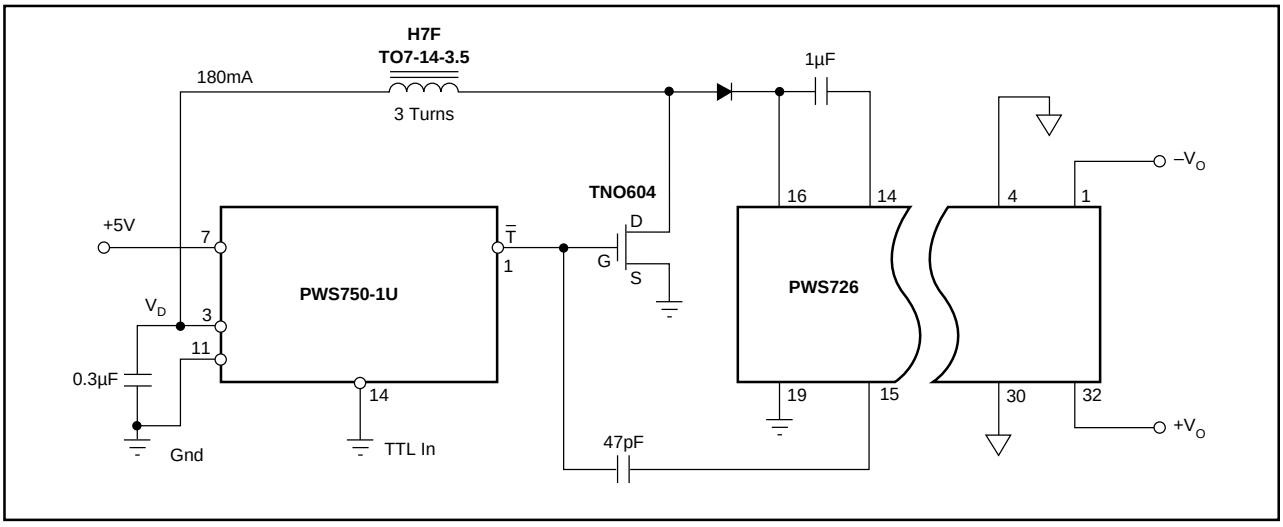


FIGURE 5. A PWS750 Driver Can Be Used to Boost the Input Voltage to 15V to Power a PWS726 From a 5V Supply.

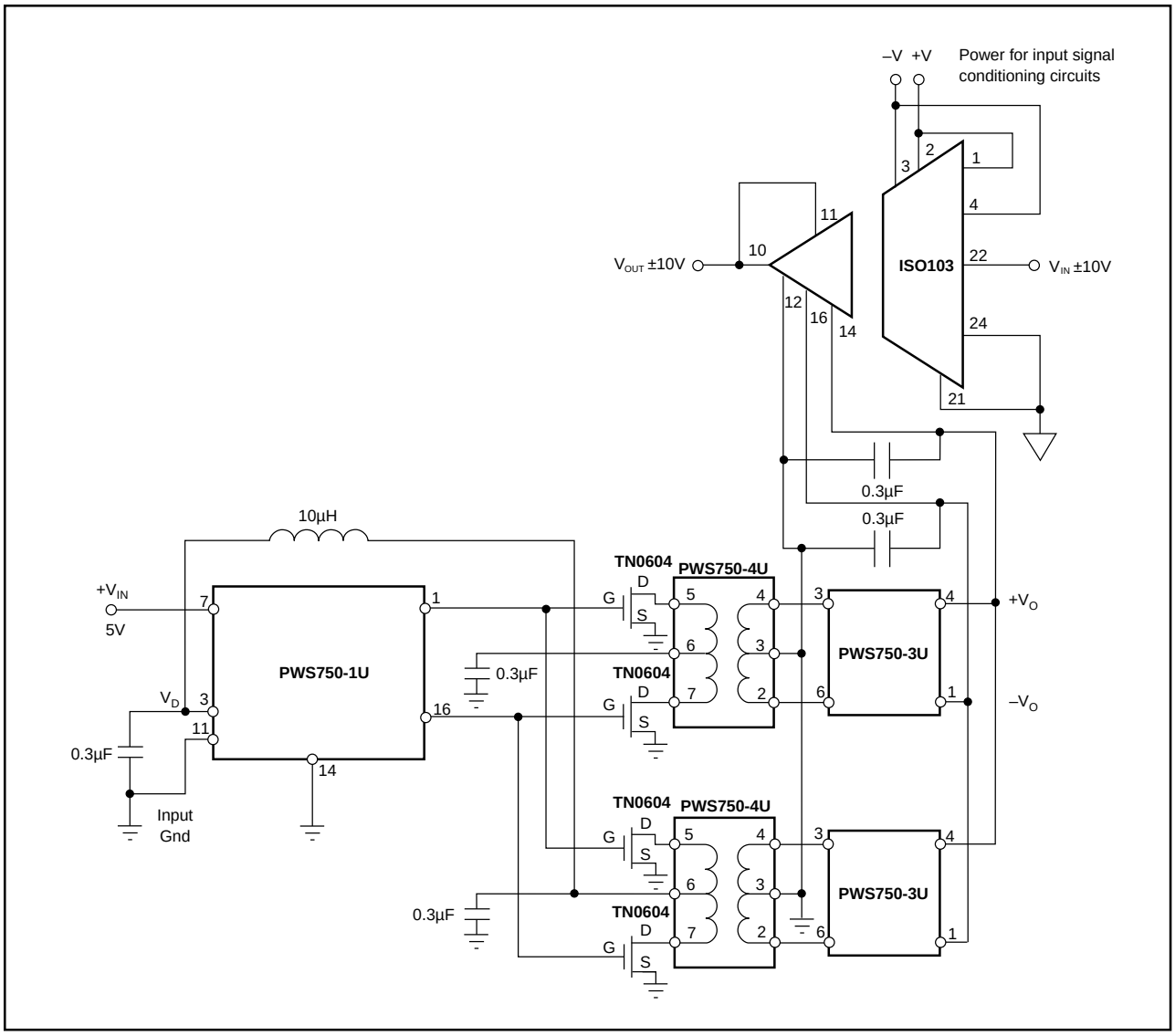


FIGURE 6. Powering the Internally Powered ISO103 Isolation Buffer From a Single 5V Supply. Two Power Channels Are Necessary to Provide the 80mA Nominal for the +V of the ISO103.

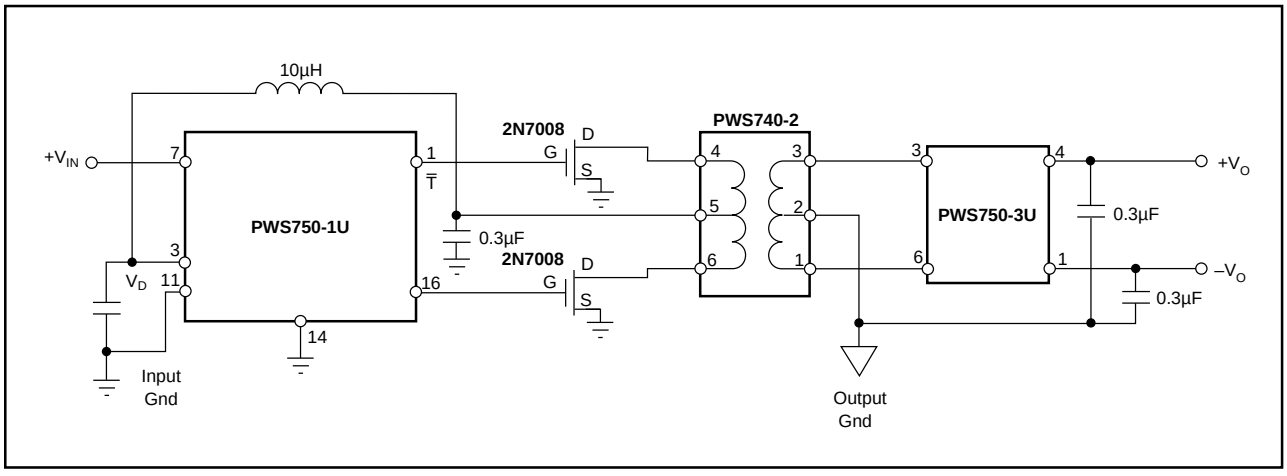


FIGURE 7. 1500VAC Isolation Using PWS740-2 Transformer.

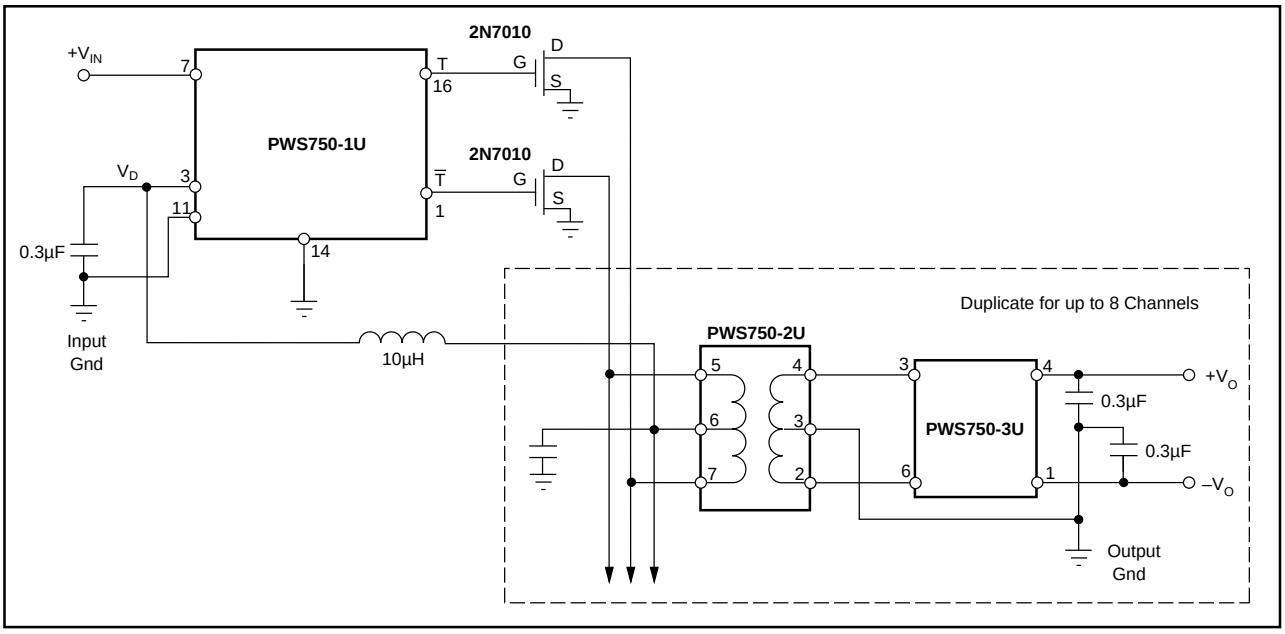


FIGURE 8. FET Pair Driving Up to Eight-Channels.

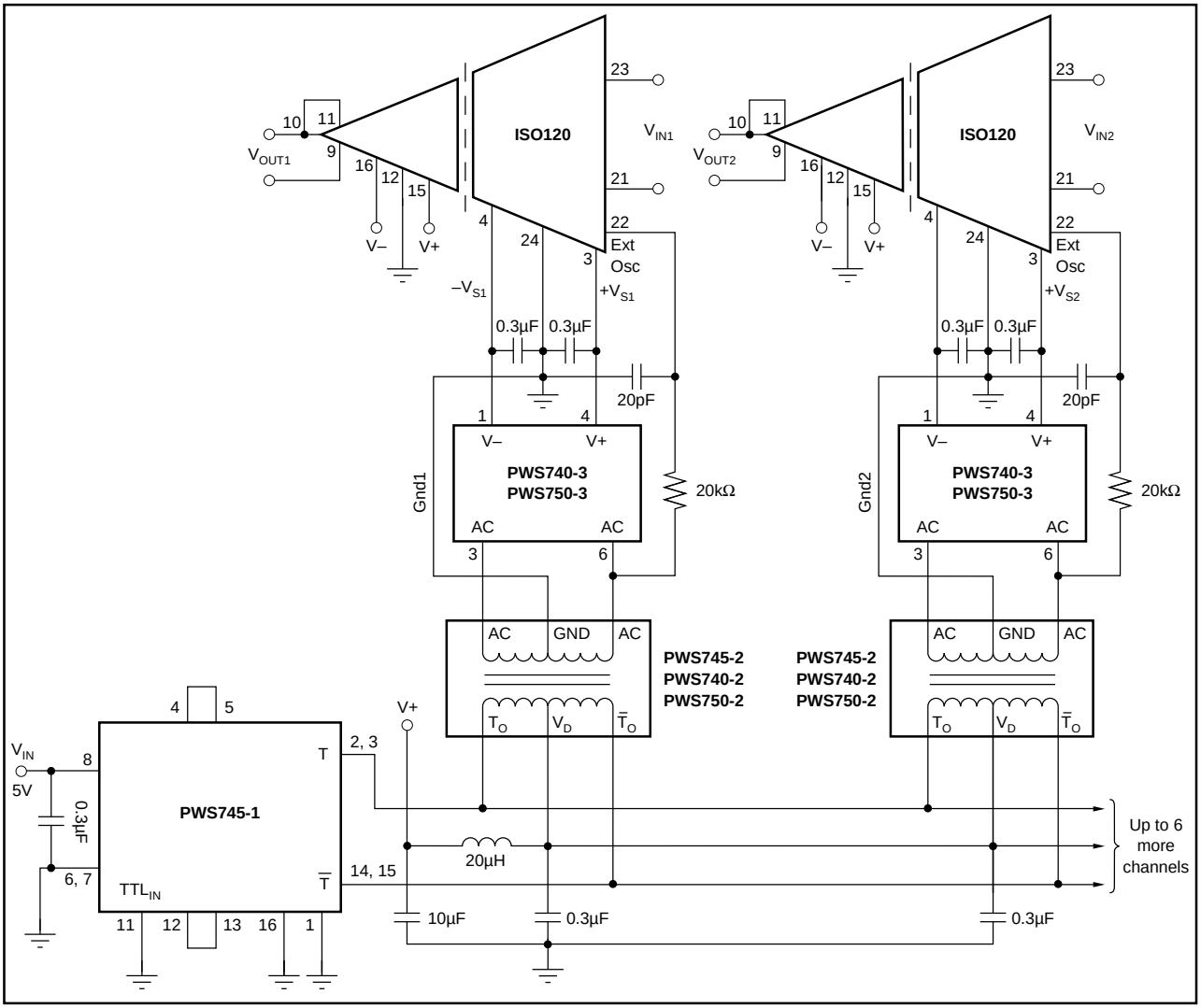


FIGURE 9. Synchronized-Multichannel Isolation System.