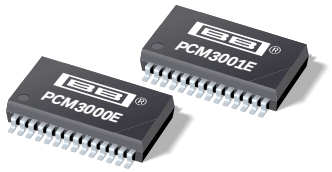
BURR - BROWN®



PCM3000
PCM3001

SoundPLUS™ Stereo Audio CODEC
18-BITS, SERIAL INTERFACE

FEATURES

- **MONOLITHIC 18-BIT ΔΣ ADC AND DAC**
- **16 OR 18-BIT INPUT/OUTPUT DATA**
- **STEREO ADC:**
  Single-ended Voltage Input
  64X Oversampling
  High Performance:
  –88dB THD+N
  94dB SNR
  94dB Dynamic Range
  Digital High-Pass Filter
- **STEREO DAC:**
  Single-ended Voltage Output
  Analog Low Pass Filter
  8X Oversampling Digital Filter
  High Performance:
  –90dB THD+N
  98dB SNR
  97dB Dynamic Range
- **SPECIAL FEATURES (PCM3000):**
  Digital De-emphasis
  Digital Attenuation (256 Steps)
  Soft Mute
  Analog Loop Back
- **SAMPLE RATE: 32kHz, 44.1kHz, 48kHz**
- **SYSTEM CLOCK: 256f_S, 384f_S, 512f_S**
- **SINGLE +5V POWER SUPPLY**
- **SMALL PACKAGE: 28-Pin SSOP**

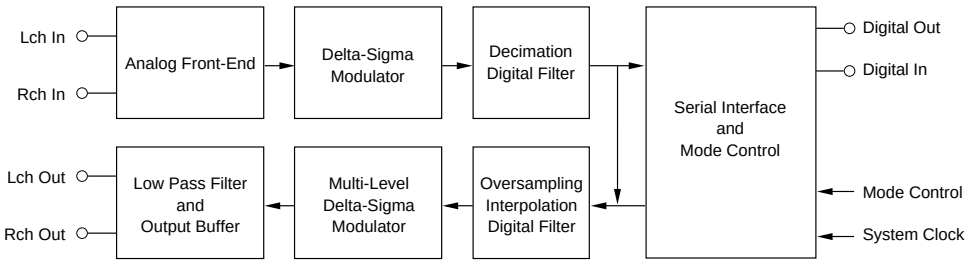
DESCRIPTION

The PCM3000/3001 is a low cost single chip stereo audio CODEC (analog-to-digital and digital-to-analog converter) with single-ended analog voltage input and output.

Both ADCs and DACs employ delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter and the DACs include an 8X oversampling digital interpolation filter. The DACs also include digital attenuation, de-emphasis, infinite zero detection and soft mute to form a complete subsystem. PCM3000/3001 operates with left-justified, right-justified, I^2S or DSP data formats.

PCM3000 can be bit-mapped with a 3-wire serial interface for special features and data formats. PCM3001 can be pin-programmed for data formats.

Fabricated on a highly advanced 0.6µ CMOS process, PCM3000/3001 is suitable for a wide variety of cost-sensitive consumer applications where good performance is required. Applications include sampling keyboards, digital mixers, mini-disc recorders, hard-disk recorders, karaoke systems, DSP-based car stereo, DAT recorders, and video conferencing.



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PDS-1342B
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SPECIFICATIONS

All specifications at +25°C, V_{DD} = V_{CC} = +5V, f_S = 44.1kHz, SYSCLK = 384f_S, CLKIO Input, 18-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM3000E/3001E MIN	PCM3000E/3001E TYP	PCM3000E/3001E MAX	UNITS
DIGITAL INPUT/OUTPUT					
Input Logic					
Input Logic Level: V_{IH}(1)		2.0			VDC
V_{IL}(1)				0.8	VDC
Input Logic Current: I_{IN}(2)				±1	µA
Input Logic Current: I_{IN}(3)				–120	µA
Input Logic Level: V_{IH}(4)		0.64 x V_{DD}			VDC
V_{IL}(4)				0.28 x V_{DD}	VDC
Input Logic Current: I_{IN}(4)				±40	µA
Output Logic					
Output Logic Level: V_{OH}(5)	I_{OUT} = –1.6mA	4.5			VDC
V_{OL}(5)	I_{OUT} = +3.2mA			0.5	VDC
Output Logic Level: V_{OH}(6)	I_{OUT} = –3.2mA	4.5			VDC
V_{OL}(6)	I_{OUT} = +3.2mA			0.5	VDC
CLOCK FREQUENCY					
Sampling Frequency (f_S)		32	44.1	48	kHz
System Clock Frequency	256f_S	8.1920	11.2896	12.2880	MHz
	384f_S	12.2880	16.9344	18.4320	MHz
	512f_S	16.3840	22.5792	24.5760	MHz
ADC CHARACTERISTICS					
RESOLUTION		18			Bits
DC ACCURACY					
Gain Mismatch Channel-to-Channel			±1.0	±5.0	% of FSR
Gain Error			±2.0	±5.0	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error	High-Pass Filter Off(7)		±1.7		%of FSR
Bipolar Zero Drift	High-Pass Filter Off(7)		±20		ppm of FSR/°C
DYNAMIC PERFORMANCE(8)					
THD+N: V_{IN} = –0.5dB	f = 1kHz		–88	–80	dB
V_{IN} = –60dB	f = 1kHz		–51		dB
Dynamic Range	f = 1kHz, A-Weighted	90	94		dB
Signal-to-Noise Ratio	f = 1kHz, A-Weighted	90	94		dB
Channel Separation		88	92		dB
DIGITAL FILTER PERFORMANCE(8)					
Passband				0.454f_S	Hz
Stopband		0.583f_S			Hz
Passband Ripple				±0.05	dB
Stopband Attenuation		–65			dB
Delay Time (Latency)			17.4/f_S		sec
DIGITAL HIGH PASS FILTER RESPONSE					
–3dB Frequency			0.019f_S		mHz
ANALOG INPUT					
Voltage Range	0dB (Full Scale)		2.9		Vp-p
Center Voltage			2.1		V
Input Impedance			15		kΩ
ANTI-ALIASING FILTER					
–3dB Frequency	C_{EXT} = 470pF		170		kHz

NOTES: (1) Pins 16, 17, 18, 22, 25, 26, 27, 28: LRCIN, BCKIN, DIN, CLKIO, MC/FMT2, MD/FMT1, ML/FMT0, RSTB. (2) Pins 16, 17, 18, 22: LRCIN, BCKIN, DIN, CLKIO (Schmitt Trigger Input). (3) Pins 25, 26, 27, 28: MC/FMT2, MD/FMT1, ML/FMT0, RSTB (Schmitt Trigger Input, 70kΩ Internal Pull-Up Resistor). (4) Pin 20: XTI. (5) Pins 19, 22: DOUT,CLKIO. (6) Pin 21: XTO. (7) High Pass Filter disabled (PCM3000 only) to measure DC offset. (8) f_{IN} = 1kHz, using Audio Precision System II, rms mode with 20kHz LPF, 400Hz HPF used for performance calculation. (9) With no load on XTO and CLKIO.

SPECIFICATIONS (CONT)

All specifications at +25°C, V_{DD} = V_{CC} = 5V, f_S = 44.1kHz, SYSCLK = 384f_S, CLKIO Input, 18-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM3000E/3001E MIN	PCM3000E/3001E TYP	PCM3000E/3001E MAX	UNITS
DAC CHARACTERISTICS					
RESOLUTION		18			Bits
DC ACCURACY					
Gain Mismatch Channel-to-Channel			±1.0	±5.0	% of FSR
Gain Error			±1.0	±5.0	% of FSR
Gain Drift			±20		ppm of FSR/°C
Bipolar Zero Error			±1.0		% of FSR
Bipolar Zero Drift			±20		ppm of FSR/°C
DYNAMIC PERFORMANCE[8]					
THD+N: V_{OUT} = 0dB (Full Scale)			–90	–80	dB
V_{OUT} = –60dB			–34		dB
Dynamic Range	A-Weighted	90	97		dB
Signal-to-Noise Ratio (Idle Channel)	A-Weighted	92	98		dB
Channel Separation		90	95		dB
DIGITAL FILTER PERFORMANCE					
Passband				0.445f_S	Hz
Stopband		0.555f_S			Hz
Passband Ripple				±0.17	dB
Stopband Attenuation		–35			dB
Delay Time			11.1/f_S		sec
ANALOG OUTPUT					
Voltage Range			0.62 x V_{CC}		Vp-p
Center Voltage			0.5 x V_{CC}		VDC
Load Impedance	AC Load	5			kΩ
ANALOG LOW PASS FILTER					
Frequency Response	f = 20kHz		–0.16		dB
POWER SUPPLY REQUIREMENTS					
Voltage Range: V_{CC}		4.5	5	5.5	VDC
V_{DD}		4.5	5	5.5	VDC
Supply Current: $+I_{CC}$, $+I_{DD}$[9]	V_{CC} = V_{DD} = 5V		32	50	mA
Power Dissipation	V_{CC} = V_{DD} = 5V		160	250	mW
TEMPERATURE RANGE					
Operation		–25		+85	°C
Storage		–55		+125	°C

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]
PCM3000E/3001E	28-Pin SSOP	324

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

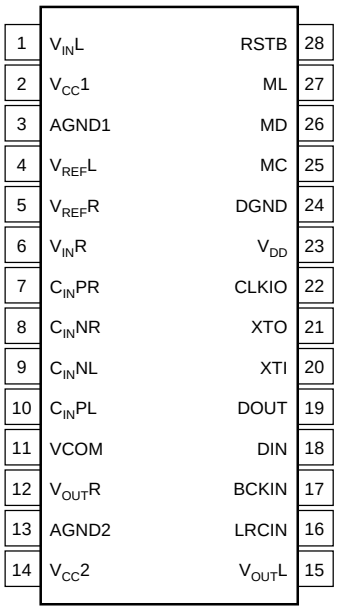
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
$+V_{DD}$, $+V_{CC}1$, $+V_{CC}2$ ..... +6.5V
Supply Voltage Differences ..... ±0.1V
GND Voltage Differences ..... ±0.1V
Digital Input Voltage ..... –0.3 to V_{DD} + 0.3V
Analog Input Voltage ..... –0.3 to $V_{CC}1$, $V_{CC}2$ + 0.3V
Power Dissipation 300mW
Input Current ..... ±10mA
Operating Temperature Range ..... –25°C to +85°C
Storage Temperature ..... –55°C to +125°C
Lead Temperature (soldering, 5s) ..... +260°C
(reflow, 10s) ..... +235°C
Thermal Resistance, θ_{JA} ..... 100°C/W

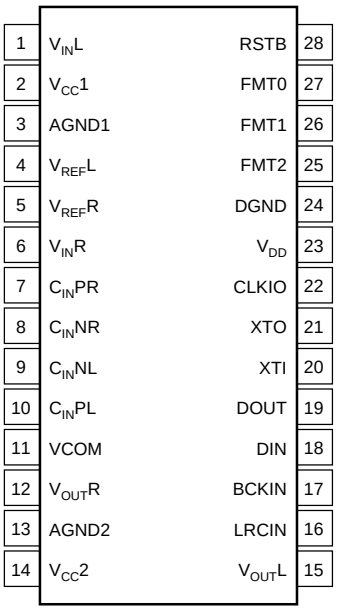
PIN CONFIGURATION—PCM3000

Top View **SSOP**



PIN CONFIGURATION—PCM3001

Top View **SSOP**



PIN ASSIGNMENTS PCM3000/3001

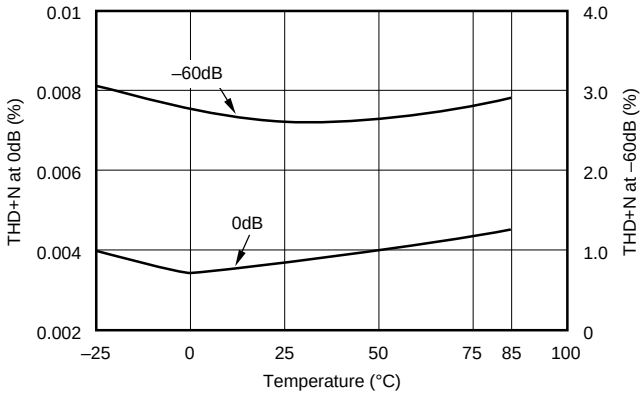
PIN	NAME	I/O	DESCRIPTION
1	$V_{IN}L$	IN	ADC Analog Input, Lch
2	$V_{CC}1$	—	ADC Analog Power Supply
3	AGND1	—	ADC Analog Ground
4	$V_{REF}L$	—	ADC Input Reference, Lch
5	$V_{REF}R$	—	ADC Input Reference, Rch
6	$V_{IN}R$	IN	ADC Analog Input, Rch
7	$C_{IN}PR$	—	ADC Anti-alias Filter Capacitor (+), Rch
8	$C_{IN}NR$	—	ADC Anti-alias Filter Capacitor (–), Rch
9	$C_{IN}NL$	—	ADC Anti-alias Filter Capacitor (–), Lch
10	$C_{IN}PL$	—	ADC Anti-alias Filter Capacitor (+), Lch
11	VCOM	—	DAC Output Common
12	$V_{OUT}R$	OUT	DAC Analog Output, Rch
13	AGND2	—	DAC Analog Ground
14	$V_{CC}2$	—	DAC Analog Power Supply
15	$V_{OUT}L$	OUT	DAC Analog Output, Lch
16	LRCIN	IN	Sample Rate Clock Input (f_S)[2]
17	BCKIN	IN	Bit Clock Input
18	DIN	IN	Data Input
19	DOUT	OUT	Data Output
20	XTI	IN	Oscillator Input
21	XTO	OUT	Oscillator Output
22	CLKIO	I/O	Buffered Output of Oscillator or External Clock Input[2]
23	V_{DD}	—	Digital Power Supply
24	DGND	—	Digital Ground
25	MC/FMT2	IN	Serial Control Bit Clock (PCM3000)/Data Format Control 2 (PCM3001)[1, 2]
26	MD/FMT1	IN	Serial Control Data (PCM3000)/Data Format Control 1 (PCM3001)[1, 2]
27	ML/FMT0	IN	Serial Control Strobe Pulse/Data Format Control 0 (PCM3001)[1, 2]
28	RSTB	IN	Reset[1]

NOTES: (1) With 70kΩ typical internal pull-up resistor. (2) Schmitt trigger input.

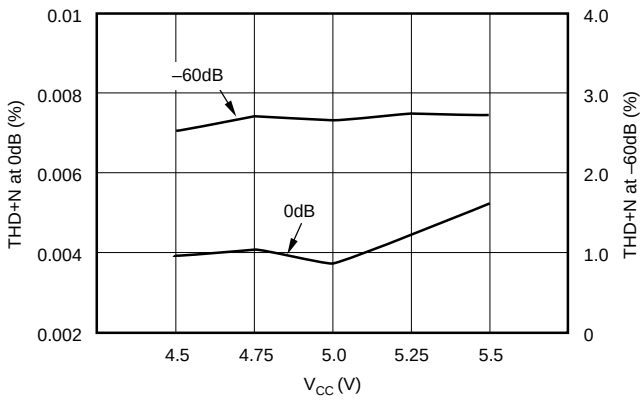
TYPICAL PERFORMANCE CURVES
ADC SECTION

At T_A = +25°C, V_{CC} = V_{DD} = +5V, f_{IN} = 1.0kHz, V_{IN} = 2.9Vp-p, and SYSCLK = 384f_S, unless otherwise noted.

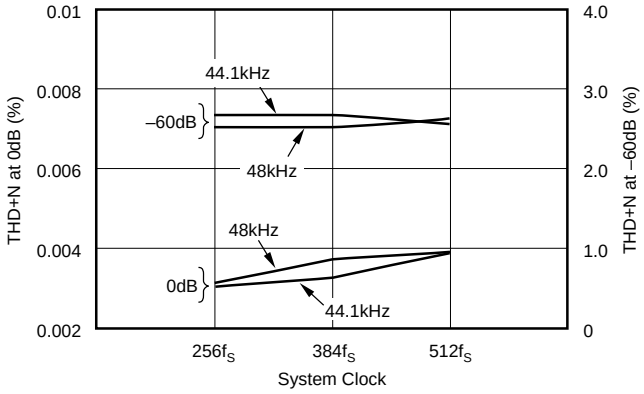
THD+N vs TEMPERATURE



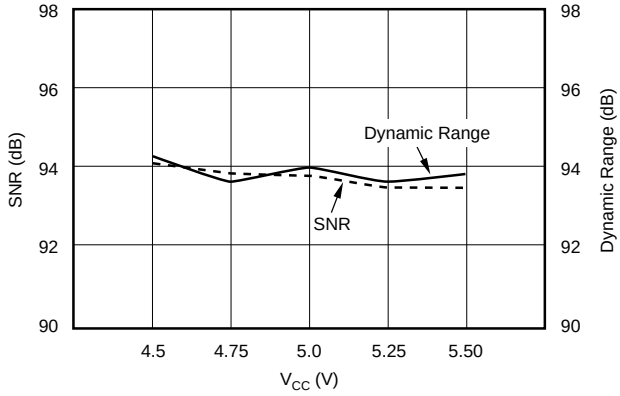
THD+N vs POWER SUPPLY



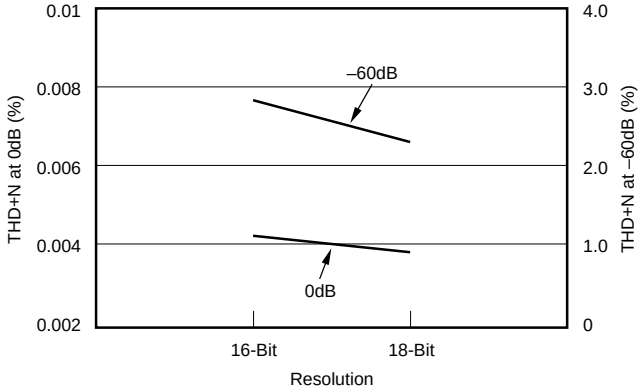
THD+N vs SYSTEM CLOCK
and SAMPLING FREQUENCY



SNR and DYNAMIC RANGE vs POWER SUPPLY



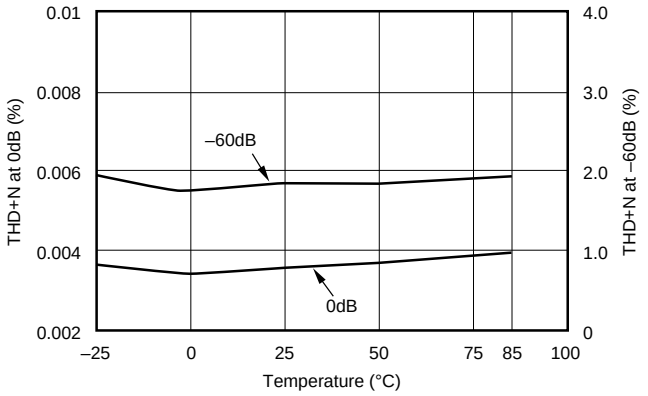
THD+N vs OUTPUT DATA RESOLUTION



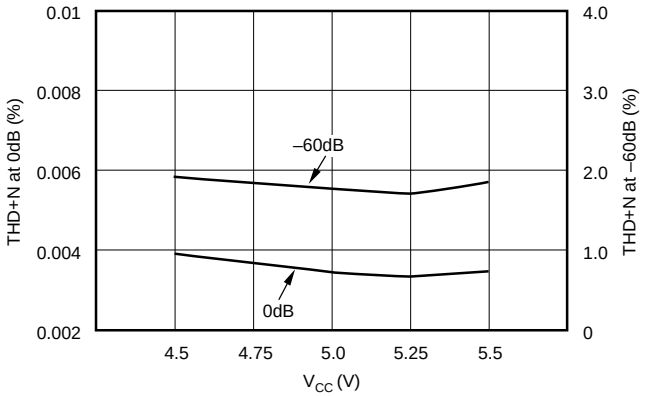
TYPICAL PERFORMANCE CURVES
DAC SECTION

At T_A = +25°C, V_{CC} = V_{DD} = +5V, f_{IN} = 1.0kHz, and SYSCLK = 384f_S, unless otherwise noted.

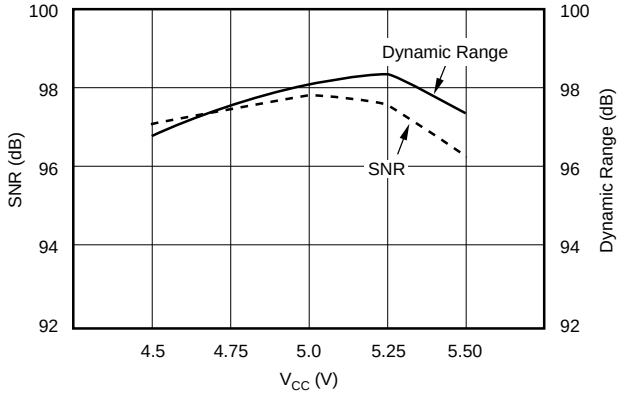
THD+N vs TEMPERATURE



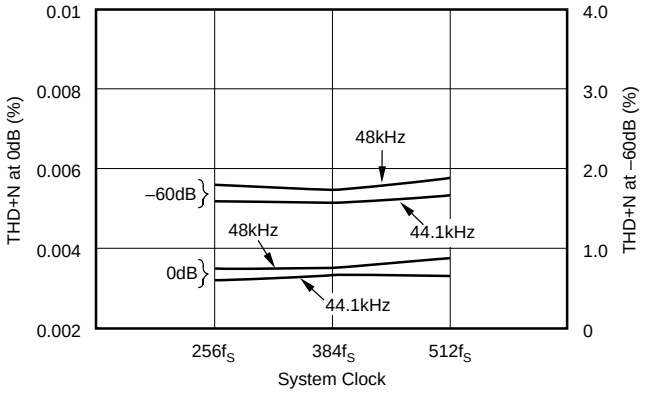
THD+N vs POWER SUPPLY



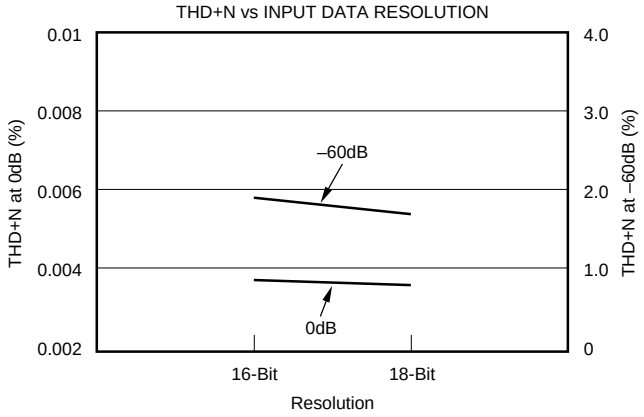
SNR and DYNAMIC RANGE vs POWER SUPPLY



THD+N vs SYSTEM CLOCK
and SAMPLING FREQUENCY



THD+N vs INPUT DATA RESOLUTION

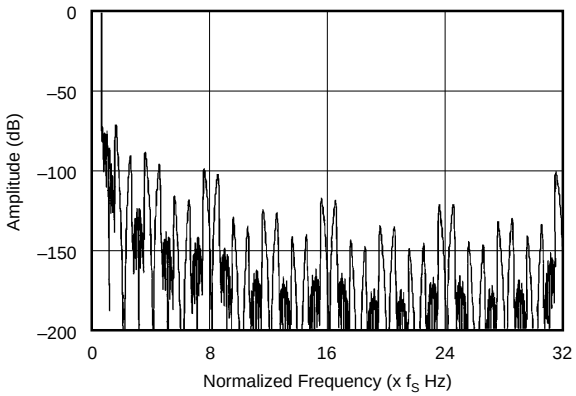


TYPICAL PERFORMANCE CURVES

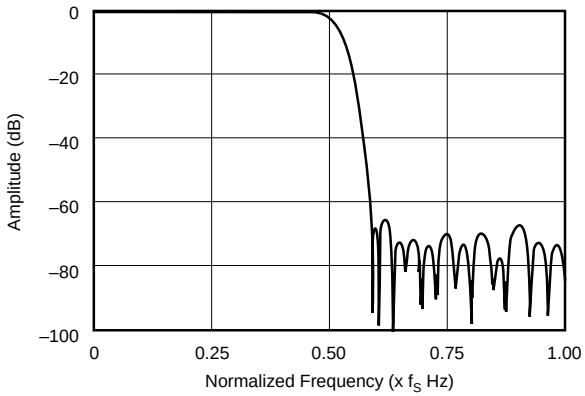
At T_A = +25°C, V_{CC} = V_{DD} = +5V, and SYSCLK = 384f_S, unless otherwise noted.

ADC DIGITAL FILTER

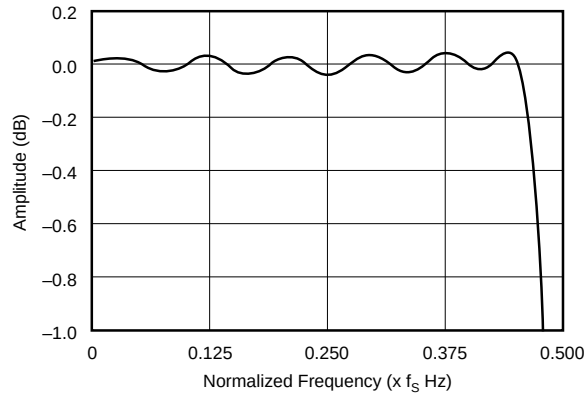
OVERALL CHARACTERISTICS



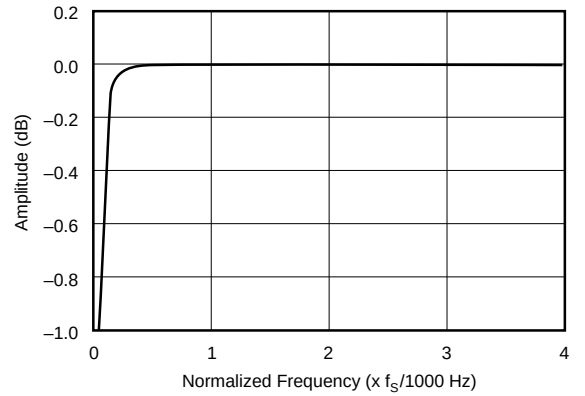
STOPBAND ATTENUATION CHARACTERISTICS



PASSBAND RIPPLE CHARACTERISTICS

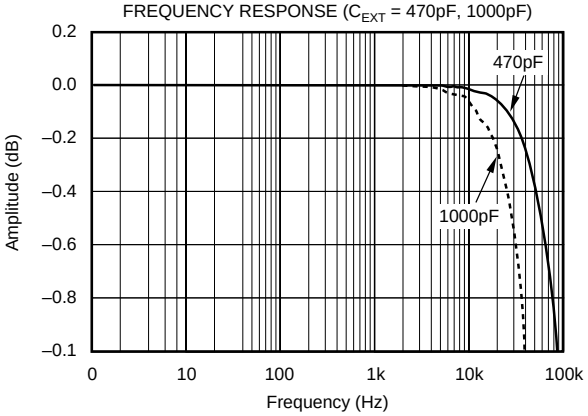


HIGH PASS FILTER RESPONSE

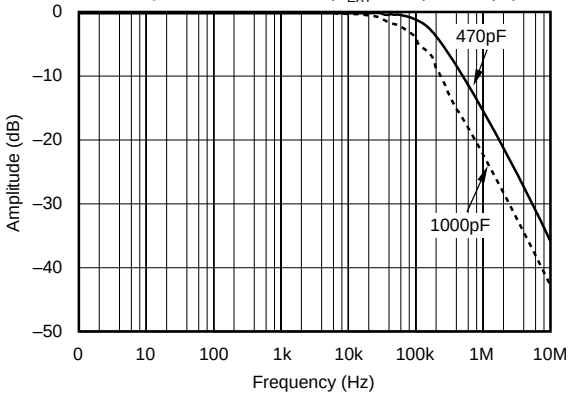


ANTI-ALIASING FILTER

ANTI-ALIASING FILTER PASSBAND
FREQUENCY RESPONSE (C_{EXT} = 470pF, 1000pF)



ANTI-ALIASING FILTER OVERALL
FREQUENCY RESPONSE (C_{EXT} = 470pF, 1000pF)

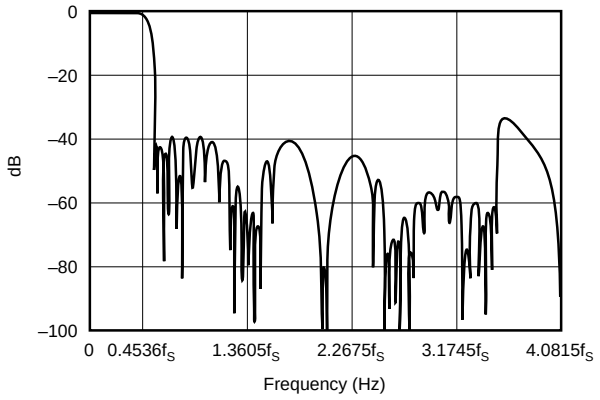


TYPICAL PERFORMANCE CURVES

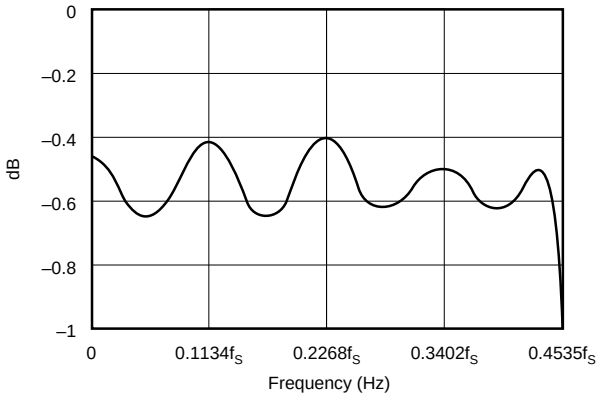
At T_A = +25°C, V_{CC} = V_{DD} = +5V, and SYSCLK = 384f_S, unless otherwise noted.

DAC DIGITAL FILTER

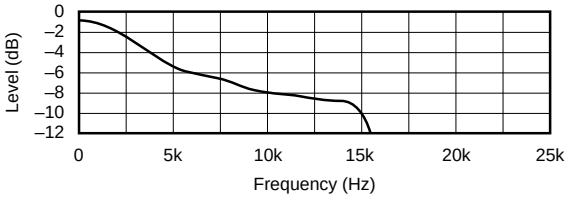
OVERALL FREQUENCY CHARACTERISTIC



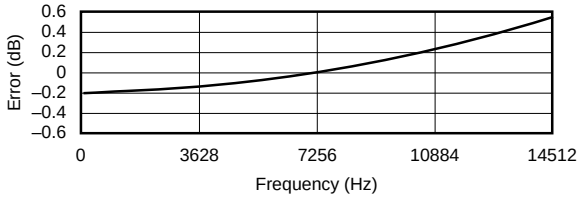
PASSBAND RIPPLE CHARACTERISTIC



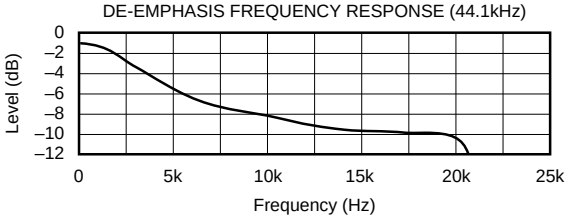
DE-EMPHASIS FREQUENCY RESPONSE (3kHz)



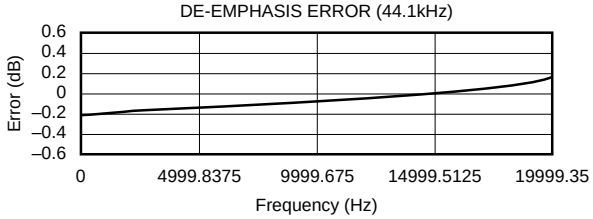
DE-EMPHASIS ERROR (3kHz)



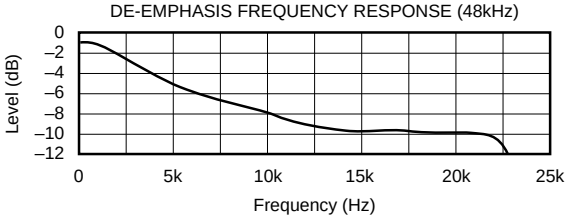
DE-EMPHASIS FREQUENCY RESPONSE (44.1kHz)



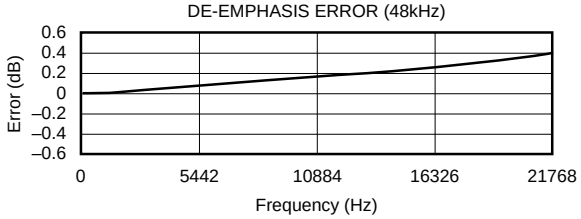
DE-EMPHASIS ERROR (44.1kHz)



DE-EMPHASIS FREQUENCY RESPONSE (48kHz)

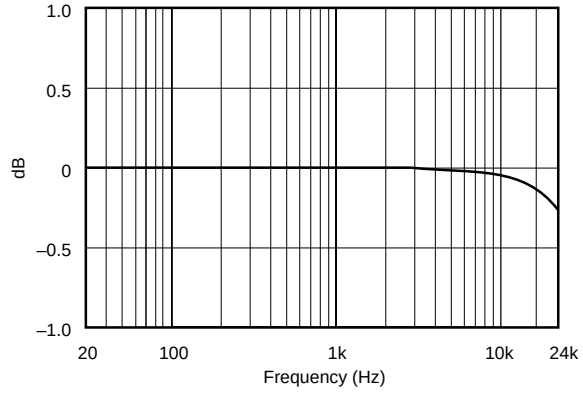


DE-EMPHASIS ERROR (48kHz)

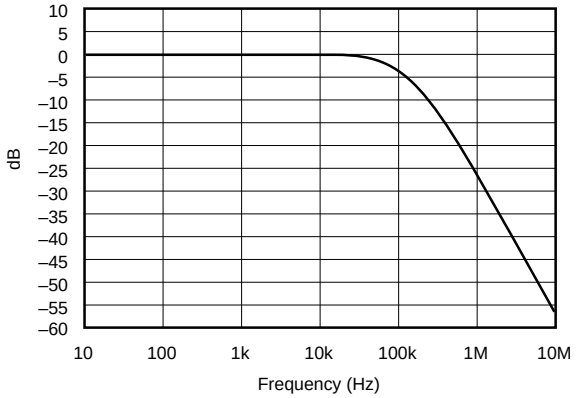


ANALOG OUTPUT FILTER

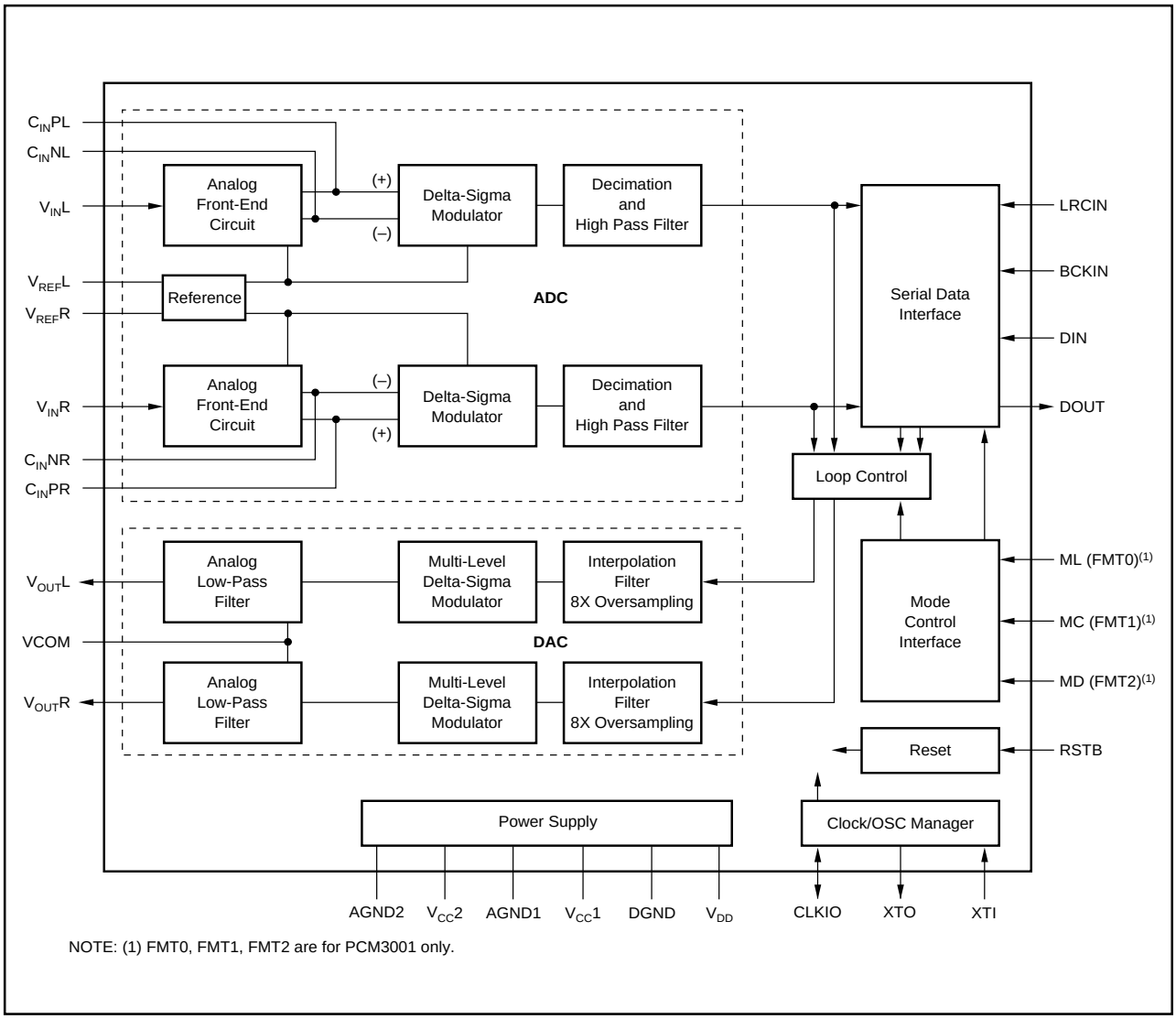
INTERNAL ANALOG FILTER FREQUENCY RESPONSE
(20Hz~24kHz, Expanded Scale)



INTERNAL ANALOG FILTER FREQUENCY RESPONSE
(10Hz~10MHz)



BLOCK DIAGRAM



NOTE: (1) FMT0, FMT1, FMT2 are for PCM3001 only.

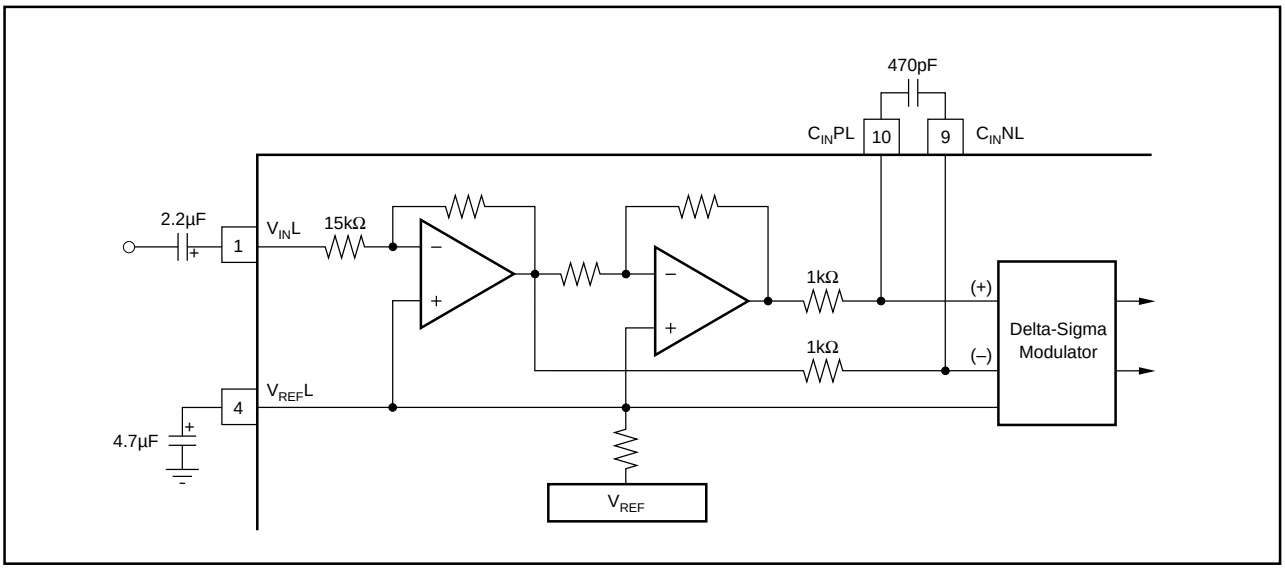


FIGURE 1. Analog Front-End (Single-Channel).

PCM AUDIO INTERFACE

The three-wire digital audio interface for PCM3000/3001 is on LRCIN (Pin 16), BCKIN (Pin 17), DIN (Pin 18), and DOUT (Pin 19). PCM3000/3001 can operate with seven different data formats. For PCM3000, these formats are selected through PROGRAM REGISTER 3 in the software mode. For PCM3001, data formats are selected by pin-strapping the three format pins. Figures 2, 3 and 4 illustrate audio data input/output format and timing.

PCM3000/3001 can accept 32, 48, or 64 bit clocks (BCKIN) in one clock of LRCIN. Only formats 0, 2, and 6 can be selected when 32 bit clocks/LRCIN are applied.

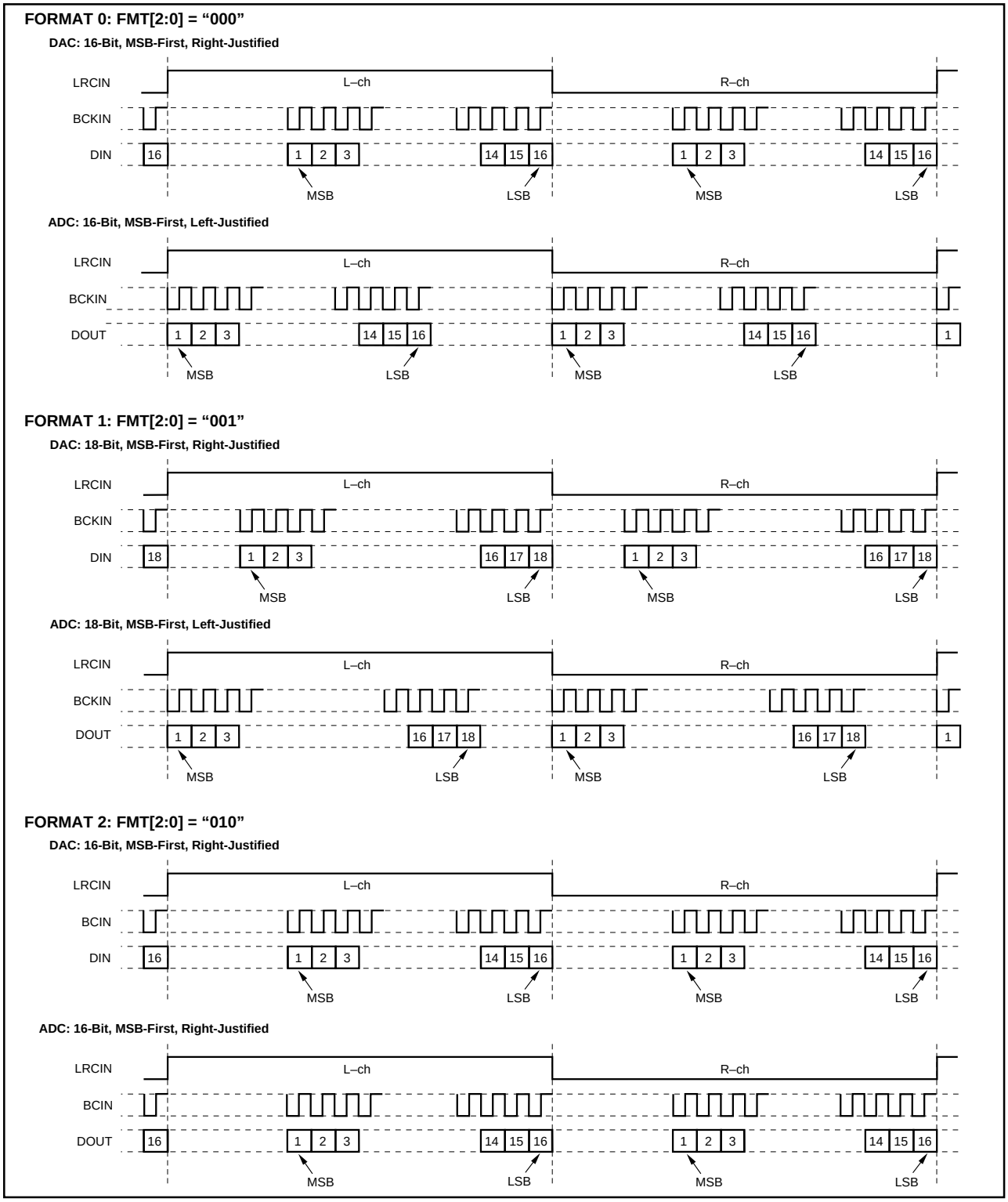


FIGURE 2. Audio Data Input/Output Format.

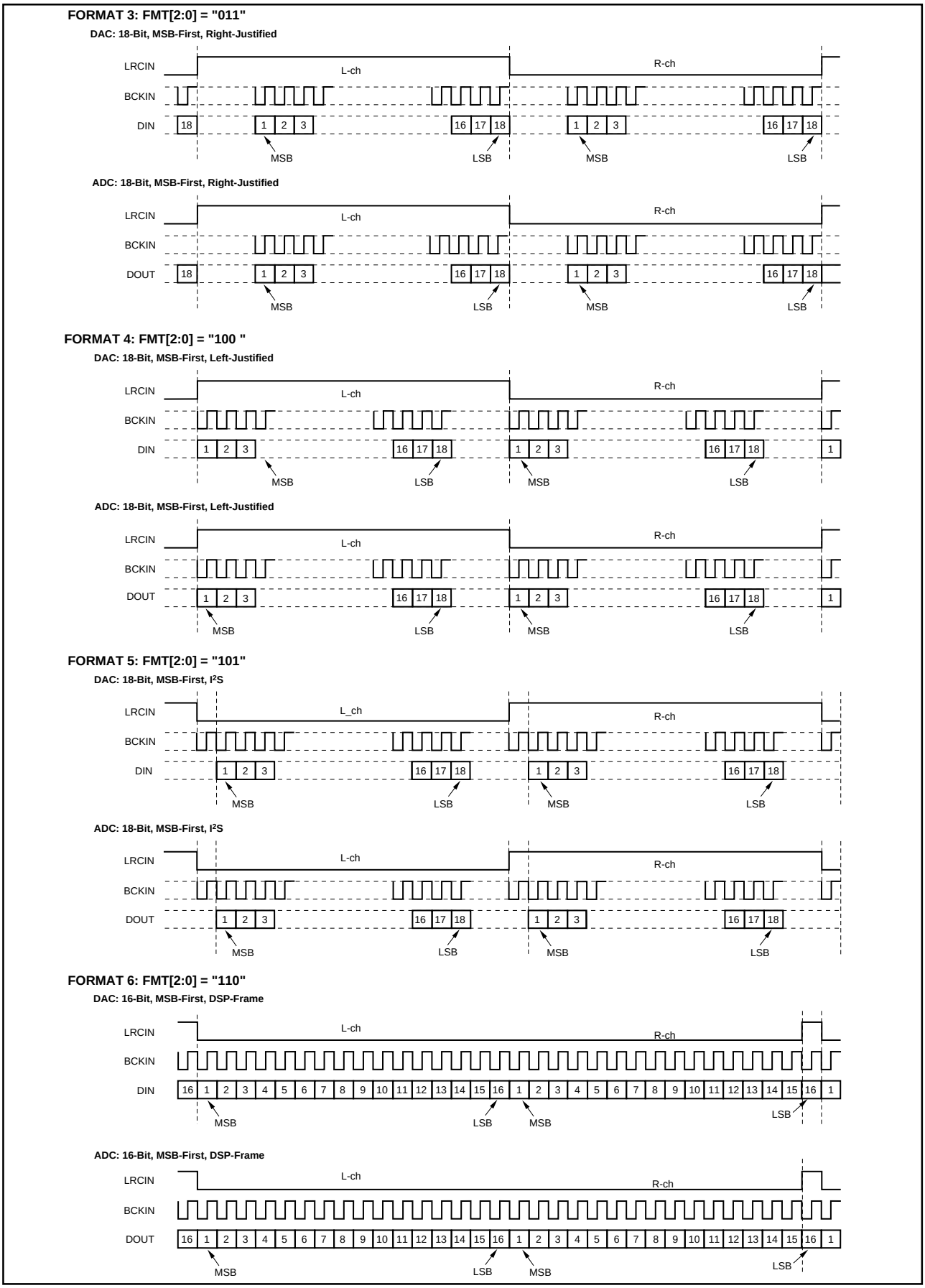
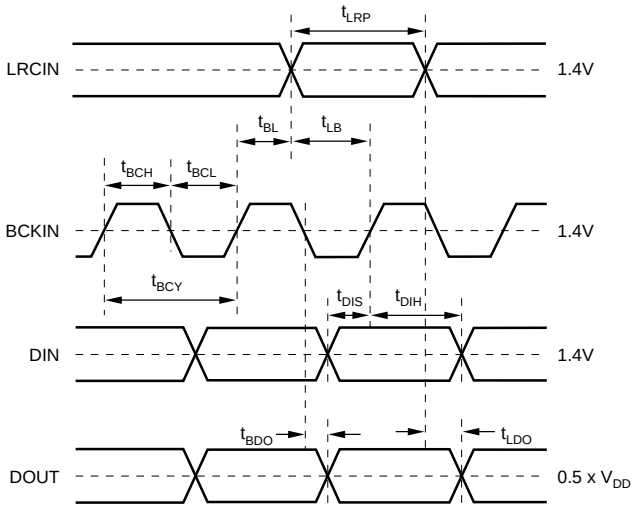


FIGURE 3. Audio Data Input/Output Format.



BCKIN Pulse Cycle Time	t_{BCY}	300ns (min)
BCKIN Pulse Width High	t_{BCH}	120ns (min)
BCKIN Pulse Width Low	t_{BCL}	120ns (min)
BCKIN Rising Edge to LRCIN Edge	t_{BL}	40ns (min)
LRCIN Edge to BCKIN Rising Edge	t_{LB}	40ns (min)
LRCIN Pulse Width	t_{LRP}	t_{BCY} (min)
DIN Set-up Time	t_{DIS}	40ns (min)
DIN Hold Time	t_{DIH}	40ns (min)
DOUT Delay Time to BCKIN Falling Edge	t_{BDO}	40ns (max)
DOUT Delay Time to LRCIN Edge	t_{LDO}	40ns (max)
Rising Time of All Signals	t_{RISE}	20ns (max)
Falling Time of All Signals	t_{FALL}	20ns (max)

FIGURE 4. Audio Data Input/Output Timing.

SYSTEM CLOCK

The system clock for PCM3000/3001 must be either $256f_S$, $384f_S$ or $512f_S$, where f_S is the audio sampling frequency. The system clock can be either a crystal oscillator placed between XTI (Pin 20) and XTO (Pin 21), or an external clock input. If an external clock is used, the clock is provided to either XTI or CLKIO (Pin 22), and XTO is open. PCM3000/3001 has an XTI clock detection circuit which senses if an XTI clock is operating. When the external clock is delivered to XTI, CLKIO is a buffered output of XTI. When XTI is connected to ground, the external clock must be tied to CLKIO. For best performance, the "External Clock Input 2" circuit in Figure 5 is recommended.

PCM3000/3001 also has a system clock detection circuit which automatically senses if the system clock is operating at $256f_S$, $384f_S$, or $512f_S$. When $384f_S$ or $512f_S$ system clock is used, the clock is divded into $256f_S$ automatically. The $256f_S$ clock is used to operate the digital filter and the modulator.

Table I lists the relationship of typical sampling frequencies and system clock frequencies, and Figures 5 and 6 illustrate the typical system clock connections and external system clock timing.

SAMPLING RATE FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHz)		
	$256f_S$	$384f_S$	$512f_S$
32	8.1920	12.2880	16.3840
44.1	11.2896	16.9340	22.5792
48	12.2880	18.4320	24.5760

TABLE I. System Clock Frequencies.

RESET

PCM3000/3001 has an internal power-on reset circuit, as well as an external forced reset (RSTB, Pin 28). The internal power-on reset initializes (resets) when the supply voltage V_{DD} >4V (typ). External forced reset occurs when RSTB = LOW, setting the outputs of the DAC to $V_{CC}/2$. The power-on reset has an initialization period equal to 1024 system clock periods after V_{DD} >4V and RSTB = "HIGH". During

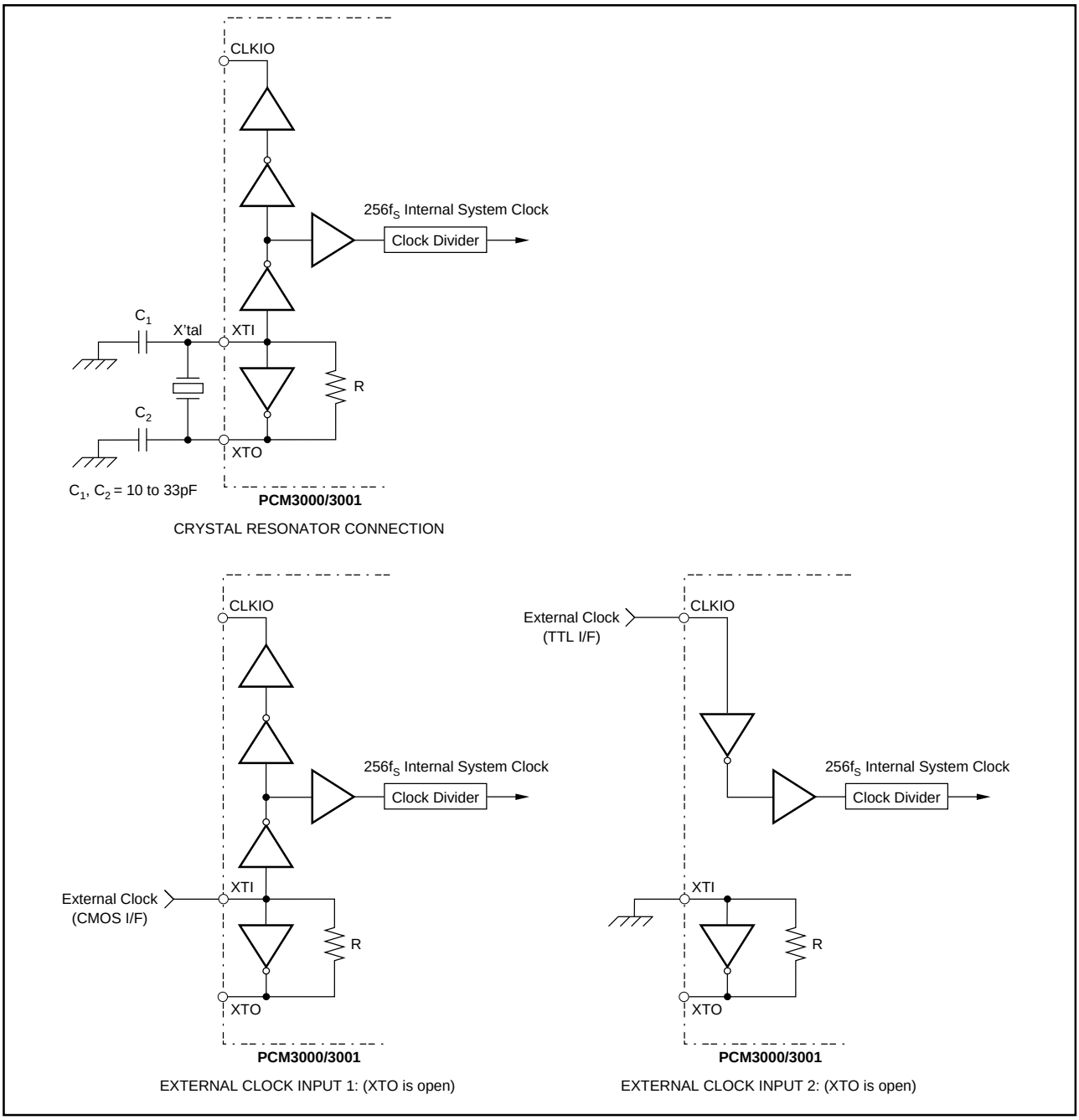


FIGURE 5. System Clock Connections.

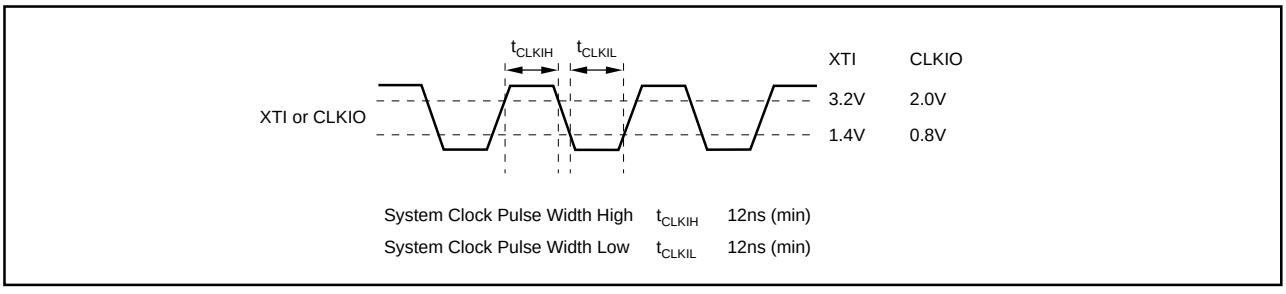


FIGURE 6. External System Clock Timing.

the initialization period, the outputs of the DAC are invalid, and the analog outputs are forced to $V_{CC}/2$. The output of the ADC is also invalid during initialization or forced reset, and the digital outputs are forced to all zeroes. Digital output data is valid after $4096/f_S$ once reset conditions are removed. Figures 7 and 8 illustrate the power-on reset and reset-pin reset timing.

SYNCHRONIZATION WITH THE DIGITAL AUDIO SYSTEM

PCM3000/3001 operates with LRCIN synchronized to the system clock. The CODEC does not require any specific phase relationship between LRCIN and the system clock, but there must be synchronization. If the synchronization between the system clock and LRCIN changes more than 6 bit

FUNCTION	ADC/DAC	DEFAULT (PCM3000/3001)
Audio Data Format (7 Selectable Formats)	ADC/DAC	DAC: 16-bit, MSB-first, Right-Justified ADC: 16-bit, MSB-first, Left-Justified
LRCIN Polarity	ADC/DAC	Left/Right = High/Low
Loop Back Control	ADC/DAC	OFF
Left Channel Attenuation	DAC	0dB
Right Channel Attenuation	DAC	0dB
Attenuation Control	DAC	Left Channel and Right Channel = Individual Control
Infinite Zero Detection	DAC	OFF
DAC Output Control	DAC	Output Enabled
Soft Mute Control	DAC	OFF
De-emphasis (OFF, 32kHz, 44.1kHz, 48kHz)	DAC	OFF
Power Down Control	ADC	OFF
High Pass Filter Operation	ADC	ON

TABLE II. Selectable Functions.

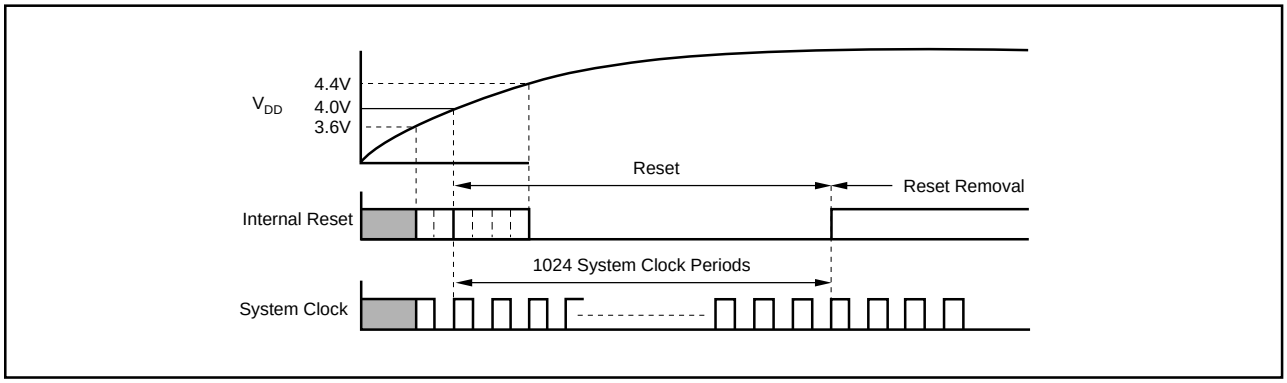


FIGURE 7. Internal Power-On Reset Timing.

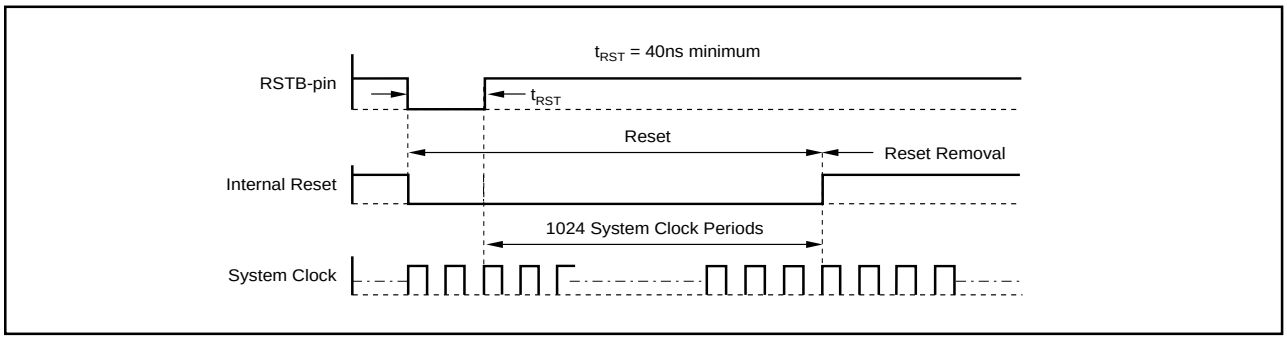


FIGURE 8. External Forced Reset Timing.

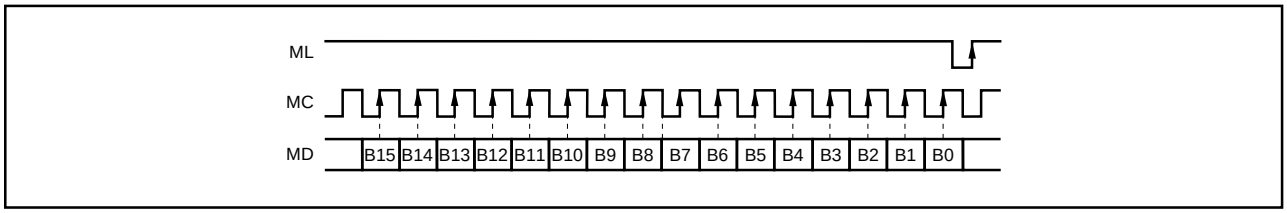


FIGURE 9. Control Data Input Format.

clocks (BCKIN) during one sample (LRCIN) period because of phase jitter on LRCIN, internal operation of the DAC will stop within $1/f_S$, and the analog output will be forced to bipolar zero ($V_{CC}/2$) until the system clock is re-synchronized to LRCIN. Internal operation of the ADC will also stop with $1/f_S$, and the digital output codes will be set to bipolar zero until re-synchronization occurs. If LRCIN is synchronized with 5 or less bit clocks to the system clock, operation will be normal.

Figures 10 and 11 illustrate the effects on the output when synchronization is lost. Before the outputs are forced to bipolar zero ($<1/f_S$ seconds), the outputs are not defined and some noise may occur. During the transitions between normal data and undefined states, the output has discontinuities, which will cause output noise.

OPERATIONAL CONTROL

PCM3000 can be controlled in a software mode with a three-wire serial interface on MC (Pin 25), MD (Pin 26), and ML (Pin 27). Table II indicates selectable functions, and Figures 9 and 12 illustrate control data input format and timing. PCM3001 only allows for control of data format.

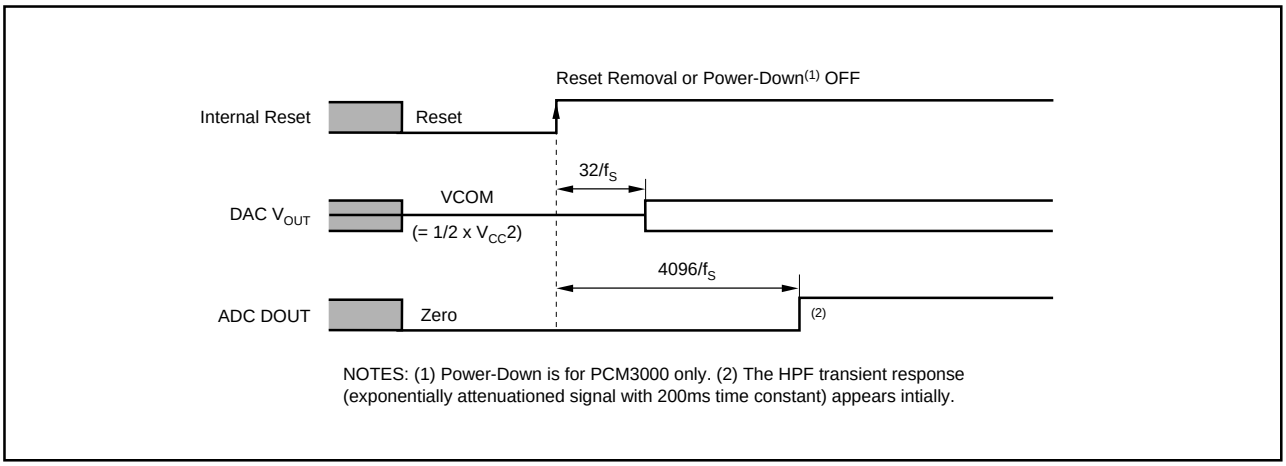


FIGURE 10. DAC Output and ADC Output for Reset and Power-Down.

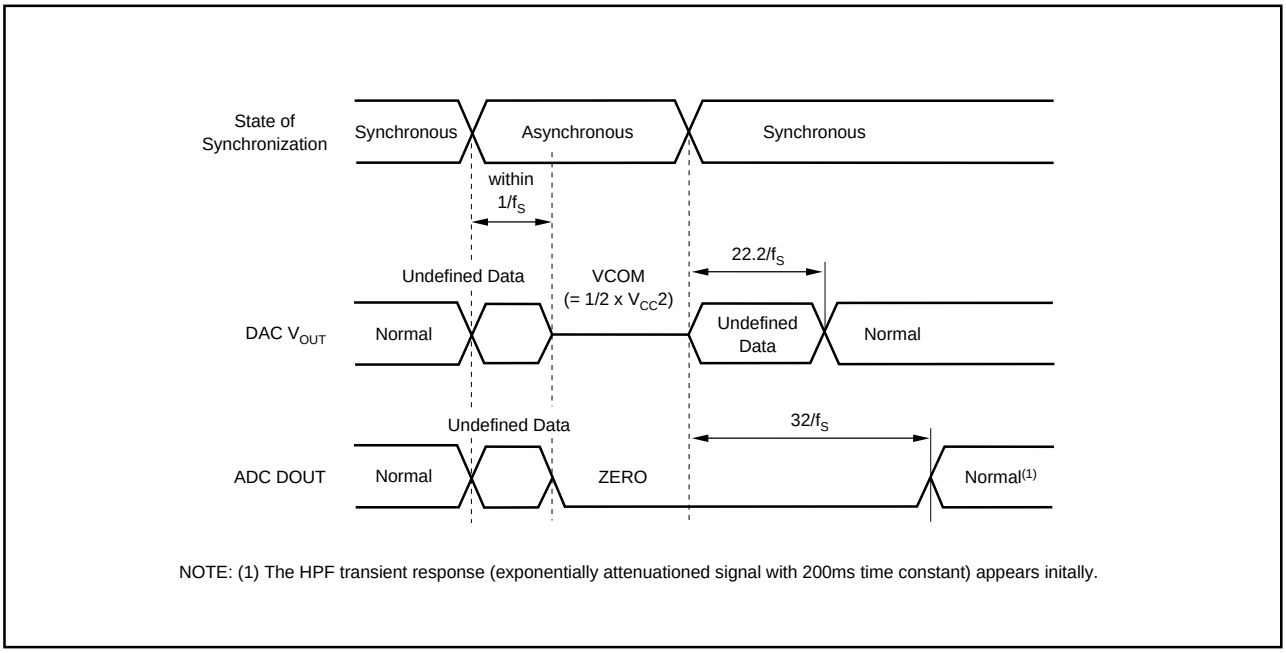
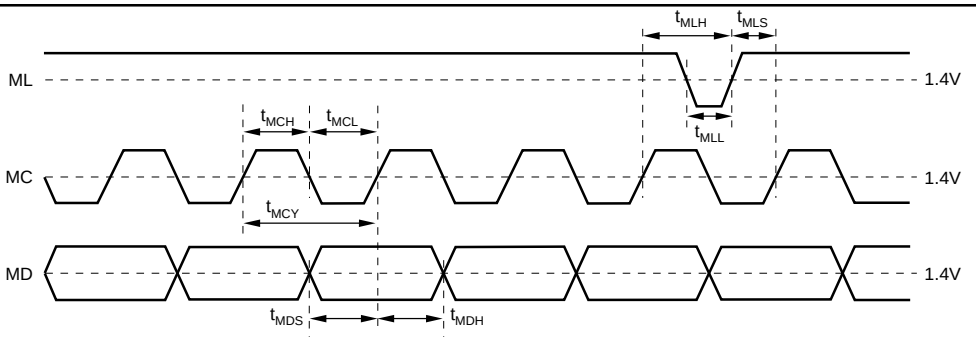


FIGURE 11. DAC Output and ADC Output When Synchronization is Lost.



MC Pulse Cycle Time	t_{MCY}	100ns (min)
MC PUlse Width Low	t_{MCL}	40ns (min)
MC Pulse Width High	t_{MCH}	40ns (min)
MD Set-up Time	t_{MDS}	40ns (min)
MD Hold Time	t_{MDH}	40ns (min)
ML Low Level Time	t_{MLL}	40ns + 1 SYSCLK (min)
ML Set-up Time	t_{MLS}	40ns (min)
ML Hold Time	t_{MLH}	40ns (min)

FIGURE 12. Control Data Input Timing.

MAPPING OF PROGRAM REGISTERS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 0	res	res	res	res	res	A1	A0	LDL	AL7	AL6	AL5	AL4	AL3	AL2	AL1	AL0
REGISTER 1	res	res	res	res	res	A1	A0	LDR	AR7	AR6	AR5	AR4	AR3	AR2	AR1	AR0
REGISTER 2	res	res	res	res	res	A1	A0	PDWN	BYPS	res	ATC	IZD	OUT	DM1	DM0	MUT
REGISTER 3	res	res	res	res	res	A1	A0	res	res	res	LOP	FMT2	FMT1	FMT0	LRP	res

PROGRAM REGISTER (PCM3000)

The software mode allows the user to control special functions. PCM3000's special functions are controlled using four program registers which are 16 bits long. There are four distinct registers, with bits 9 and 10 determining which register is in use. Table III describes the functions of the four registers.

REGISTER NAME	BIT NAME	DESCRIPTION
Register 0	A (1:0)	Register Address "00"
	res	Reserved, should be set to "0"
	LDL	DAC Attenuation Data Load Control for Lch
	AL (7:0)	Attenuation Data for Lch
Register 1	A (1:0)	Register Address "01"
	res	Reserved, should be set to "0"
	LDR	DAC Attenuation Data Load Control for Rch
	AR (7:0)	DAC Attenuation for Rch
Register 2	A (1:0)	Register Address "10"
	res	Reserved, should be set to "0"
	PDWN	ADC Power Down Control
	BYPS	ADC High-Pass Filter Operation Control
	ATC	DAC Attenuation Data Mode Control
	IZD	DAC Infinite Zero Detection Circuit Control
	OUT	DAC Output Enable Control
	DEM (1:0)	DAC De-emphasis Control
	MUT	Lch and Rch Soft Mute Control
Register 3	A (1:0)	Register Address "11"
	res	Reserved, should be set to "0"
	LOP	ADC/DAC Analog Loop-back Control
	FMT (2:0)	ADC/DAC Audio Data Format Selection
	LRP	ADC/DAC Polarity of LR-clock Selection

TABLE III. Functions of the Registers.

PROGRAM REGISTER 0

A (1:0): Bit 10, 9 Register Address

These bits define the address for REGISTER 0:

A1	A0	
0	0	Register 0

res: Bit 11 : 15 Reserved

These bits are reserved and should be set to "0".

LDL: Bit 8 DAC Attenuation Data Load Control for Left Channel

This bit is used to simultaneously set analog outputs of the left and right channels. The output level is controlled by AL (7:0) attenuation data when this bit is set to "1". When set to "0", the new attenuation data will be ignored, and the output level will remain at the previous attenuation level. The LDR bit in REGISTER 1 has the equivalent function as LDL. When either LDL or LDR is set to "1", the output level of the left and right channels are simultaneously controlled.

AL (7:0): Bit 7 :0 DAC Attenuation Data for Left Channel

AL7 and AL0 are MSB and LSB, respectively. The attenuation level (ATT) is given by:

ATT = 20 x $\log_{10}$ (ATT data/255) (dB)

AL (7:0)	ATTENUATION LEVEL
00h	–∞dB (Mute)
01h	–48.16dB
:	:
FEh	–0.07dB
FFh	0dB

PROGRAM REGISTER 1

A (1:0): Register Address

These bits define the address for REGISTER 1:

A1	A0	
0	1	Register 1

res: Bit 15 : 11 Reserved

These bits are reserved and should be set to “0”

LDR: Bit 8 DAC Attenuation Data Load Control for Right Channel

This bit is used to simultaneously set analog outputs of the left and right channels. The output level is controlled by AL (7:0) attenuation data when this bit is set to “1”. When set to “0”, the new attenuation data will be ignored, and the output level will remain at the previous attenuation level. The LDL bit in REGISTER 0 has the equivalent function as LDR. When either LDL or LDR is set to “1”, the output level of the left and right channels are simultaneously controlled.

AR (7:0): Bit 7 : 0 DAC Attenuation Data for Left Channel

AR7 and AR0 are MSB and LSB respectively. See REGISTER 0 for the attenuation formula.

PROGRAM REGISTER 2

A (1:0): Bit 10, 9 Register Address

These bits define the address for REGISTER 2:

A1	A0	
1	0	Register 2

res: Bit 15:11, 6 Reserved

These bits are reserved and should be set to “0”.

PDWN: Bit 8 ADC Power-Down Control

This bit places the ADC section in a power-down mode, forcing the output data to all zeroes. This has no effect on the DAC section.

PDWN	
0	Power Down Mode Disabled
1	Power Down Mode Enabled

BYPS: Bit 7 ADC High-Pass Filter Bypass Control

This bit determines enables or disables the high-pass filter for the ADC.

BYPS	
0	High-Pass Filter Enabled
1	High-Pass Filter Disabled (bypassed)

ATC: Bit 5 DAC Attenuation Channel Control

When set to “1”, the REGISTER 0 attenuation data can be used for both DAC channels. In this case, the REGISTER 1 attenuation data is ignored.

ATC	
0	Individual Channel Attenuation Data Control
1	Common Channel Attenuation Data Control

IZD: Bit 4 DAC Infinite Zero Detection Circuit Control

This bit enables the Infinite Zero Detection Circuit in PCM3000. When enabled, this circuit will disconnect the analog output amplifier from the delta-sigma DAC when the input is continuously zero for 65,536 consecutive cycles of BCKIN.

IZD	
0	Infinite Zero Detection Disabled
1	Infinite Zero Detection Enabled

OUT: Bit 3 DAC Output Enable Control

When set to “1”, the outputs are forced to $V_{CC}/2$ (bipolar zero). In this case, all registers in PCM3000 hold the present data. Therefore, when set to “0”, the outputs return to the previous programmed state.

OUT	
0	DAC Outputs Enabled (normal operation)
1	DAC Outputs Disabled (forced to BPZ)

DM (1:0):Bit 2,1 DAC De-emphasis Control

These bits select the de-emphasis mode as shown below:

DM1	DM0	
0	0	De-emphasis OFF
0	1	De-emphasis 48kHz ON
1	0	De-emphasis 44.1kHz ON
1	1	De-emphasis 32kHz ON

MUT: Bit 0 DAC Soft Mute Control

When set to “1”, both left and right-channel DAC outputs are muted at the same time. This muting is done by attenuating the data in the digital filter, so there is no audible click noise when soft mute is turned on.

MUT	
0	Mute Disable
1	Mute Enable

PROGRAM REGISTER 3

A (1:0): Bit 10, 9 Register Address

These bits define the address for REGISTER 3:

A1	A0	
1	1	Register 3

res: Bit 15:11, 8:6, 0 Reserved

These bits are reserved, and should be set to “0”.

FMT (2:0) Bit 4:2 Audio Data Format Select

These bits determine the input and output audio data formats.

FMT2	FMT1	FMT0	DAC Data Format	ADC Data Format
0	0	0	16-bit, MSB-first, Right-justified	16-bit, MSB-first, Left-justified
0	0	1	18-bit, MSB-first, Right-justified	18-bit, MSB-first, Left-justified
0	1	0	16-bit, MSB-first, Right-justified	16-bit, MSB-first, Right-justified
0	1	1	18-bit, MSB-first, Right-justified	18-bit, MSB-first, Right-justified
1	0	0	16-/18-bit, MSB-first, Left-justified	18-bit, MSB-first, Left-justified
1	0	1	16-/18-bit, MSB-first, I²S	18-bit, MSB-first, I²S
1	1	0	16-bit, MSB-first, DSP-frame	16-bit, MSB-first, DSP-frame
1	1	1	Reserved	

LOP: Bit 5 ADC to DAC Loop-back Control

When this bit is set to “1”, the ADC’s audio data is sent directly to the DAC. The data format will default to I²S. In Format 6 (DSP Frame), Loop-back is not supported.

LOP	
0	Loop-back Disable
1	Loop-back Enable

LRP: Bit 1 ADC and DAC Polarity of LR-clock Selection. Applies only to Formats 0 through 4.

LRP	
0	Left-Channel is “H”, Right-Channel is “L”.
1	Left-Channel is “L”, Right-Channel is “H”.

PCM3001 DATA FORMAT CONTROL

The input and output data formats are controlled by pins 27 (FMT0), 26 (FMT1), and 25 (FMT2). Setting these pins to the same values shown for the bit-mapped PCM3001 controls the data formats.

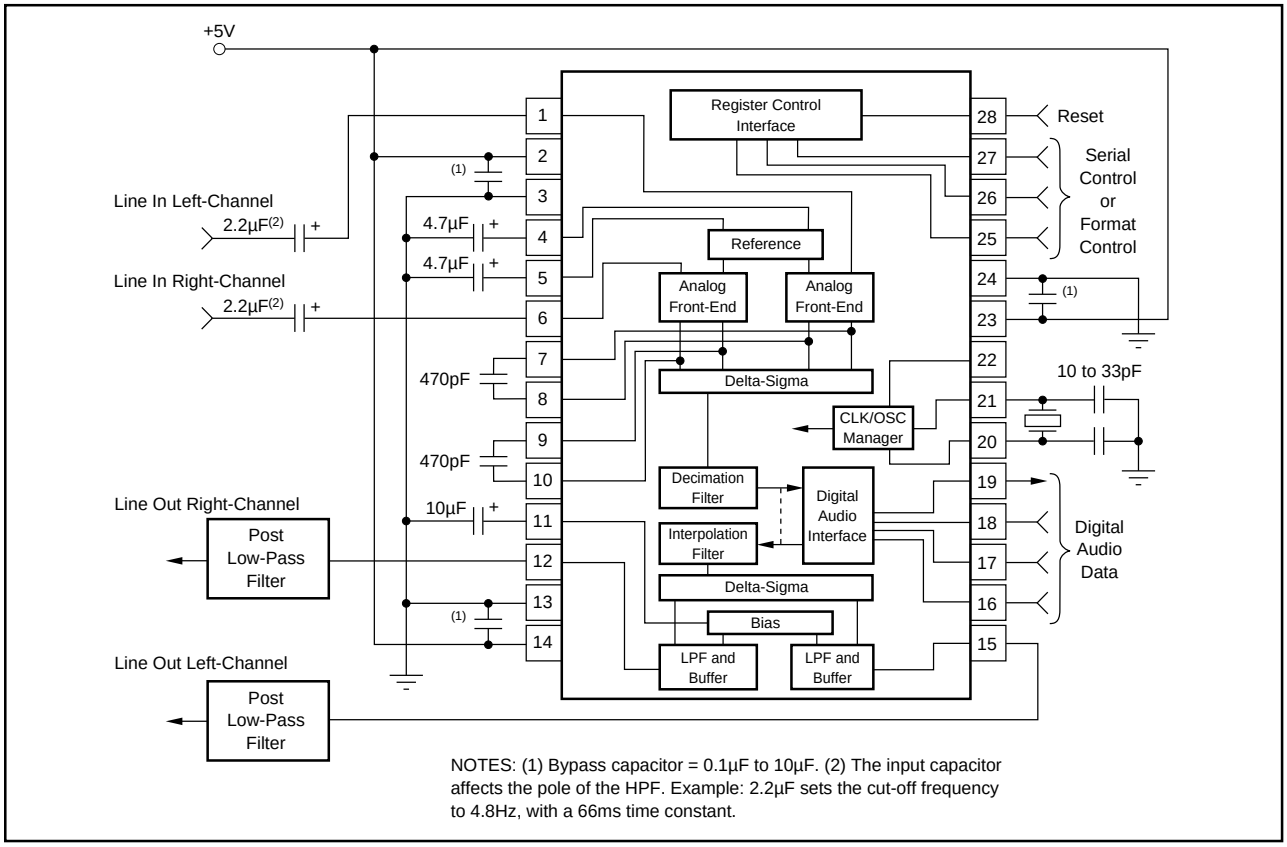


FIGURE 13. Typical Connection Diagram for PCM3000/3001.

APPLICATION AND LAYOUT CONSIDERATIONS

POWER SUPPLY BYPASSING

The digital and analog power supply lines to PCM3000/3001 should be bypassed to the corresponding ground pins with both 0.1µF ceramic and 10µF tantalum capacitors as close to the device pins as possible. Although PCM3000/3001 has three power supply lines to optimize dynamic performance, the use of one common power supply is generally recommended to avoid unexpected latch-up or pop noise due to power supply sequencing problems. If separate power supplies are used, back-to-back diodes are recommended to avoid latch-up problems.

GROUNDING

In order to optimize dynamic performance of PCM3000/3001, the analog and digital grounds are not internally connected. PCM3000/3001 performance is optimized with a single ground plane for all returns. It is recommended to tie all PCM3000/3001 ground pins with low impedance connections to the analog ground plane. PCM3000/3001 should reside entirely over this plane to avoid coupling high frequency digital switching noise into the analog ground plane.

VOLTAGE INPUT PINS

A tantalum capacitor, between 2.2µF and 10µF, is recommended as an AC-coupling capacitor at the inputs. Combined with the 15kΩ characteristic input impedance, a 2.2µF coupling capacitor will establish a 4.8Hz cutoff frequency for blocking DC. The input voltage range can be increased by adding a series resistor on the analog input line. This series resistor, when combined with the 15kΩ input impedance, creates a voltage divider and enables larger input ranges.

V_{REF} INPUTS

A 4.7µF to 10µF tantalum capacitor is recommended between V_{REF}L, V_{REF}R, and AGND1 to ensure low source impedance for the ADC's references. These capacitors should be located as close as possible to the reference pins to reduce dynamic errors on the ADC reference.

C_{IN}P AND C_{IN}N INPUTS

A 470pF to 1000pF film capacitor is recommended between C_{IN}PL and C_{IN}NL, C_{IN}PR, and C_{IN}NR to create an anti-alias filter, which will have an 170kHz to 80kHz cut-off frequency. These capacitors should be located as close as possible to the C_{IN}P and C_{IN}N pins to avoid introducing unexpected noise or dynamic errors into the delta-sigma modulator.

VCOM INPUTS

A 4.7µF to 10µF tantalum capacitor is recommended between VCOM and AGND2 to ensure low source impedance of the DAC output common. This capacitor should be located as close as possible to the VCOM pin to reduce dynamic errors on the DAC common.

SYSTEM CLOCK

The quality of the system clock can influence dynamic performance of both the ADC and DAC in the PCM3000/3001. The duty cycle, jitter, and threshold voltage at the system clock input pin must be carefully managed. When power is supplied to the part, the system clock, bit clock (BCKIN) and a word clock (LCRIN) should also be supplied simultaneously. Failure to supply the audio clocks will result in a power dissipation increase of up to three times normal dissipation and may degrade long term reliability if the maximum power dissipation limit is exceeded.

RSTB CONTROL

If the capacitance between V_{REF} and VCOM exceeds 4.7µF, an external reset control delay time circuit must be used.

THEORY OF OPERATION

ADC SECTION

The PCM3000/3001 ADC consists of a bandgap reference, a stereo single-to-differential converter, a fully differential 5th-order delta-sigma modulator, a decimation filter (including digital high pass), and a serial interface circuit. The Block Diagram in this data sheet illustrates the architecture of the ADC section, Figure 1 shows the single-to-differential converter, and Figure 14 illustrates the architecture of the 5th-order delta-sigma modulator and transfer functions.

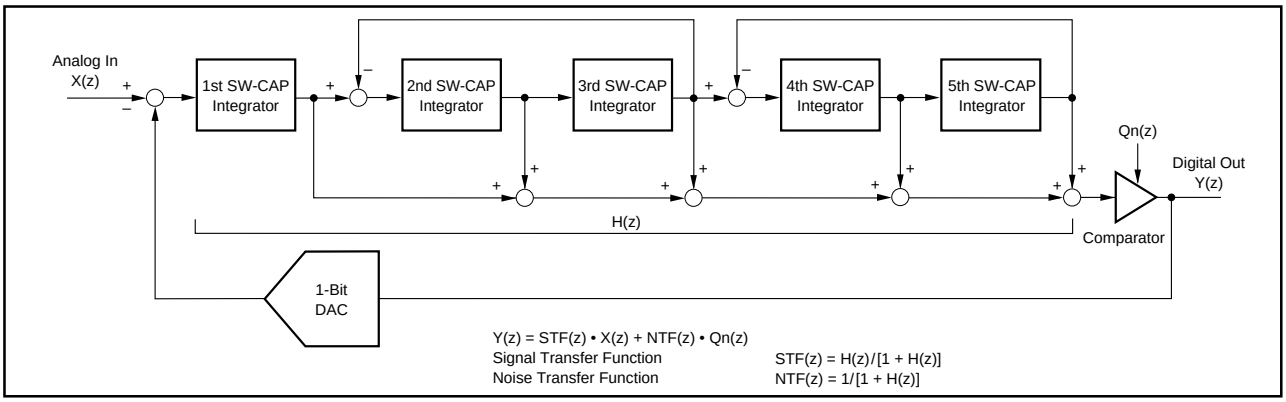


FIGURE 14. Simplified 5th-Order Delta-Sigma Modulator.

An internal high precision reference with two external capacitors provides all reference voltages which are required by the ADC, which defines the full scale range for the converter. The internal single-to-differential voltage converter saves the design, space and extra parts needed for external circuitry required by many delta-sigma converters. The internal full differential signal processing architecture provides a wide dynamic range and excellent power supply rejection performance.

The input signal is sampled at 64X oversampling rate, eliminating the need for a sample-and-hold circuit, and simplifying anti-alias filtering requirements. The 5th-order delta-sigma noise shaper consists of five integrators which use a switched-capacitor topology, a comparator and a feedback loop consisting of a one-bit DAC. The delta-sigma modulator shapes the quantization noise, shifting it out of the audio band in the frequency domain. The high order of the modulator enables it to randomize the modulator outputs, reducing idle tone levels.

The $64f_S$ one-bit data stream from the modulator is converted to $1f_S$ 18-bit data words by the decimation filter, which also acts as a low pass filter to remove the shaped quantization noise. The DC components are removed by a high pass filter function contained within the decimation filter.

THEORY OF OPERATION

DAC SECTION

The delta-sigma DAC section of PCM3000/3001 is based on a 5-level amplitude quantizer and a 3rd-order noise shaper. This section converts the oversampled input data to 5-level delta-sigma format. A block diagram of the 5-level delta-sigma modulator is shown in Figure 15. This 5-level delta-sigma modulator has the advantage of stability and clock jitter sensitivity over the typical one-bit (2 level) delta-sigma modulator.

The combined oversampling rate of the delta-sigma modulator and the internal 8X interpolation filter is $64f_S$ for a $256f_S$system clock. The theoretical quantization noise performance of the 5-level delta-sigma modulator is shown in Figure 16.

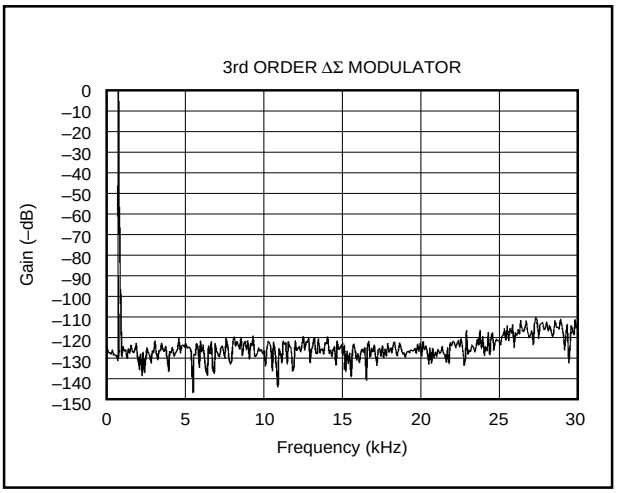


FIGURE 16. Quanitzation Noise Spectrum.

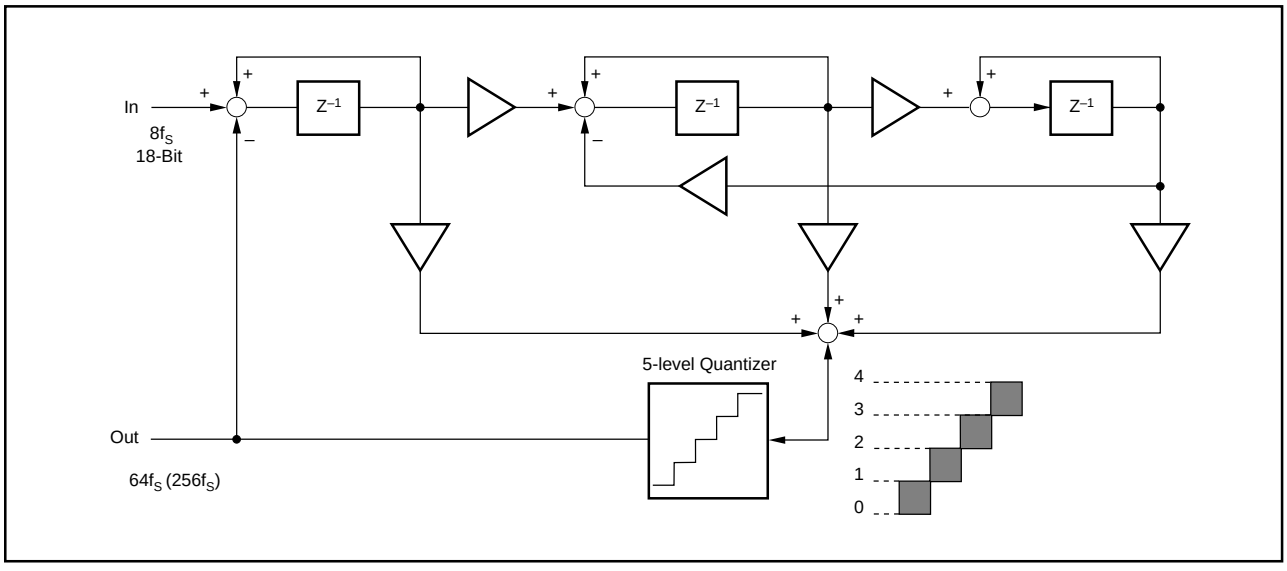


FIGURE 15. 5-Level ΔΣ Modulator Block Diagram.