

ISO808

Isolated 12-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 100kHz SAMPLING RATE
- 1500Vrms ISOLATION CONTINUOUS
- 10 μ S CONVERSION TIME
- 12-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

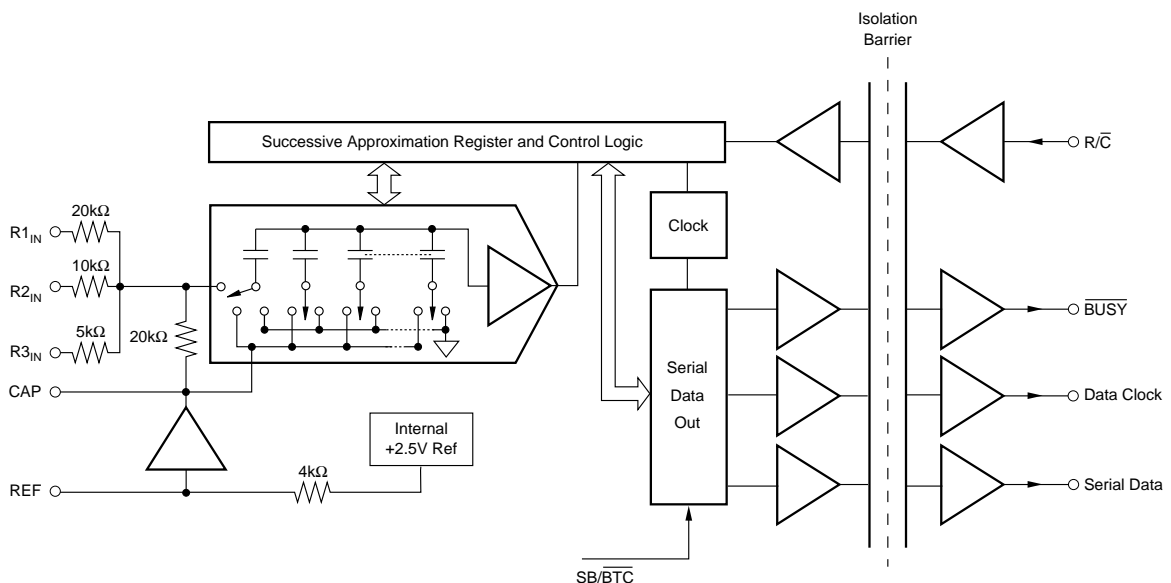
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

DESCRIPTION

The ISO808 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO808 contains a complete 12-bit capacitor based SAR, ADC with S/H, clock, reference, μ P interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including $\pm 10V$, $\pm 5V$, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of $-40^{\circ}C$ to $+85^{\circ}C$.



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SPECIFICATIONS

ELECTRICAL

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $f_S = 100\text{kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

PARAMETER	CONDITIONS	ISO808P			UNITS
		MIN	TYP	MAX	
ISOLATION PARAMETERS Rated Voltage, Continuous Partial Discharge, 100% Test ⁽⁸⁾ Creepage Distance (External) DIP = "P" Package Internal Isolation Distance Barrier Impedance Leakage Current ⁽⁹⁾	50Hz 1s, 5pC 240Vrms, 60Hz 240Vrms, 50Hz	1500 2500	16 0.10 >10 ¹³ 15	1.7 1.4	Vrms Vrms mm mm Ω pF μArms μArms
RESOLUTION				12	Bits
ANALOG INPUT Voltage Ranges Impedance Capacitance			$\pm 10\text{V}$, 0V to 5V, etc. (See Table I) See Table I 35		pF
THROUGHPUT SPEED Conversion Time Complete Cycle Throughput Rate	Acquire and Convert	100	5.7	8 10	μs μs kHz
DC ACCURACY Integral Linearity Error Differential Linearity Error No Missing Codes Transition Noise ⁽²⁾ Full Scale Error ^(3,4) Full Scale Error Drift Full Scale Error Drift Bipolar Zero Error ⁽³⁾ Bipolar Zero Error Drift Unipolar Zero Error ⁽³⁾ Unipolar Zero Error Drift Power Supply Sensitivity ($V_{\text{DIG}} = V_{\text{ANA}} = V_{\text{D}}$)	Ext. 2.5000V Ref Bipolar Ranges Bipolar Ranges Unipolar Ranges Unipolar Ranges $+4.75\text{V} < V_{\text{D}} < +5.25\text{V}$		Guaranteed 0.1 ± 7 ± 2 ± 2 ± 2	± 0.9 ± 0.9 ± 0.5 ± 10 ± 5 ± 0.5	LSB ⁽¹⁾ LSB LSB % ppm/ $^{\circ}\text{C}$ ppm/ $^{\circ}\text{C}$ mV ppm/ $^{\circ}\text{C}$ mV ppm/ $^{\circ}\text{C}$ LSB
AC ACCURACY Spurious-Free Dynamic Range Total Harmonic Distortion Signal-to-(Noise+Distortion) Signal-to-Noise Full-Power Bandwidth ⁽⁶⁾	$f_{\text{IN}} = 45\text{kHz} \pm 10\text{V}$ $f_{\text{IN}} = 45\text{kHz} \pm 10\text{V}$ $f_{\text{IN}} = 45\text{kHz} \pm 10\text{V}$ $f_{\text{IN}} = 45\text{kHz} \pm 10\text{V}$		90 -90 73 73 250		dB ⁽⁵⁾ dB dB dB kHz
SAMPLING DYNAMICS Aperture Delay Aperture Jitter Overvoltage Recovery ⁽⁷⁾			40 Sufficient to meet AC specs 150		ns ns ns
REFERENCE Internal Reference Voltage Internal Reference Source Current (Must use external buffer) External Reference Voltage Range for Specified Linearity External Reference Current Drain	No Load Ext. 2.5000V Ref	2.48 2.3	2.5 1 2.5	2.52 2.7 100	V μA V μA
DIGITAL INPUTS Logic Levels V_{IL} V_{IH} I_{IL} I_{IH}	$V_{\text{IL}} = 0\text{V}$ $V_{\text{IH}} = 5\text{V}$	-0.3 $V_{\text{D}} - 1.0$		1.0 $V_{\text{D}} + 0.3\text{V}$ ± 10 ± 10	V V μA μA
DIGITAL OUTPUTS Data Coding V_{OL} V_{OH}	$I_{\text{SINK}} = 1.6\text{mA}$ $I_{\text{SOURCE}} = 500\mu\text{A}$	Binary Two's Complement or Straight Binary +4		± 0.4	V V

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SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $f_S = 100\text{kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$, using internal reference and fixed resistors shown in Figure 3, unless otherwise specified.

PARAMETER	CONDITIONS	ISO808P			UNITS
		MIN	TYP	MAX	
POWER SUPPLIES					
Specified Performance	Must be $\leq V_{\text{ANA}}$				
V_{DIG1}		+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
V_{DIG2}		+4.75		+5.25	V
I_{DIG1}			4.2		mA
I_{ANA}		16		mA	
I_{DIG2}		10.8		mA	
Power Dissipation	$V_{\text{ANA}} = V_{\text{DIG}} = 5\text{V}$, $f_S = 100\text{kHz}$		175		mW
TEMPERATURE RANGE					
Specified Performance		-40		+85	$^{\circ}\text{C}$
Storage		-65		+150	$^{\circ}\text{C}$
Thermal Resistance, ϕ_{JA}			75		$^{\circ}\text{C}/\text{W}$
Plastic DIP					

NOTES: (1) LSB means Least Significant Bit. One LSB for the $\pm 10\text{V}$ input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of $\geq 5\text{pC}$. (9) Tested at 2500Vrms, 50Hz limit 10 μA .

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{\text{IN}}$	$\pm 25\text{V}$
$R2_{\text{IN}}$	$\pm 25\text{V}$
$R3_{\text{IN}}$	$\pm 25\text{V}$
CAP	$V_{\text{ANA}} + 0.3\text{V}$ to AGND2 -0.3V
REF	Indefinite Short to AGND, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND and AGND	$\pm 0.3\text{V}$
DGND, AGND, and GND _{ISO}	1563Vrms
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	-0.3V to $V_{\text{DIG}} + 0.3\text{V}$
Maximum Junction Temperature	+165 $^{\circ}\text{C}$
Internal Power Dissipation	700mW
Lead Temperature (soldering, 10s)	+300 $^{\circ}\text{C}$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
ISO808P	28-Pin Plastic DIP	215-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

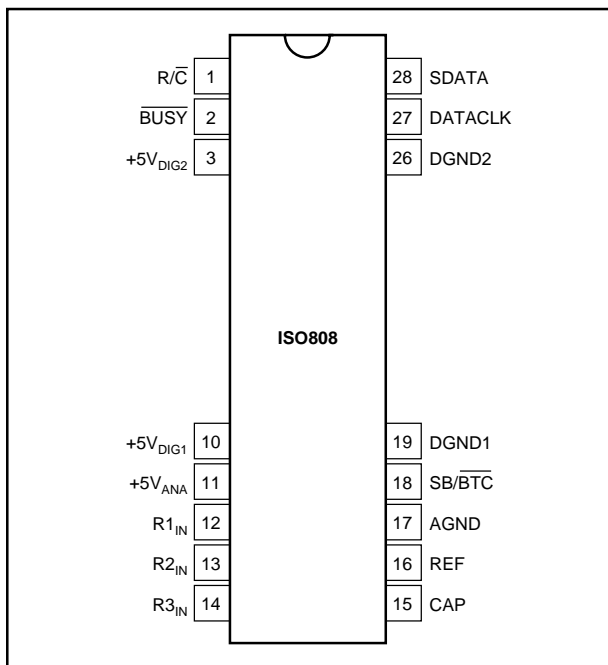
ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE ($^{\circ}\text{C}$)	PACKAGE
ISO808P	± 0.9	70	-40°C to $+85^{\circ}\text{C}$	28-Pin Plastic DIP

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	$\overline{R/C}$	I	Read/Convert. With \overline{BUSY} high, a falling edge on $\overline{R/C}$ initiates a new conversion.
2	\overline{BUSY}	O	At the start of conversion \overline{BUSY} goes LOW and stays LOW until conversion is complete.
3	+5V _{DIG2}		Isolated Digital Supply Volts.
10	+5V _{DIG1}		Digital Supply Volts.
11	+5V _{ANA}		Analog Supply Volts.
12	R1 _{IN}		Analog Input.
13	R2 _{IN}		Analog Input.
14	R3 _{IN}		Analog Input.
15	CAP		Reference Buffer Output. 2.2 μ F tantalum capacitor to ground.
16	REF		Reference Input/Output. 2.2 μ F tantalum capacitor to ground.
17	AGND		Analog Ground.
18	SB/ \overline{BTC}	I	Selects Straight Binary or Binary Two's Complement for output data format.
19	DGND1		Digital Ground.
26	DGND2		Isolated Ground.
27	DATACLK	O	Data Clock Output.
28	SDATA	O	Serial Output Synchronized to DATACLK.

TABLE I. Pin Assignments.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT R1 _{IN} VIA 200 Ω TO	CONNECT R2 _{IN} VIA 100 Ω TO	CONNECT R3 _{IN} TO	IMPEDANCE
$\pm 10V$	V _{IN}	AGND	CAP	22.9k Ω
$\pm 5V$	AGND	V _{IN}	CAP	13.3k Ω
± 3.33	V _{IN}	V _{IN}	CAP	10.7k Ω
0V to 10V	AGND	V _{IN}	AGND	13.3k Ω
0V to 5V	AGND	AGND	V _{IN}	10.0k Ω
0V to 4V	V _{IN}	AGND	V _{IN}	10.7k Ω

TABLE I. Input Range Connections. See Figure 3 for complete information.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t ₁	Convert Pulse Width	40		4500	ns
t ₂	\overline{BUSY} Delay		120		ns
t ₃	\overline{BUSY} LOW			8	μ s
t ₄	\overline{BUSY} Delay after End of Conversion		220		ns
t ₅	Aperture Delay		40		ns
t ₆	Conversion Time		5.7	8	μ s
t ₇	Acquisition Time			2	μ s
t ₆ + t ₇	Throughput Time		9	10	μ s
t ₈	$\overline{R/C}$ LOW to DATACLK Delay		450		ns
t ₉	DATACLK Period		440		ns
t ₁₀	Data Valid to DATACLK HIGH Delay	20	75		ns
t ₁₁	Data Valid after DATACLK LOW Delay	100	125		ns

TABLE II. Conversion and Data Timing. T_A = -40°C to +85°C.

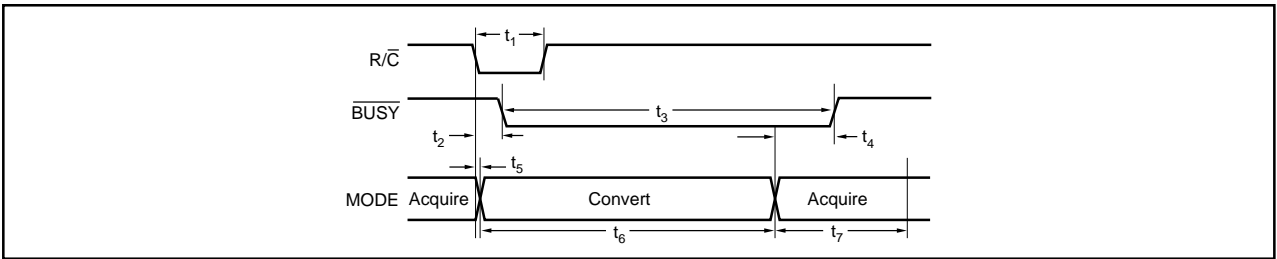


FIGURE 1. Basic Conversion Timing.

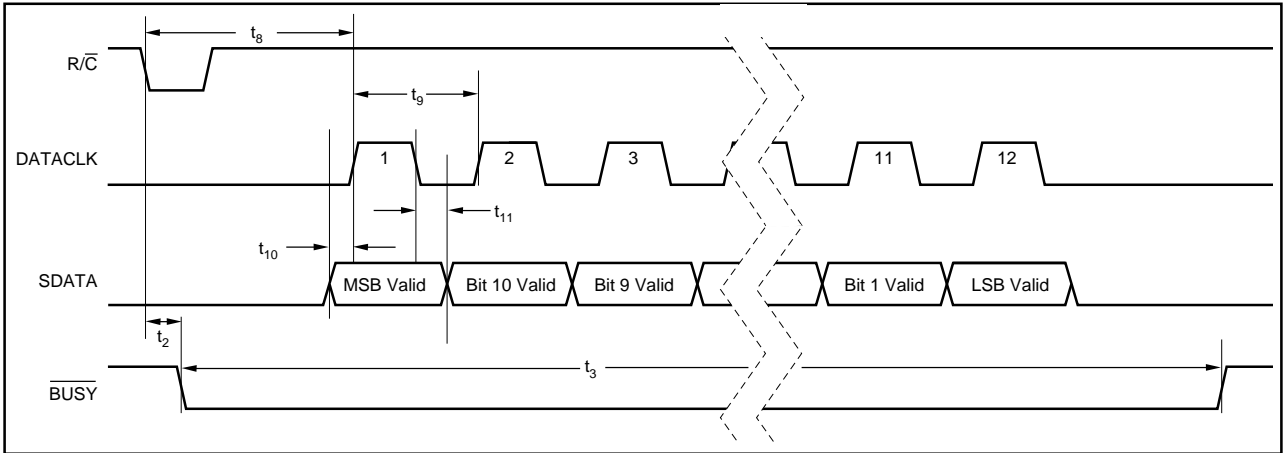


FIGURE 2. Serial Data Timing.

SPECIFIC FUNCTION	R/C	BUSY	DATACLK	SB/BTC	OPERATION
Initiate Conversion and Output Data	0	1	Output	X	Initiates Conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
	1 > 0	1	Output	X	Initiates Conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
Incorrect Conversions	0	0 > 1	X	X	R/C must be HIGH or a new conversion will be initiated without time for acquisition.
Selecting Output Format	X	X	X	0	Serial Data is output in Binary Two's Complement format.
	X	X	X	1	Serial Data is output in Straight Binary format.

TABLE III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/BTC LOW)		STRAIGHT BINARY (SB/BTC HIGH)	
							HEX BINARY CODE	CODE	HEX BINARY CODE	CODE
Full-Scale Range	±10	±5	±3.33V	0V to 5V	0V to 10V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	2.44mV	1.63mV	1.22mV	2.44mV	0.98mV				
+Full Scale (FS - 1LSB)	9.99512V	4.99756V	3.33171V	4.99878V	9.99756V	3.99902V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0V	0V	0V	2.5V	5V	2V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	-4.88mV	-2.44mV	-1.63mV	2.49878V	4.99756V	1.99902V	1111 1111 1111	FFF	0111 1111 1111	7FF
-Full Scale	-10V	-5V	-3.33333V	0V	0V	0V	1000 0000 0000	800	0000 0000 0000	000

TABLE IV. Output Codes and Ideal Input Voltages.

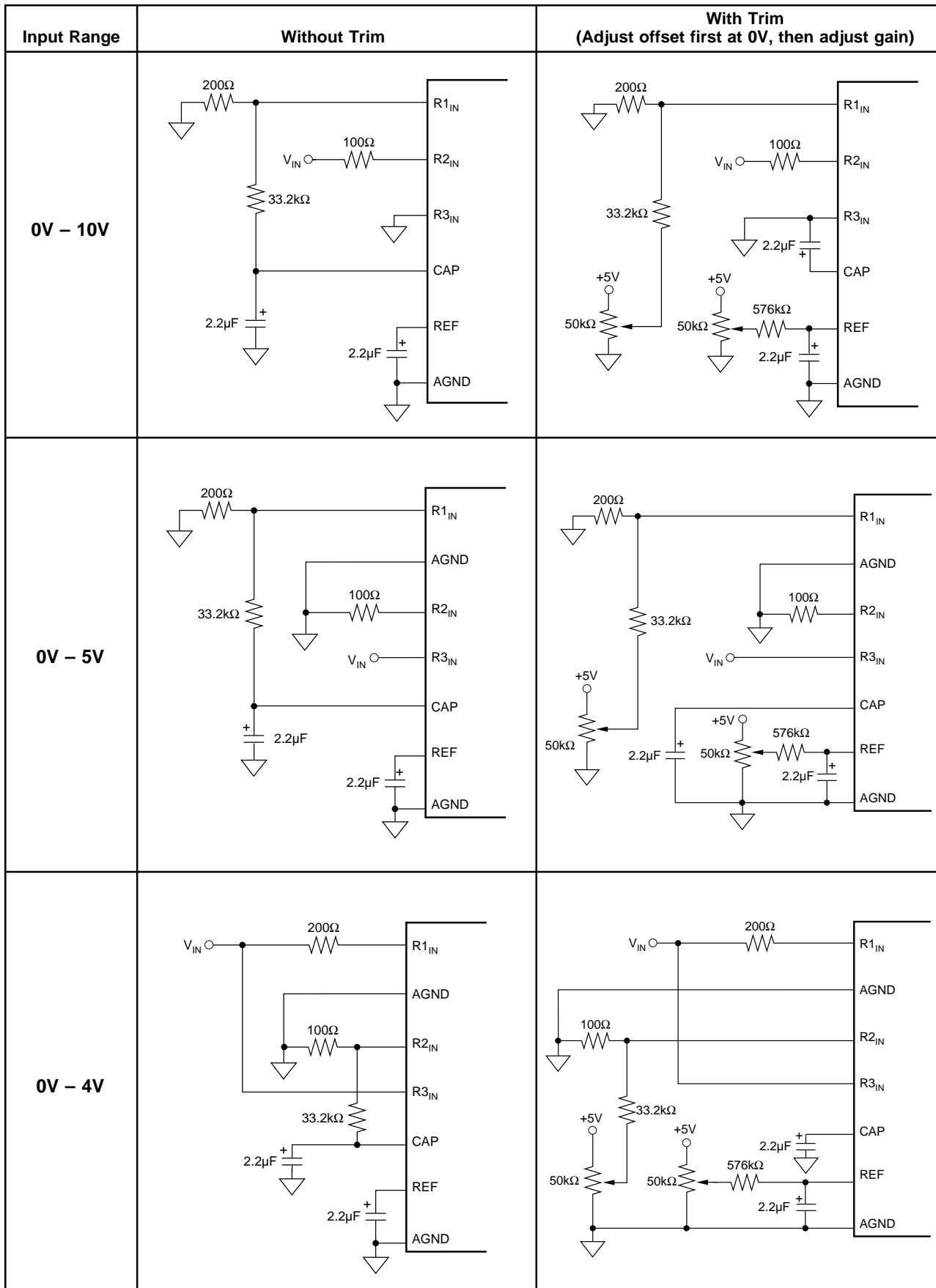


FIGURE 3a. Offset/Gain Circuits for Unipolar Input Ranges.

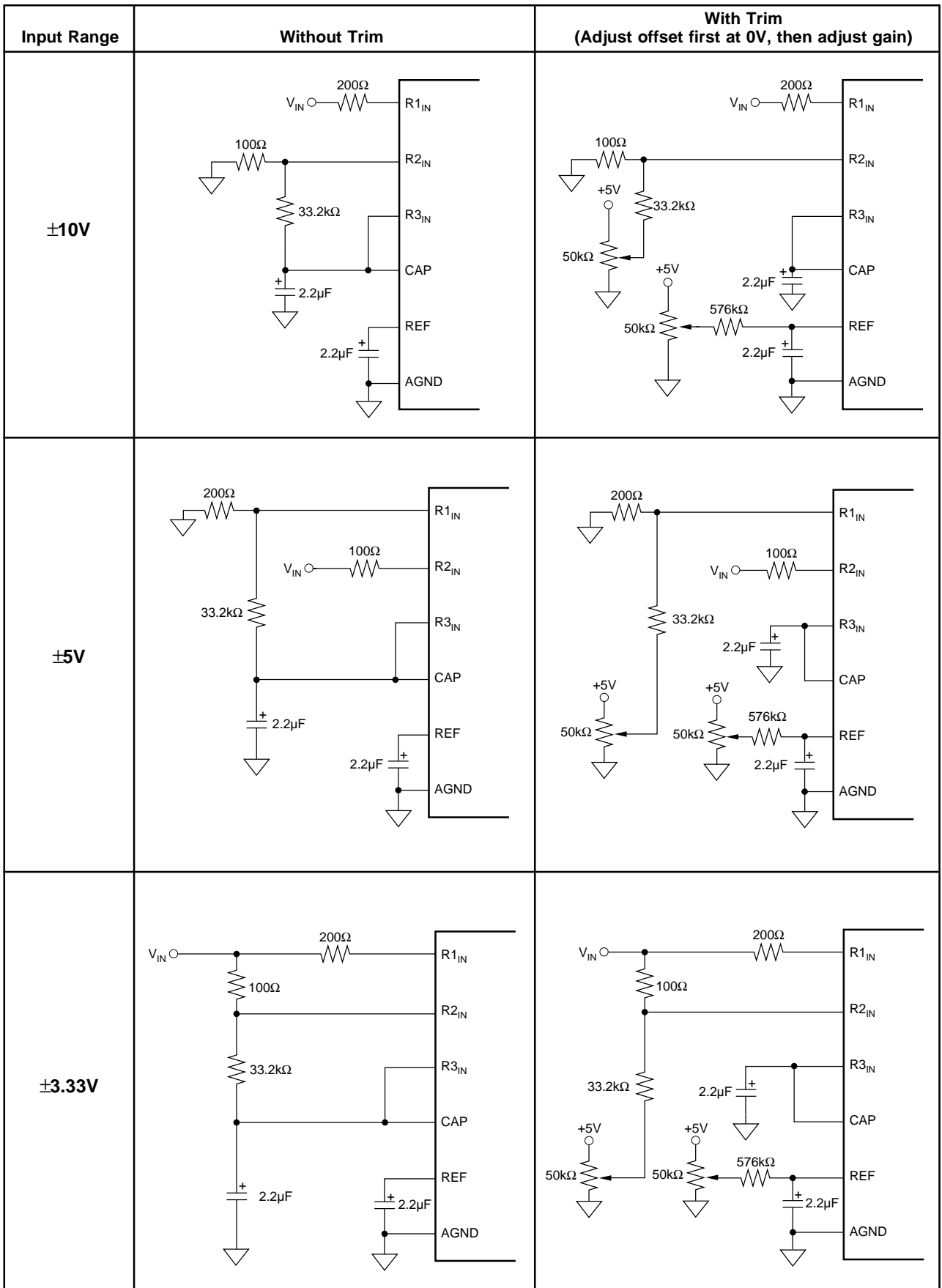


FIGURE 3b. Offset/Gain Circuits for Bipolar Input Ranges.