BURR - BROWN®

INA111

High Speed FET-Input INSTRUMENTATION AMPLIFIER

FEATURES

- FET INPUT: I_B = 20pA max
- HIGH SPEED: T_S = 4µs (G = 100, 0.01%)
- LOW OFFSET VOLTAGE: 500µV max
- LOW OFFSET VOLTAGE DRIFT: 5µV/°C max
- HIGH COMMON-MODE REJECTION: 106dB min
- 8-PIN PLASTIC DIP, SOL-16 SOIC

APPLICATIONS

- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

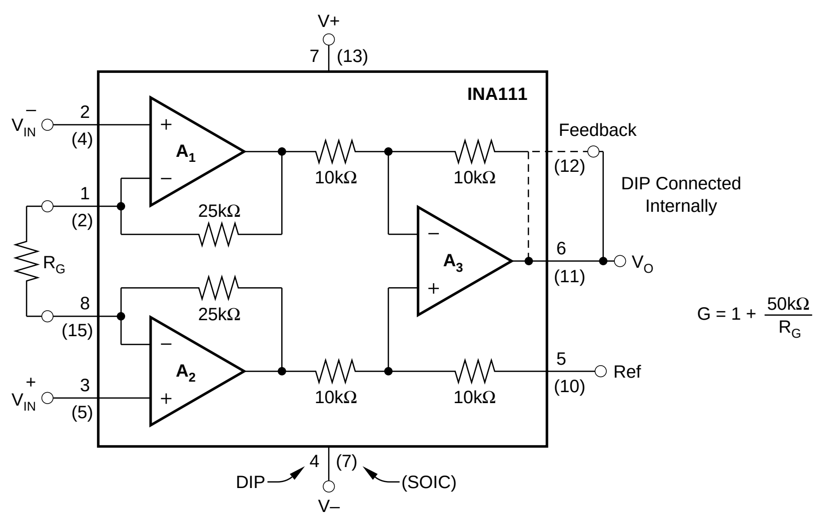
DESCRIPTION

The INA111 is a high speed, FET-input instrumentation amplifier offering excellent performance.

The INA111 uses a current-feedback topology providing extended bandwidth (2MHz at G = 10) and fast settling time (4µs to 0.01% at G = 100). A single external resistor sets any gain from 1 to over 1000.

Offset voltage and drift are laser trimmed for excellent DC accuracy. The INA111's FET inputs reduce input bias current to under 20pA, simplifying input filtering and limiting circuitry.

The INA111 is available in 8-pin plastic DIP, and SOL-16 surface-mount packages, specified for the –40°C to +85°C temperature range.



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SPECIFICATIONS

ELECTRICAL

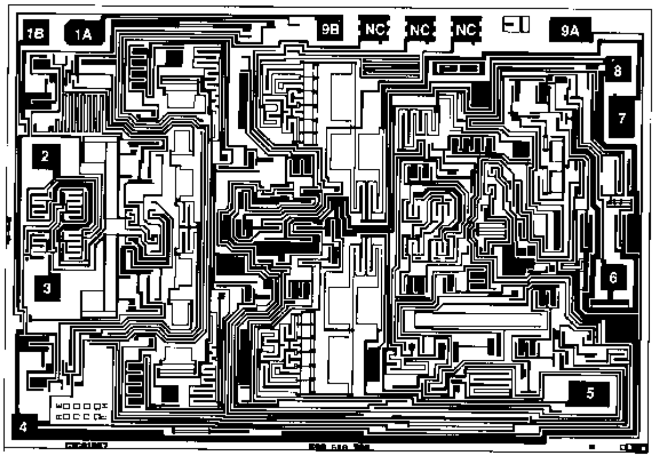
T_A = +25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

		INA111BP, BU			INA111AP, AU			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
Offset Voltage, RTI								
Initial	T_A = +25°C		±100 ± 500/G	±500 ± 2000/G		±200 ± 500/G	±1000 ± 5000/G	µV
vs Temperature	T_A = T_{MIN} to T_{MAX}		±2 ± 10/G	±5 ± 100/G		±2 ± 20/G	±10 ± 100/G	µV/°C
vs Power Supply	V_S = ±6V to ±18V		2 +10/G	30 + 100/G		*	*	µV/V
Impedance, Differential			10^{12} || 6			*		Ω || pF
Common-Mode			10^{12} || 3			*		Ω || pF
Input Common-Mode Range	V_{DIFF} = 0V	±10	±12		*	*		V
Common-Mode Rejection	V_{CM} = ±10V, ΔR_S = 1kΩ							
	G = 1	80	90		75	*		dB
	G = 10	96	110		90	*		dB
	G = 100	106	115		100	*		dB
	G = 1000	106	115		100	*		dB
BIAS CURRENT			±2	±20		*	*	pA
OFFSET CURRENT			±0.1	±10		*	*	pA
NOISE VOLTAGE, RTI	G = 1000, R_S = 0Ω							
f = 100Hz			13			*		nV/√Hz
f = 1kHz			10			*		nV/√Hz
f = 10kHz			10			*		nV/√Hz
f_B = 0.1Hz to 10Hz			1			*		µVp-p
Noise Current								
f = 10kHz			0.8			*		fA/√Hz
GAIN								
Gain Equation			1 + (50kΩ/R_G)			*		V/V
Range of Gain		1		10000	*		*	V/V
Gain Error	G = 1, R_L = 10kΩ		±0.01	±0.02		*	0.05	%
	G = 10, R_L = 10kΩ		±0.1	±0.5		*	*	%
	G = 100, R_L = 10kΩ		±0.15	±0.5		*	±0.7	%
	G = 1000, R_L = 10kΩ		±0.25	±1		*	±2	%
Gain vs Temperature	G = 1		±1	±10		*	*	ppm/°C
50kΩ Resistance(1)			±25	±100		*	*	ppm/°C
Nonlinearity	G = 1		±0.0005	±0.005		*	*	% of FSR
	G = 10		±0.001	±0.005		*	±0.01	% of FSR
	G = 100		±0.001	±0.005		*	±0.01	% of FSR
	G = 1000		±0.005	±0.02		*	±0.04	% of FSR
OUTPUT								
Voltage	I_O = 5mA, T_{MIN} to T_{MAX}	±11	±12.7		*	*		V
Load Capacitance Stability			1000			*		pF
Short Circuit Current			+30/–25			*		mA
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 1		2			*		MHz
	G = 10		2			*		MHz
	G = 100		450			*		kHz
	G = 1000		50			*		kHz
Slew Rate	V_O = ±10V, G = 2 to 100		17			*		V/µs
Settling Time, 0.01%	G = 1		2			*		µs
	G = 10		2			*		µs
	G = 100		4			*		µs
	G = 1000		30			*		µs
Overload Recovery	50% Overdrive		1			*		µs
POWER SUPPLY								
Voltage Range		±6	±15	±18	*	*	*	V
Current	V_{IN} = 0V		±3.3	±4.5		*	*	mA
TEMPERATURE RANGE								
Specification		–40		85	*		*	°C
Operating	Plastic P, U	–40		125	*		*	°C
θ_{JA}	Plastic P, U		100			*		°C/W

* Specification same as INA111BP.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.

DICE INFORMATION



INA111 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1A, 1B	R_G	6	V_O
2	V^-_{IN}	7	Feedback
3	V^+_{IN}	8	V+
4	V–	9A, 9B	R_G
5	Ref		

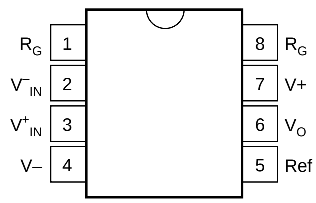
Pads 1A and 1B must be connected. Pads 9A and 9B must be connected.
NC = No Connection.
Substrate Bias: Internally connected to V– power supply.

MECHANICAL INFORMATION

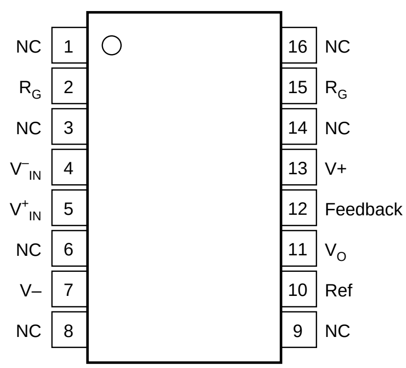
	MILS (0.001")	MILLIMETERS
Die Size	129 x 90 ±5	3.28 x 2.29 ±0.13
Die Thickness	20 ±3	0.51 ±0.08
Min. Pad Size	4 x 4	0.10 x 0.10
Backing		Gold

PIN CONFIGURATIONS

Top View DIP



Top View SOL-16 Surface Mount



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage Range	(V–) –0.7V to (V+) +15V
Output Short-Circuit (to ground)	Continuous
Operating Temperature	–40°C to +125°C
Storage Temperature	–40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
INA111AP	8-Pin Plastic DIP	–40°C to +85°C
INA111BP	8-Pin Plastic DIP	–40°C to +85°C
INA111AU	SOL-16 Surface-Mount	–40°C to +85°C
INA111BU	SOL-16 Surface-Mount	–40°C to +85°C

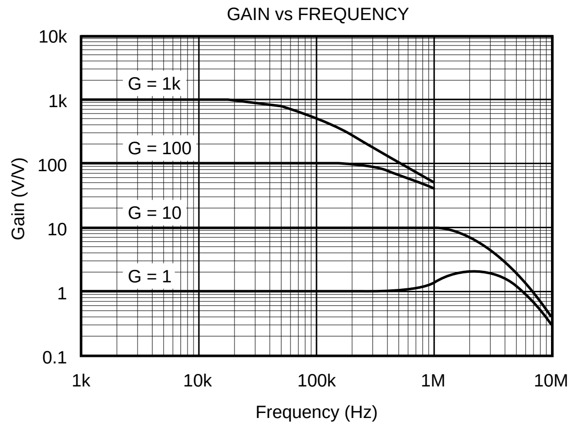
PACKAGE INFORMATION

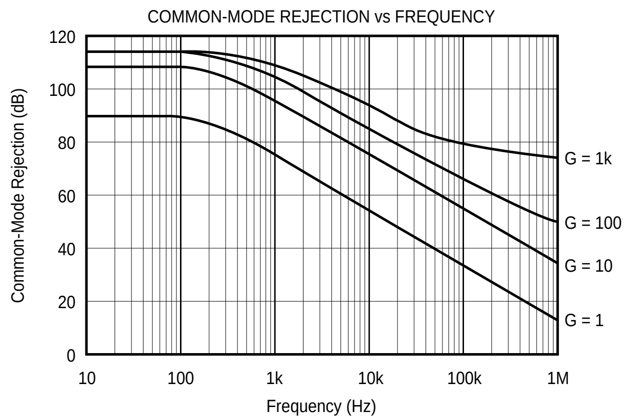
MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
INA111AP	8-Pin Plastic DIP	006
INA111BP	8-Pin Plastic DIP	006
INA111AU	16-Pin Surface Mount	211
INA111BU	16-Pin Surface Mount	211

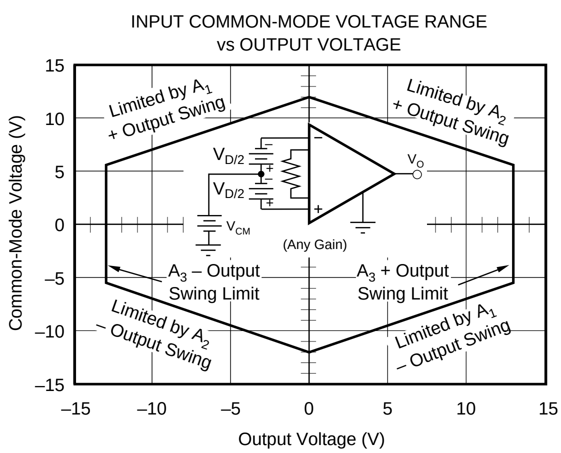
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

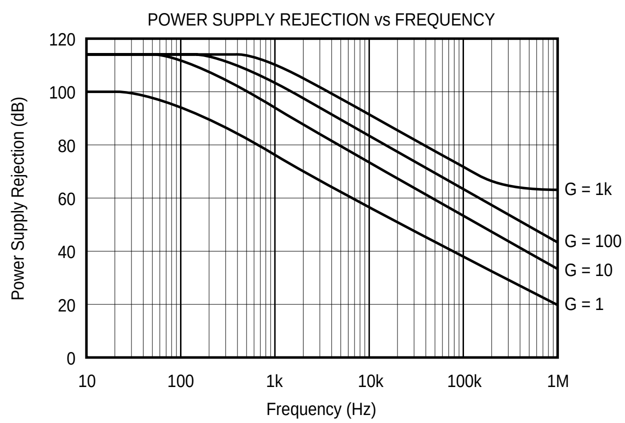
TYPICAL PERFORMANCE CURVES

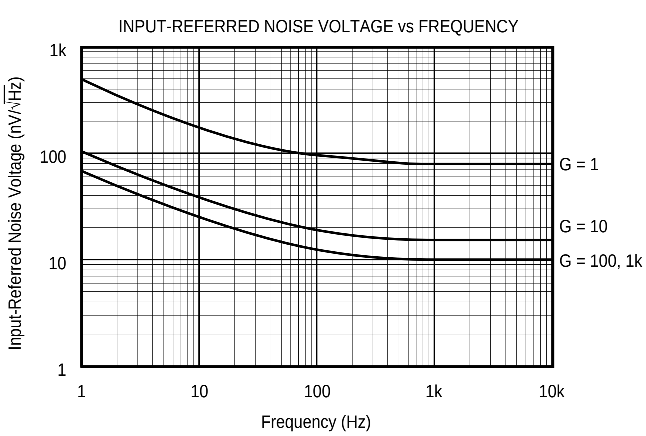
$T_A = +25°C$, $V_S = ±15V$ unless otherwise noted.

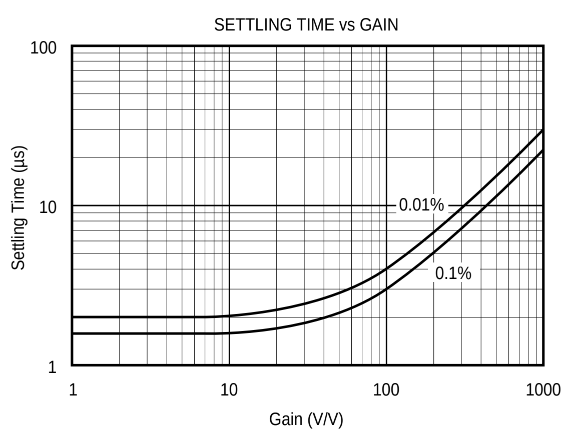






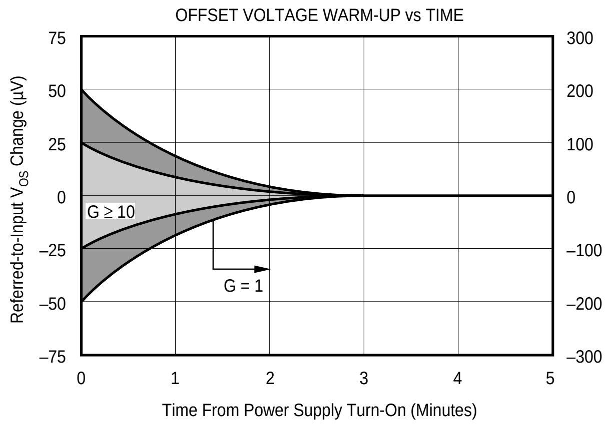


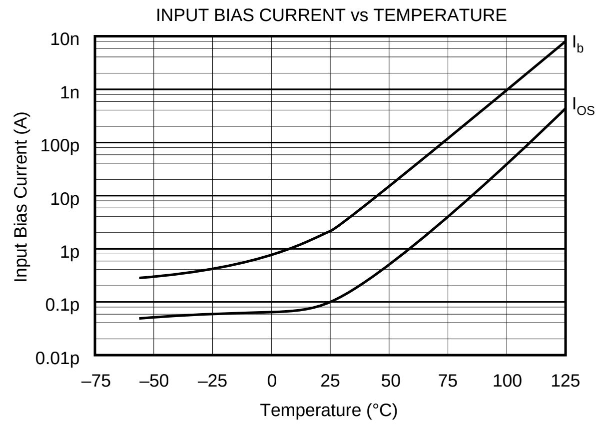


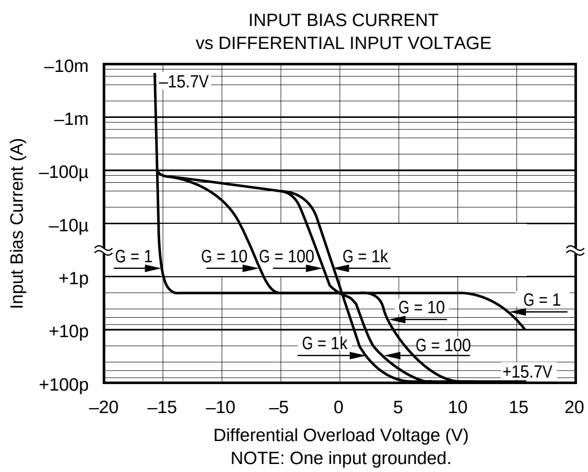


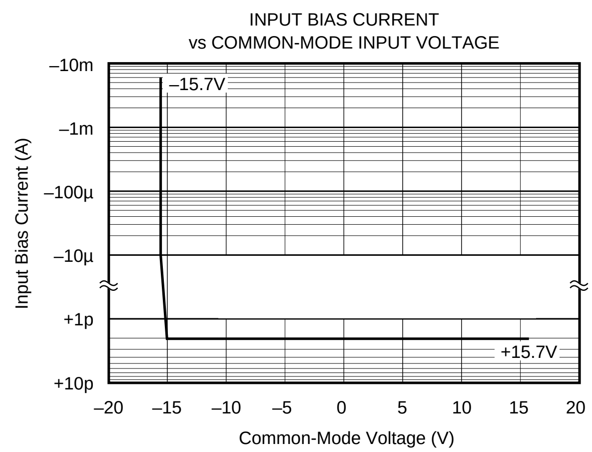
TYPICAL PERFORMANCE CURVES (CONT)

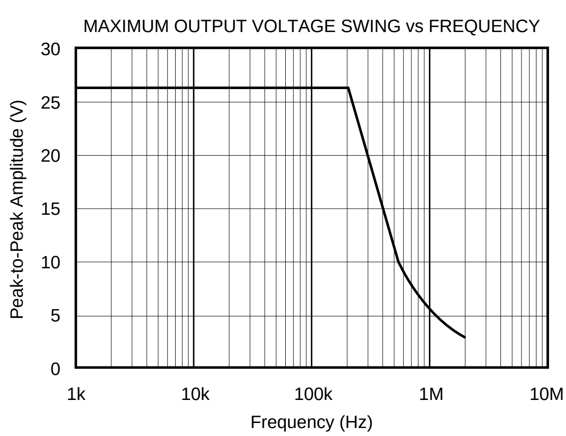
$T_A = +25°C$, $V_S = ±15V$ unless otherwise noted.

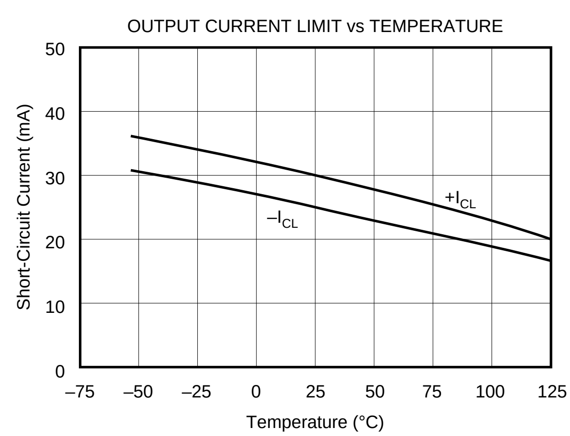








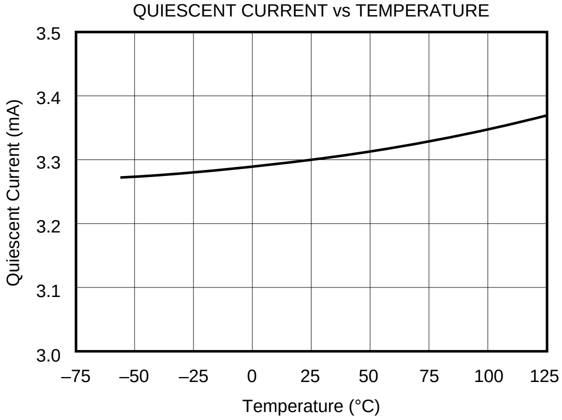




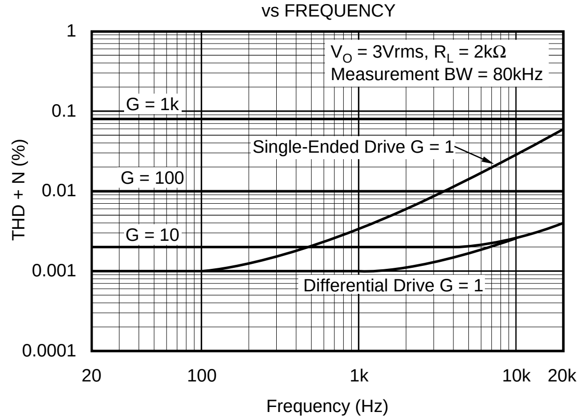
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

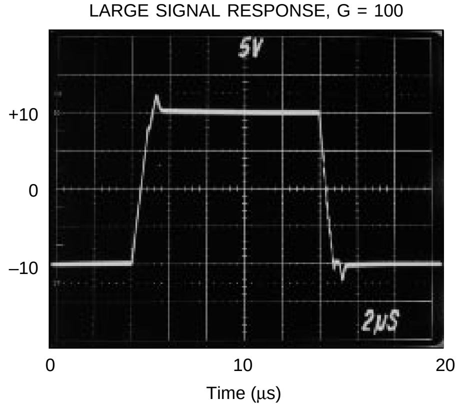
QUIESCENT CURRENT vs TEMPERATURE



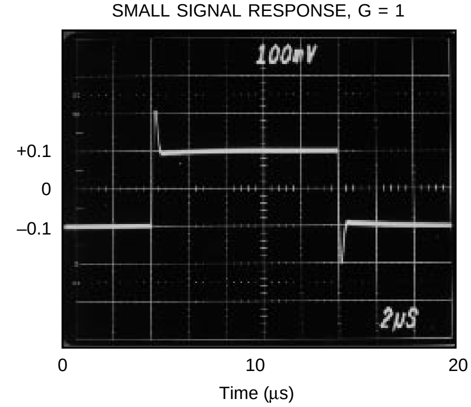
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



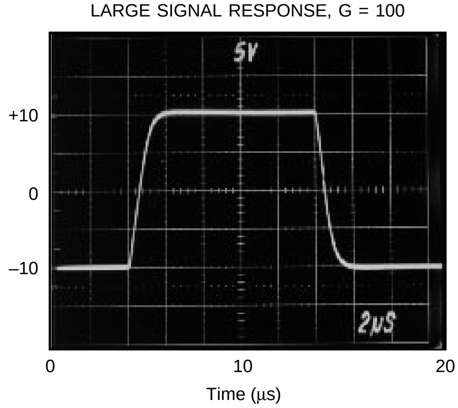
LARGE SIGNAL RESPONSE, G = 100



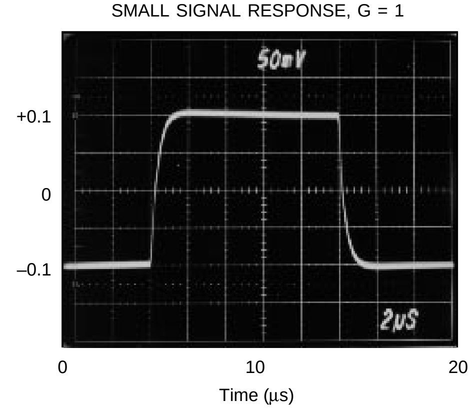
SMALL SIGNAL RESPONSE, G = 1



LARGE SIGNAL RESPONSE, G = 100



SMALL SIGNAL RESPONSE, G = 1



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA111. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 2Ω in series with the Ref pin will cause a typical device with 90dB CMR to degrade to approximately 80dB CMR (G = 1).

SETTING THE GAIN

Gain of the INA111 is set by connecting a single external resistor, R_G:

$$G = 1 + \frac{50k\Omega}{R_G} \qquad (1)$$

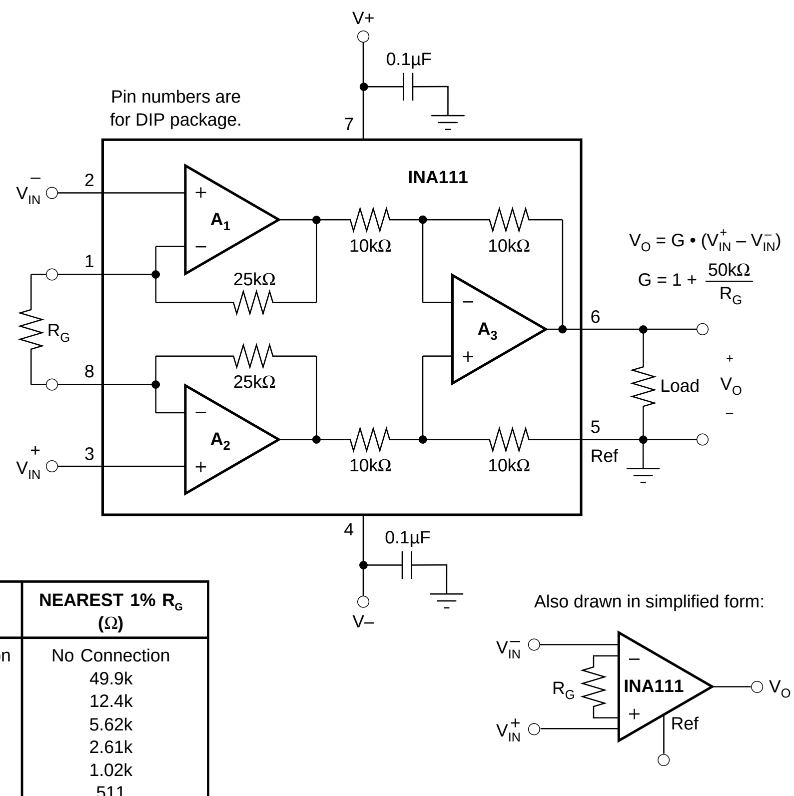
Commonly used gains and resistor values are shown in Figure 1.

The 50kΩ term in equation 1 comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA111.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

DYNAMIC PERFORMANCE

The typical performance curve "Gain vs Frequency" shows that the INA111 achieves wide bandwidth over a wide range of gain. This is due to the current-feedback topology of the INA111. Settling time also remains excellent over wide gains.



DESIRED GAIN	R_G (Ω)	NEAREST 1% R_G (Ω)
1	No Connection	No Connection
2	50.00k	49.9k
5	12.50k	12.4k
10	5.556k	5.62k
20	2.632k	2.61k
50	1.02k	1.02k
100	505.1	511
200	251.3	249
500	100.2	100
1000	50.05	49.9
2000	25.01	24.9
5000	10.00	10
10000	5.001	4.99

FIGURE 1. Basic Connections

The INA111 exhibits approximately 6dB rise in gain at 2MHz in unity gain. This is a result of its current-feedback topology and is not an indication of instability. Unlike an op amp with poor phase margin, the rise in response is a predictable +6dB/octave due to a response zero. A simple pole at 700kHz or lower will produce a flat passband response (see Input Filtering).

The INA111 provides excellent rejection of high frequency common-mode signals. The typical performance curve, "Common-Mode Rejection vs Frequency" shows this behavior. If the inputs are not properly balanced, however, common-mode signals can be converted to differential signals. Run the V_{IN}^+ and V_{IN}^- connections directly adjacent each other, from the source signal all the way to the input pins. If possible use a ground plane under both input traces. Avoid running other potentially noisy lines near the inputs.

NOISE AND ACCURACY PERFORMANCE

The INA111's FET input circuitry provides low input bias current and high speed. It achieves lower noise and higher accuracy with high impedance sources. With source impedances of 2kΩ to 50kΩ the INA114 may provide lower offset voltage and drift. For very low source impedance (≤1kΩ), the INA103 may provide improved accuracy and lower noise.

OFFSET TRIMMING

The INA111 is laser trimmed for low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. The op amp shown maintains low output impedance at high frequency. Trim circuits with higher source impedance should be buffered with an op amp follower circuit to assure low impedance on the Ref pin.

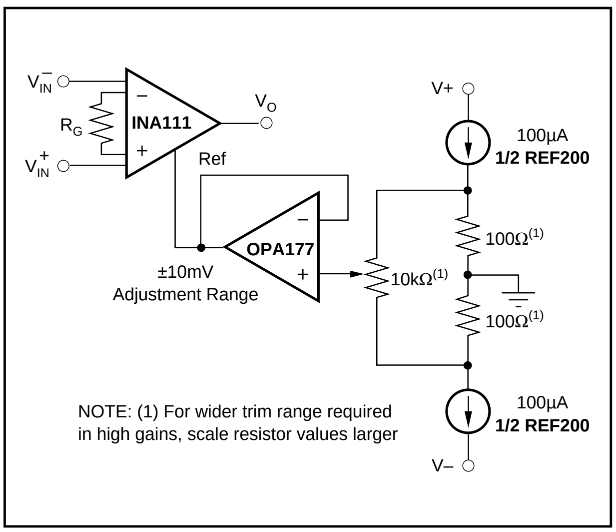


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA111 is extremely high—approximately $10^{12}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than 10pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA111 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA111 and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

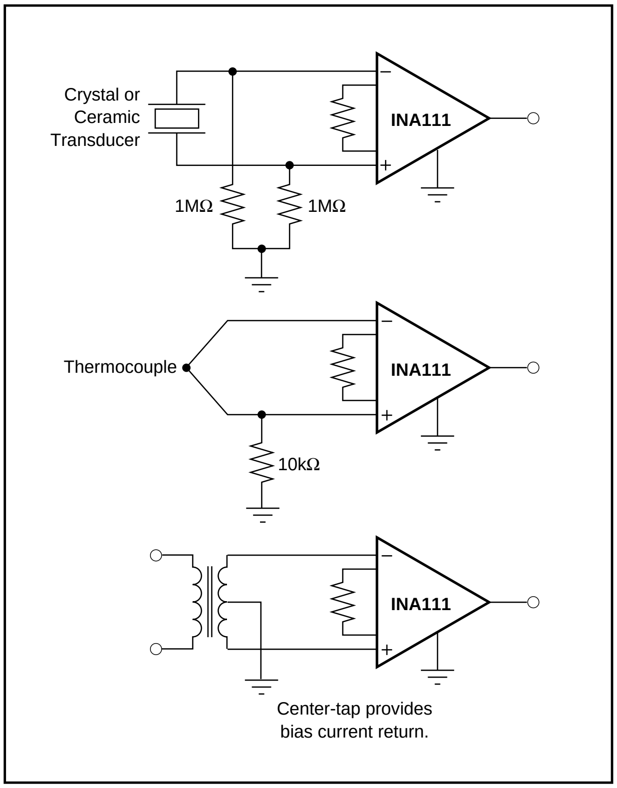


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA111 is approximately ±12V (or 3V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, A_1 and A_2. The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage".

A combination of common-mode and differential input voltage can cause the output of A_1 or A_2 to saturate. Figure 4 shows the output voltage swing of A_1 and A_2 expressed in terms of a common-mode and differential input voltages. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA111 in a lower gain (see performance curve “Input Common-Mode Voltage Range vs Output Voltage”). If necessary, add gain after the INA111 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, consider an input voltage of +14V on one input and +15V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA111 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

Inputs of the INA111 are protected for input voltages from 0.7V below the negative supply to 15V above the positive power supply voltages. If the input current is limited to less than 1mA, clamp diodes are not required; internal junctions will clamp the input voltage to safe levels. If the input source can supply more than 1mA, use external clamp diodes as shown in Figure 5. The source current can be limited with series resistors R_1 and R_2 as shown. Resistor values greater than 10kΩ will contribute noise to the circuit.

A diode formed with a 2N4117A transistor as shown in Figure 5 assures low leakage. Common signal diodes such as the 1N4148 may have leakage currents far greater than the input bias current of the INA111 and are usually sensitive to light.

INPUT FILTERING

The INA111’s FET input allows use of an R/C input filter without creating large offsets due to input bias current. Figure 6 shows proper implementation of this input filter to preserve the INA111’s excellent high frequency common-mode rejection. Mismatch of the common-mode input capacitance (C_1 and C_2), either from stray capacitance or

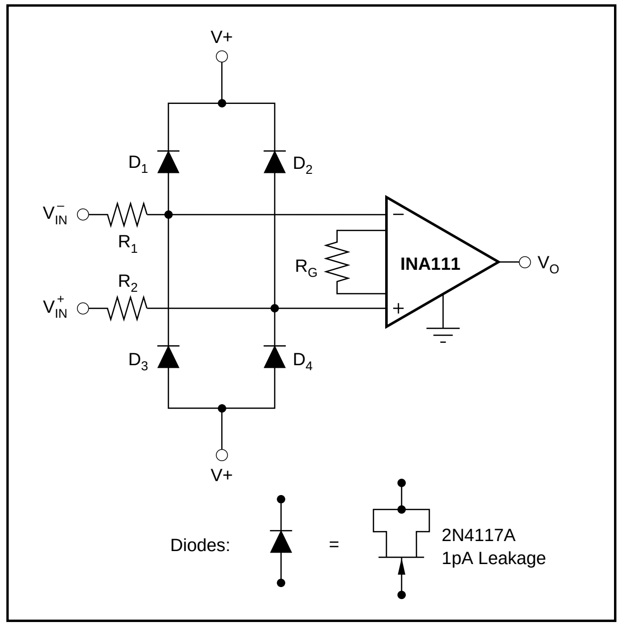


FIGURE 5. Input Protection Voltage Clamp.

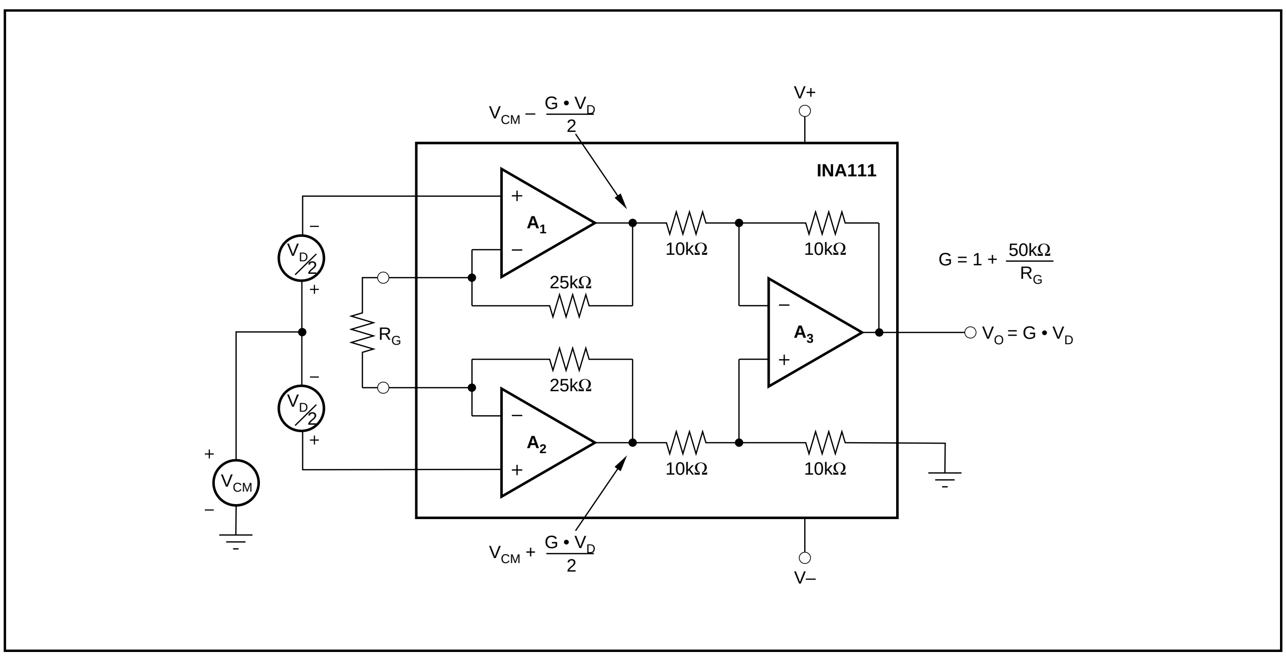


FIGURE 4. Voltage Swing of A_1 and A_2.

mismatched values, causes a high frequency common-mode signal to be converted to a differential signal. This degrades common-mode rejection. The differential input capacitor, C_3, reduces the bandwidth and mitigates the effects of mismatch in C_1 and C_2. Make C_3 much larger than C_1 and C_2. If properly matched, C_1 and C_2 also improve CMR.

OUTPUT VOLTAGE SENSE (SOL-16 Package Only)

The surface-mount version of the INA111 has a separate output sense feedback connection (pin 12). Pin 12 must be connected, usually to the output terminal, pin 11, for proper operation. (This connection is made internally on the DIP version of the INA111.)

The output feedback connection can be used to sense the output voltage directly at the load for best accuracy. Figure 8 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through C_1.

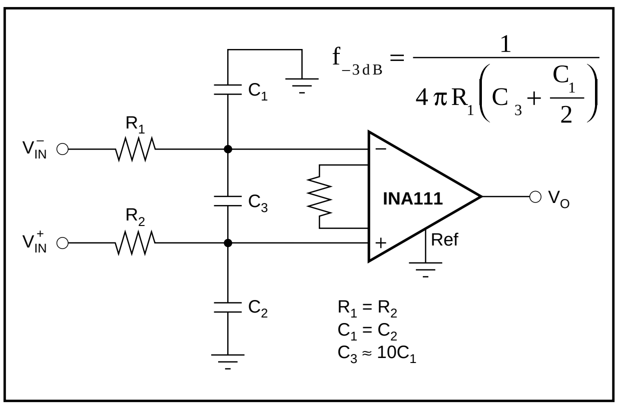


FIGURE 6. Input Low-Pass Filter.

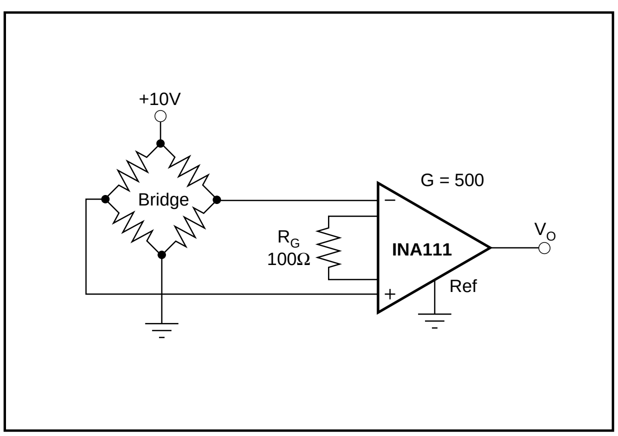


FIGURE 7. Bridge Transducer Amplifier.

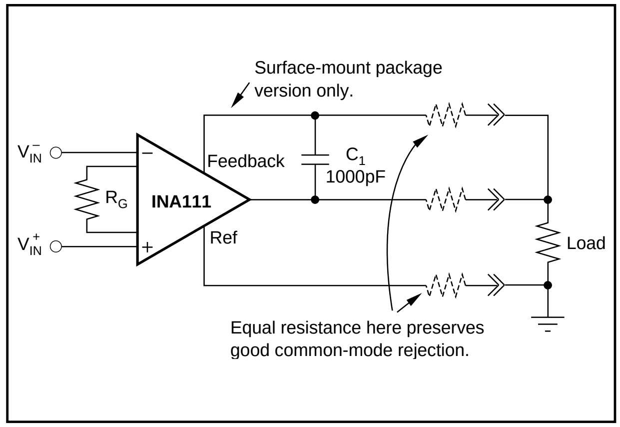


FIGURE 8. Remote Load and Ground Sensing.

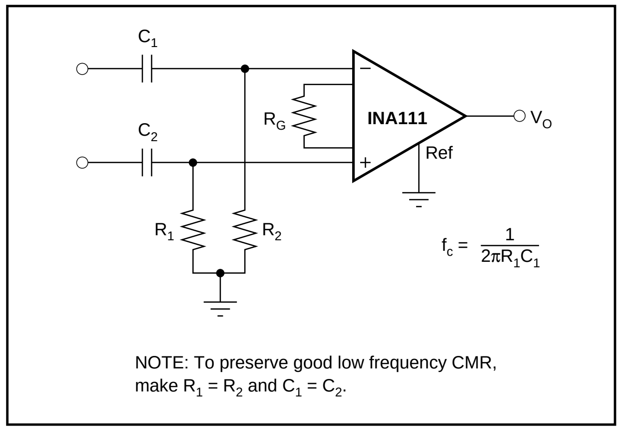


FIGURE 9. High-Pass Input Filter.

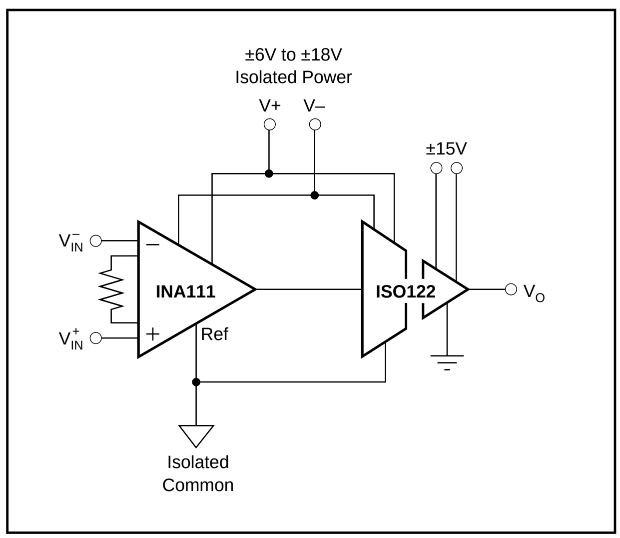


FIGURE 10. Galvanically Isolated Instrumentation Amplifier.

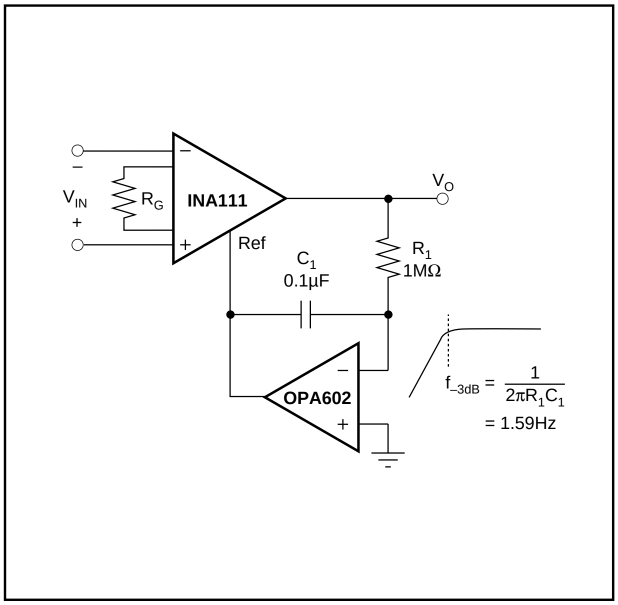


FIGURE 11. AC-Coupled Instrumentation Amplifier.

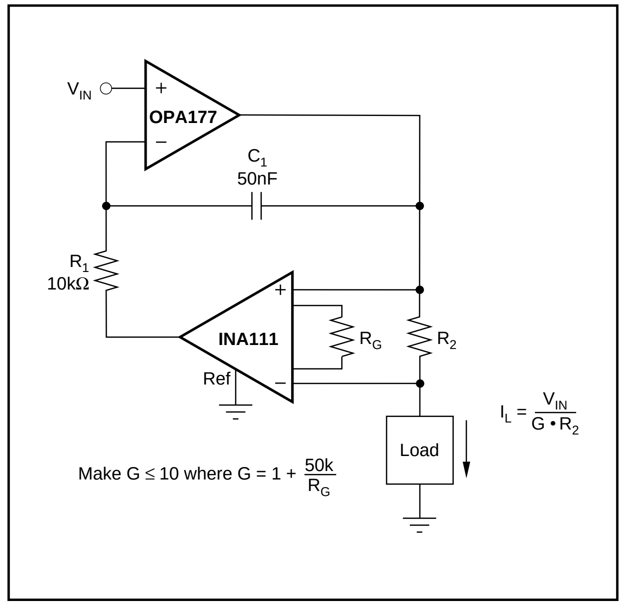


FIGURE 12. Voltage Controlled Current Source.

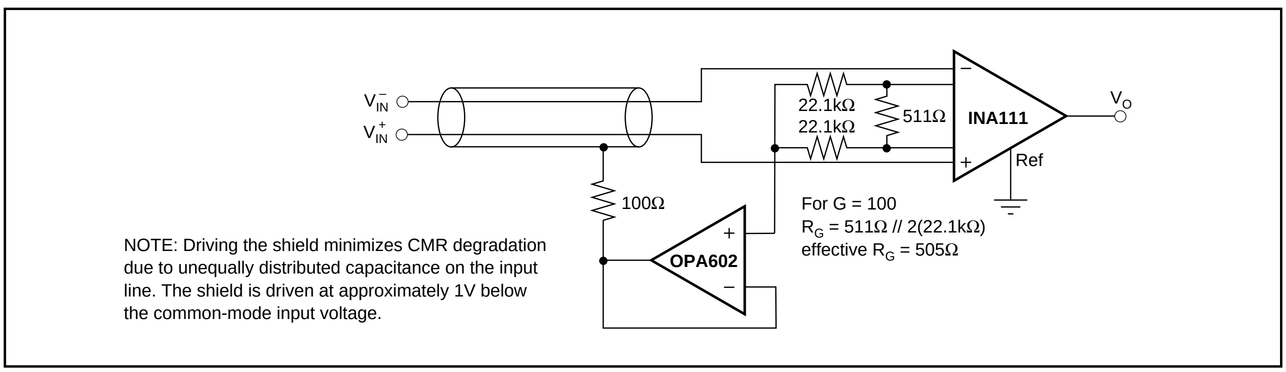


FIGURE 13. Shield Driver Circuit.

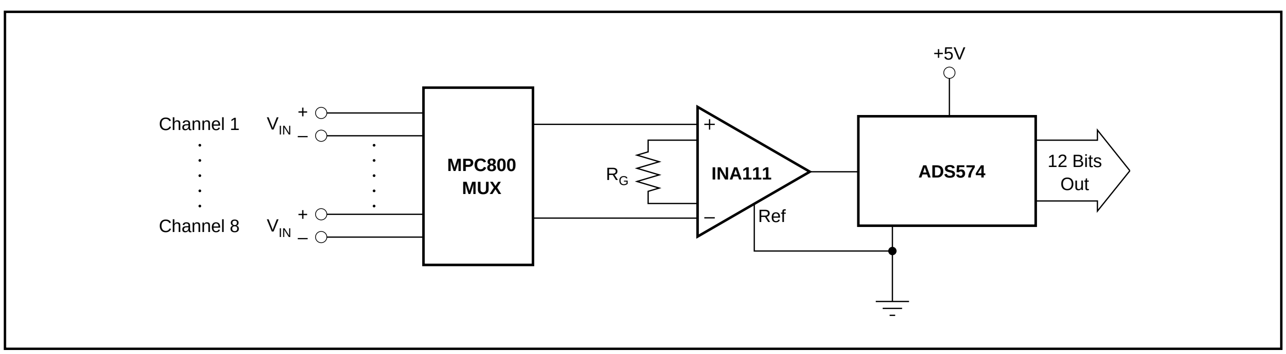


FIGURE 14. Multiplexed-Input Data Acquisition System.