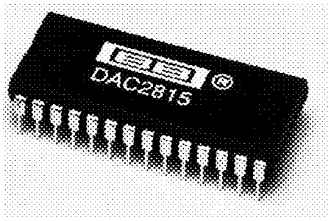
BURR - BROWN®



DAC2815

DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER (8-Bit Port Interface)

FEATURES

- COMPLETE DUAL DAC — INCLUDES INTERNAL REFERENCES AND OUTPUT AMPLIFIERS
- GUARANTEED SPECIFICATIONS OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- HIGH-SPEED 8 + 4-BIT PARALLEL INTERFACE
- LOW POWER: 300mW (150mW/DAC)
- LOW GAIN DRIFT: 5ppm/°C
- LOW NONLINEARITY: ±1/2 LSB max
- UNIPOLAR OR BIPOLAR OUTPUT
- CLEAR/RESET TO UNIPOLAR OR BIPOLAR ZERO

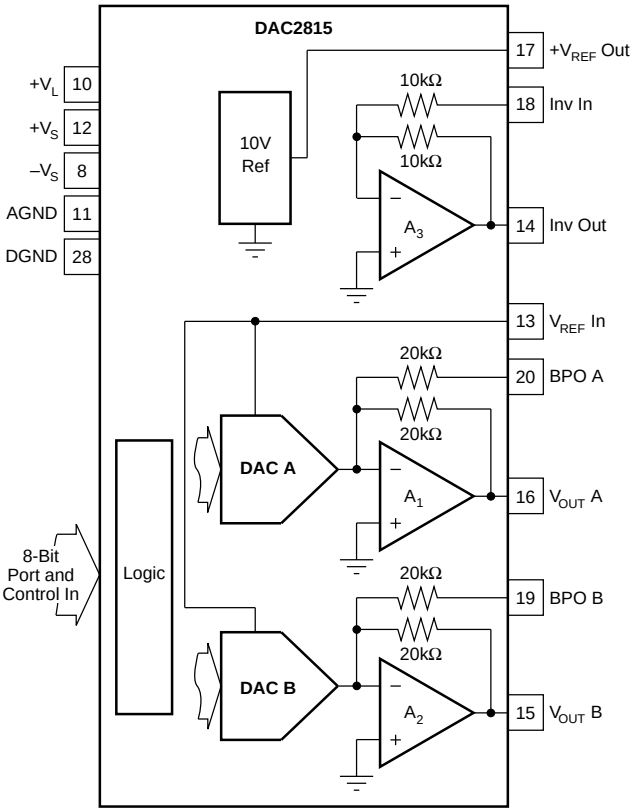
DESCRIPTION

The DAC2815 is one in a family of dual and quad 12-bit digital-to-analog converters (DACs). Serial, 8-bit, 12-bit interfaces are available.

The DAC2815 is complete. It contains CMOS logic, switches, a high-performance buried-zener reference, and low-noise bipolar output amplifiers. No external components are required for either unipolar 0 to 10V, 0 to –10V, or bipolar ±10V output ranges.

The DAC2815 has a 2-byte (8 + 4) double-buffered interface. Data is first loaded (level transferred) into the input registers in two steps for each DAC. Then both DACs are updated simultaneously. The DAC has an asynchronous clear control for reset to unipolar or bipolar zero depending on the mode selected. This feature is useful for power-on reset or system calibration. The DAC2815 is packaged in a 28-pin plastic DIP rated for the –40°C to +85°C extended industrial temperature range.

High-stability laser-trimmed thin film resistors assure high reliability and true 12-bit integral and differential linearity over the full specified temperature range.



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PDS-1110B
Printed in U.S.A. October, 1993

SPECIFICATIONS, Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2815AP			DAC2815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Resolution		12			*			Bits
V_{IH} (Input High Voltage)		2		5	*		*	V
V_{IL} (Input Low Voltage)		0		0.8	*		*	V
I_{IN} (Input Current)	T_A = 25°C			±1			*	µA
	T_A = –40°C to +85°C			±10			*	µA
C_{IN} (Input Capacitance)			0.8			*		pF
ACCURACY								
Integral, Relative Linearity[1]				±1			±1/2	LSB
Differential Nonlinearity[2]	T_A = 25°C			±1			*	LSB
	T_A = –40°C to +85°C		+1.5/–1				±1	LSB
Unipolar Offset Error	T_A = +25°C			±1			±0.5	mV
	T_A = –40°C TO +85°C			±3			*	mV
Bipolar Zero Error				±20			±10	mV
Gain Error Unipolar, Bipolar	With Internal or External 10.0V Ref			±0.2			±0.15	%
Power Supply Sensitivity[3]	V_S = ±11.4V to ±18V, V_L = +4.5V to +5.5V			30			*	ppmFSR/V
TEMPERATURE DRIFT								
Gain Drift Unipolar, Bipolar			±5	±30		*	±20	ppm/°C
Unipolar Offset Drift			±0.1	±5		*	*	ppmFSR/°C
Bipolar Zero Drift			±5	±15		*	±8	ppmFSR/°C
REFERENCE OUTPUT								
Output Voltage		+9.980	+10	+10.020	+9.985	*	+10.015	V
Reference Drift			±2	±30		*	±20	ppm/°C
Output Current	T_A = 25°C	+10/–5			*			mA
	T_A = –40°C to +85°C	+6.5/–5			*			mA
Max Load Capacitance (For Stability)			500			*		pF
Short Circuit Current			±20			*		mA
Load Regulation				40			*	ppm/mA
(ΔV_{OUT} vs ΔI_{LOAD})								
Supply Regulation				±5			*	ppm/V
(ΔV_{OUT} vs ΔV_S)								
INVERTER								
–10V Reference[4], Inverter Output		–10.020	–10	–9.980	–10.015	*	–9.985	V
–10V Reference Drift				±30			±20	ppm/°C
DC Output Impedance			0.1			*		Ω
Output Current		±7			*			mA
Max Load Capacitance (For Stability)			200			*		pF
Short Circuit Current			±30			*		mA
REFERENCE INPUT								
Reference Input Resistance		3.5	5		*	*		kΩ
Inverter Input Resistance		7	10		*	*		kΩ
BPO Input Resistance		14	20		*	*		kΩ
Reference Input Range				±10			*	V
ANALOG SIGNAL OUTPUTS								
Voltage Range		$–V_S$ + 1.4		$+V_S$ – 1.4	*		*	V
DC Output Impedance			0.1			*		Ω
Output Current		±5			*			mA
Max Load Capacitance (For Stability)	V_{OUT}		500			*		pF
Short Circuit Current			±30			*		mA
DYNAMIC PERFORMANCE[5]	C_L = 100pF							
Unipolar Mode Settling Time	To 1/2 LSB of Full Scale		2.5	10		*	*	µs
Bipolar Mode Settling Time	To 1/2 LSB of Full Scale		3.5	10		*	*	µs
Slew Rate			10			*		V/µs
Small-Signal Bandwidth			3			*		MHz
ANALOG GROUND CURRENT (Code Dependent)			±2			*		mA
DIGITAL CROSSTALK	Full Scale Transition C_L= 100pF		3			*		nV-s
D/A GLITCH IMPULSE			30			*		nV-s

SPECIFICATIONS (CONT), Guaranteed over T_A = –40°C to +85°C unless otherwise specified.

ELECTRICAL

Specifications as shown for V_S = ±12V or ±15V, V_L = +5V, and R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	DAC2815AP			DAC2815BP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY								
$+V_S$ and $-V_S$		±11.4	±15	±18	*	*	*	V
$+V_L$		4.5	5	5.5	*	*	*	V
$+I_S$			+10	+13.5		*	*	mA
$-I_S$			–10	–13.5		*	*	mA
$+I_L$	Digital Inputs = 0V or $+V_L$		0.2	1		*	*	mA
$+I_L$	Digital Inputs = V_{IL} or V_{IH}			5			*	mA
Total Power, All DACs			300	410		*	*	mW
TEMPERATURE RANGE								
Specified		–40		+85	*		*	°C
Operating		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}			75			*		°C/W

NOTES: (1) End point linearity. (2) Guaranteed monotonic. (3) Change in bipolar full scale output. Includes voltage output DAC, voltage reference, and reference inverter. (4) Inverter output with inverter input connected to $+V_{REF}$. (5) Guaranteed but not tested.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC2815AP	28-Pin Plastic DIP	215
DAC2815BP	28-Pin Plastic DIP	215

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

$+V_L$ to AGND	0V, +7V
$+V_L$ to DGND	0V, +7V
$+V_S$ to AGND	0V, +18V
$-V_S$ to AGND	0V,–18V
AGND to DGND	±0.3V
Any digital input to DGND	–0.3V, $+V_L$ +0.3V
Ref In to AGND	±25V
Ref In to DGND	±25V
Storage Temperature Range	–55°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature	+155°C
Output Short Circuit	Continuous to common or $\pm V_S$
Reference Short Circuit	Continuous to common or $+V_S$

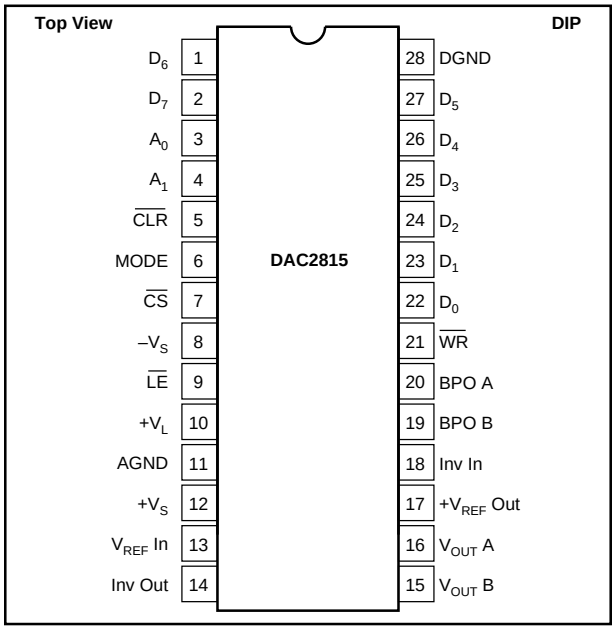
ORDERING INFORMATION

MODEL	LINEARITY ERROR (LSB)
DAC2815AP	±1
DAC2815BP	±1/2

PIN DESIGNATIONS

PIN	DESCRIPTOR	FUNCTION	PIN	DESCRIPTOR	FUNCTION
1	D_6	Data bit 6 input	28	DGND	Digital common
2	D_7	Data bit 7 input	27	D_5	Data bit 5 input
3	A_0	Address 0 input	26	D_4	Data bit 4 input
4	A_1	Address 1 input	25	D_3	Data bit 3 input
5	$\overline{CLR}$	Asychronous input reset to zero	24	D_2	Data bit 2 input
6	MODE	Selection input for unipolar or bipolar reset to zero	23	D_1	Data bit 1 input
7	$\overline{CS}$	Chip select enable, DAC A and DAC B	22	D_0	Data bit 0 input
8	$-V_S$	Negative analog power supply, –15V input	21	$\overline{WR}$	Write input, DAC A and DAC B
9	$\overline{LE}$	Latch data enable, DAC A and DAC B	20	BPO A	Bipolar offset input, DAC A
10	$+V_L$	Positive logic power supply, +5V input	19	BPO B	Bipolar offset input, DAC B
11	AGND	Analog common	18	Inv In	Inverter (A3) input
12	$+V_S$	Positive analog power supply, +15V input	17	$+V_{REF}$ Out	Reference voltage, +10V output
13	V_{REF} In	± Reference voltage input	16	V_{OUT} A	Analog output voltage, DAC A
14	Inv Out	Inverter (A_3) output	15	V_{OUT} B	Analog output voltage, DAC B

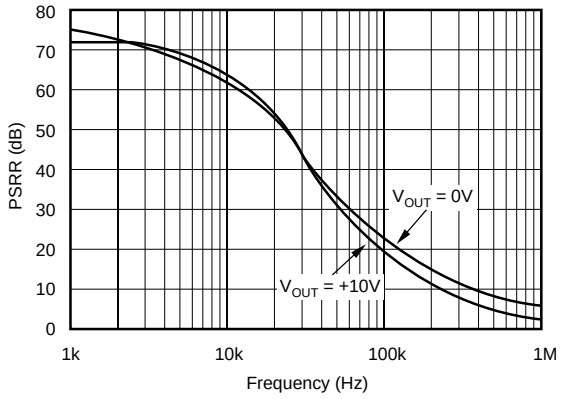
PIN CONFIGURATION



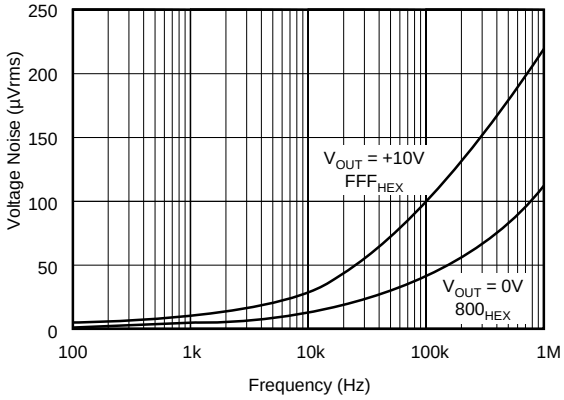
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

PSRR vs FREQUENCY (Bipolar Mode)



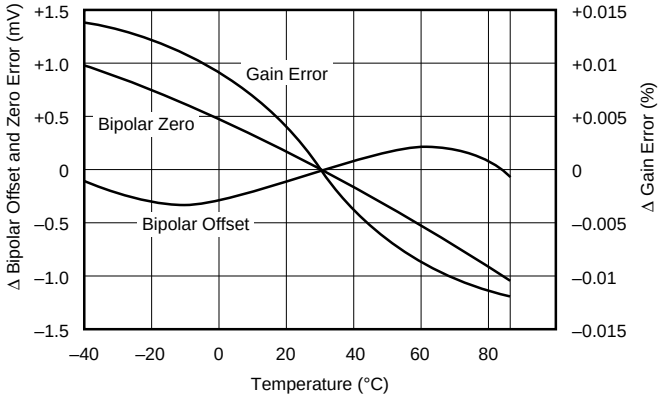
NOISE vs BANDWIDTH (Bipolar Mode)



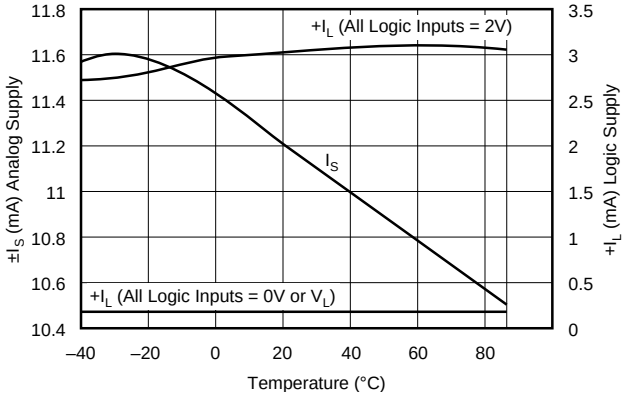
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

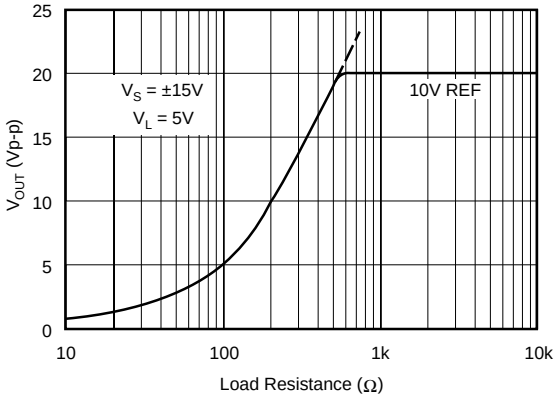
CHANGE OF GAIN, BIPOLAR OFFSET AND ZERO ERROR vs TEMPERATURE



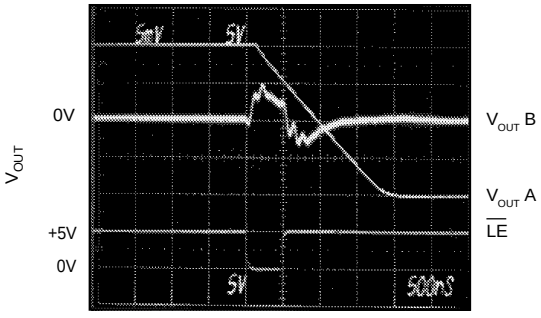
POWER SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs RESISTOR LOAD



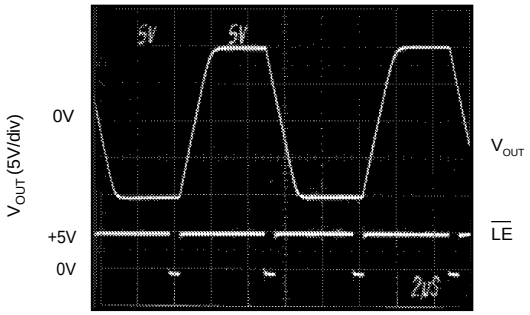
CROSSTALK (Bipolar Mode)



Time (500ns/div)

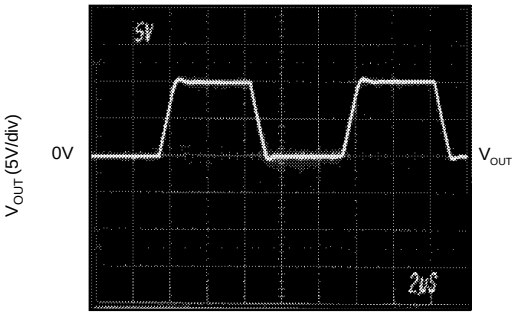
NOTE: Crosstalk is dominated by digital crosstalk/ feedthrough of the $\overline{LE}$ signal.

FULL-SCALE OUTPUT SWING BIPOLAR (20V Step)



Time (2µs/div)

FULL-SCALE OUTPUT SWING UNIPOLAR (10V Step)

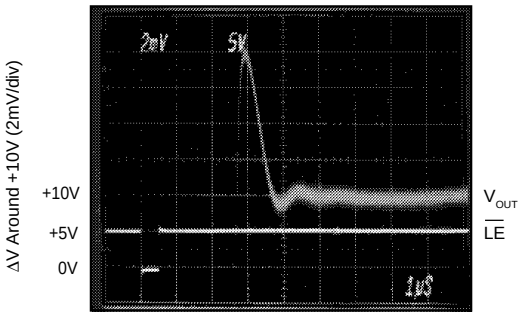


Time (2µs/div)

TYPICAL PERFORMANCE CURVES (CONT)

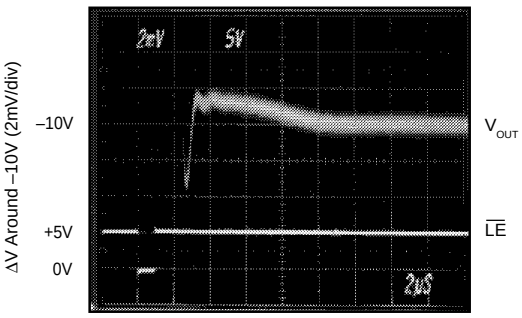
T_A = +25°C, V_S = ±12V or ±15V, V_L = +5V unless otherwise noted.

SETTLING TIME
BIPOLAR (–10V to +10V)



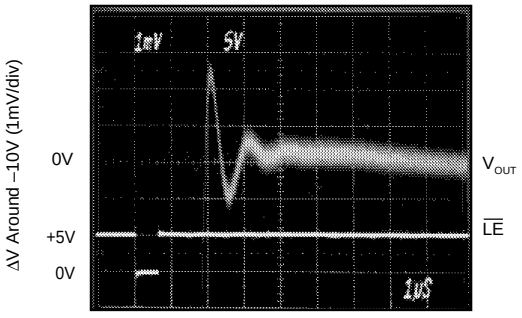
Time (1µs/div)

SETTLING TIME
BIPOLAR (+10V to –10V Step)



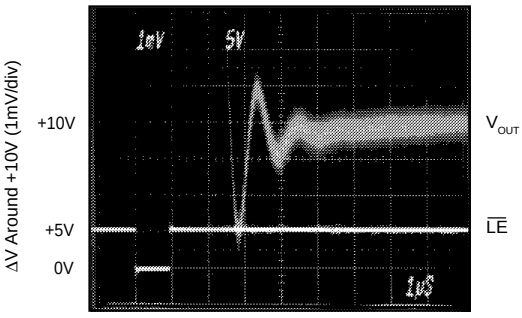
Time (2µs/div)

SETTLING TIME
UNIPOLAR (+10V to 0V STEP)



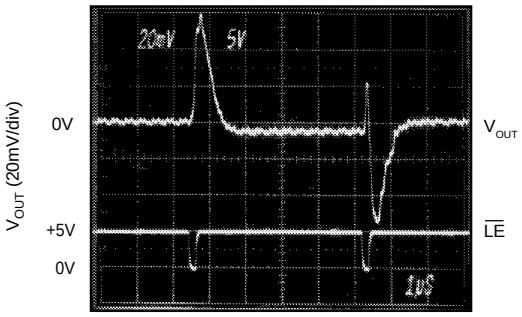
Time (1µs/div)

SETTLING TIME
UNIPOLAR (0V to +10V Step)



Time (1µs/div)

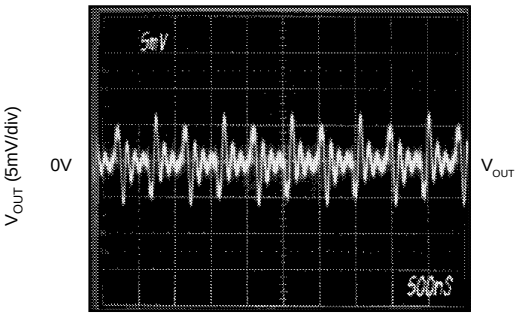
MAJOR CARRY GLITCH



Time (1µs/div)

NOTE: Data transition 800_{HEX} to $7FF_{HEX}$.

DIGITAL FEEDTHROUGH



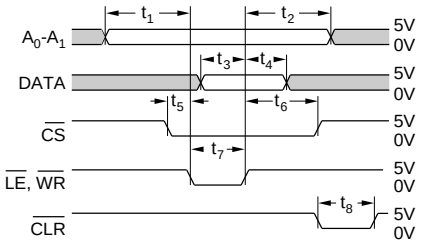
Time (500ns/div)

DAC output noise due to activity on digital inputs with latch disabled.

TIMING CHARACTERISTICS

$+V_L$ = +5V, T_A = –40°C to +85°C.

PARAMETER	MINIMUM
t_1—Address Valid to Write Setup Time	10ns
t_2—Address Valid to Write Hold Time	10ns
t_3—Data Setup Time	30ns
t_4—Data Hold Time	10ns
t_5—Chip Select to $\overline{LE}$ or Write Setup Time	0ns
t_6—Chip Select to $\overline{LE}$ or Write Hold Time	0ns
t_7—Write Pulse Width	40ns
t_8—Clear Pulse Width	40ns



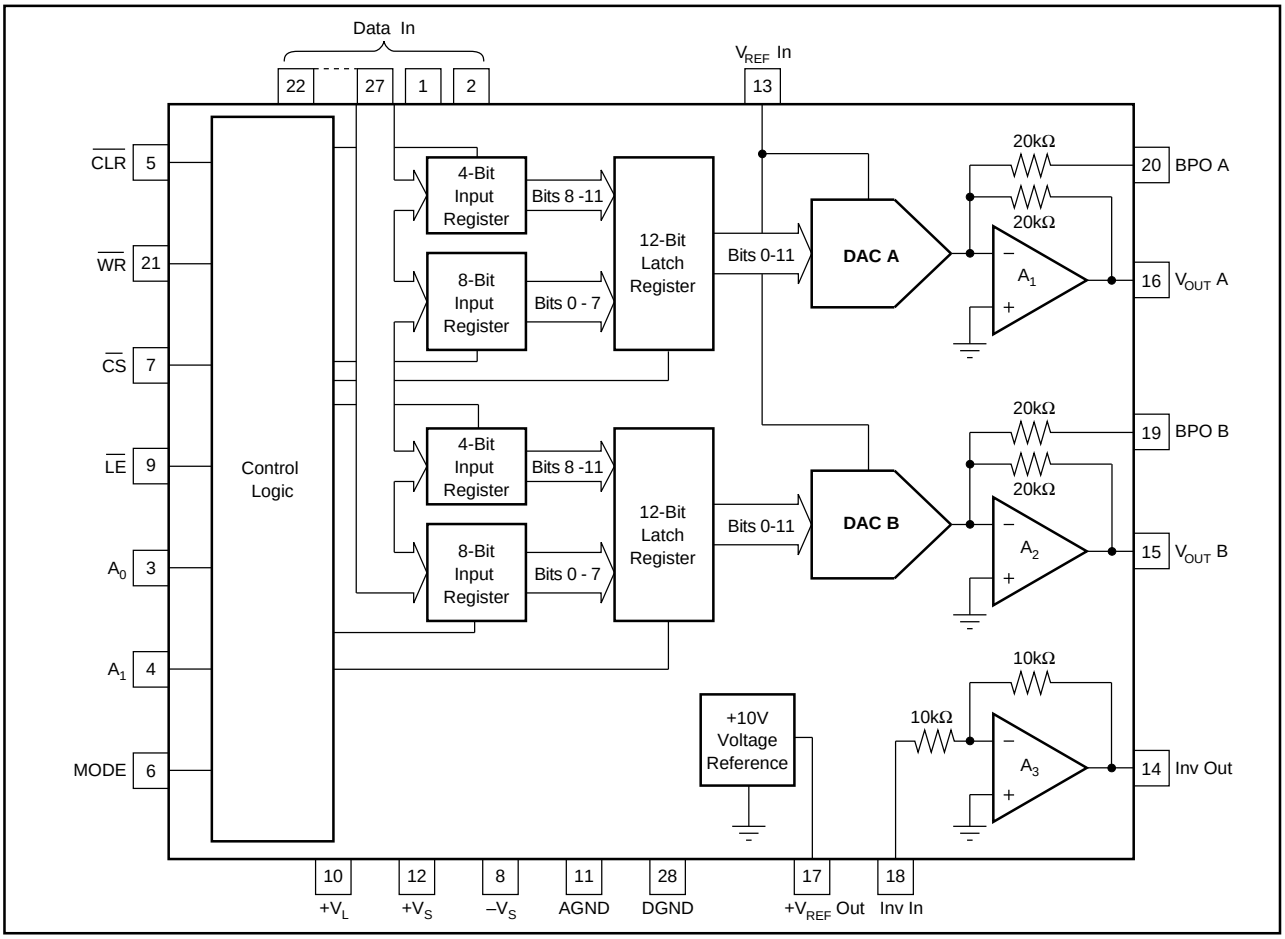
NOTES: (1) All input signal rise and fall times are measured from 10% to 90% of +5V. $t_R = t_F$ = 5ns.
(2) Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$.

INTERFACE LOGIC TRUTH TABLE

MODE	$\overline{CLR}$	$\overline{LE}$	$\overline{CS}$	$\overline{WR}$	A_1	A_0	FUNCTION
X	1	1	0	0	0	0	DAC A LS Input Register Loaded with D7-D0 (LSB)
X	1	1	0	0	0	1	DAC A MS Input Register Loaded with D3-(MSB)-D0
X	1	1	0	0	1	0	DAC B LS Input Register Loaded with D7-D0 (LSB)
X	1	1	0	0	1	1	DAC B MS Input Register Loaded with D3-(MSB)-D0
X	1	0	0	1	X	X	DAC A, DAC B Registers Updated Simultaneously from Input Registers
X	1	0	0	0	X	X	DAC A, DAC B Registers are Transparent
X	1	X	1	X	X	X	No Data Transfer
X	1	1	X	1	X	X	No Data Transfer
0	0	X	X	X	X	X	All Registers Cleared
1	0	X	X	X	X	X	Input Registers Cleared = 000_{HEX}, DAC Registers = 800_{HEX}

NOTE: X = Don't care.

FUNCTIONAL BLOCK DIAGRAM, DAC2815 — Dual 12-bit DAC, 8-bit Port



DISCUSSION OF SPECIFICATIONS

INPUT CODES

All digital inputs of the DAC2815 are TTL and 5V CMOS compatible. Input codes for the DAC2815 are either USB (Unipolar Straight Binary) or BOB (Bipolar Offset Binary) depending on the mode of operation. See Figure 3 for ±10V bipolar connection. See Figures 4 and 5 for 0 to 10V and 0 to –10V unipolar connections.

UNIPOLAR AND BIPOLAR OUTPUTS FOR SELECTED INPUT

DIGITAL INPUT	UNIPOLAR (USB)	BIPOLAR (BOB)
FFF_{HEX}	+Full scale	+Full scale
800_{HEX}	+1/2 Full scale	Zero
$7FF_{HEX}$	+1/2 Full scale – 1 LSB	Zero – 1 LSB
000_{HEX}	Zero	–Full scale

INTEGRAL OR RELATIVE LINEARITY

This term, also known as end point linearity, describes the transfer function of analog output to digital input code. Integral linearity error is the deviation of the analog output versus code transfer function from a straight line drawn through the end points.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the deviation from an ideal 1 LSB change in the output voltage when the input code changes by 1 LSB. A differential nonlinearity specification of ±1 LSB maximum guarantees monotonicity.

UNIPOLAR OFFSET ERROR

The output voltage for code 000_{HEX} when the DAC is in the unipolar mode of operation.

BIPOLAR ZERO ERROR

The output voltage for code 800_{HEX} when the DAC is in the bipolar mode of operation.

GAIN ERROR

The deviation of the output voltage span ($V_{MAX} – V_{MIN}$) from the ideal span of 10V – 1 LSB (unipolar mode) or 20V – 1 LSB (bipolar mode). The gain error is specified with and without the internal +10V reference error included.

OUTPUT SETTLING TIME

The time required for the output voltage to settle within a percentage-of-full-scale error band for a full scale transition. Settling to ±0.012% (1/2 LSB) is specified for the DAC2815.

DIGITAL-TO-ANALOG GLITCH

Ideally, the DAC output would make a clean step change in response to an input code change. In reality, glitches occur during the transition. See Typical Performance Curves.

DIGITAL CROSSTALK

Digital crosstalk is the glitch impulse measured at the output of one DAC due to a full scale transition on the other DAC—see Typical Performance Curves. It is dominated by digital coupling. Also, the integrated area of the glitch pulse is specified in nV–s. See table of electrical specifications.

DIGITAL FEEDTHROUGH

Digital feedthrough is the noise at a DAC output due to activity on the digital inputs—see Typical Performance Curves.

OPERATION

Depending on the address selected, the 4 MSBs or the 8 LSBs are written into the appropriate input register for each DAC when the $\overline{WR}$ signal is brought low. This data is latched in the input register when the $\overline{WR}$ goes high. Data are then transferred from the input registers to the DAC latch registers by bring $\overline{LE}$ low. The data are latched in the DAC latch registers when $\overline{LE}$ goes high. Both DACs are updated simultaneously.

When $\overline{CLR}$ is brought low, the input registers are cleared to 000_{HEX} (–10V), while the DAC registers = 800_{HEX}. If $\overline{LE}$ is brought low, the DACs are updated with 000_{HEX} resulting in –10V (bipolar) or 0V (unipolar) on the output.

CIRCUIT DESCRIPTION

Each of the two DACs in the DAC2815 consists of a CMOS logic section, a CMOS DAC cell, and an output amplifier. One buried-zener +10.0V reference and a reference inverter (for a –10.0V reference) are shared by both DACs.

Figure 1 is a simplified circuit for a DAC cell. An R, 2R ladder network is driven by a voltage reference at V_{REF}. Current from the ladder is switched either to I_{OUT} or AGND by 12 single-pole double-throw CMOS switches. This maintains constant current in each leg of the ladder regardless of

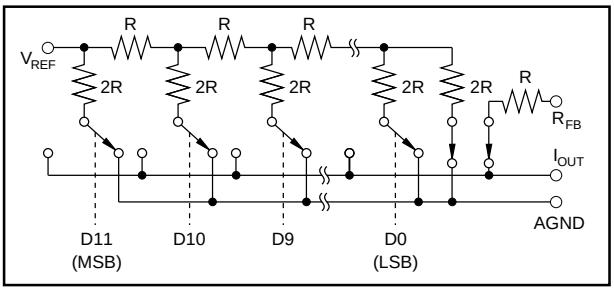


FIGURE 1. Simplified Circuit Diagram of DAC Cell.

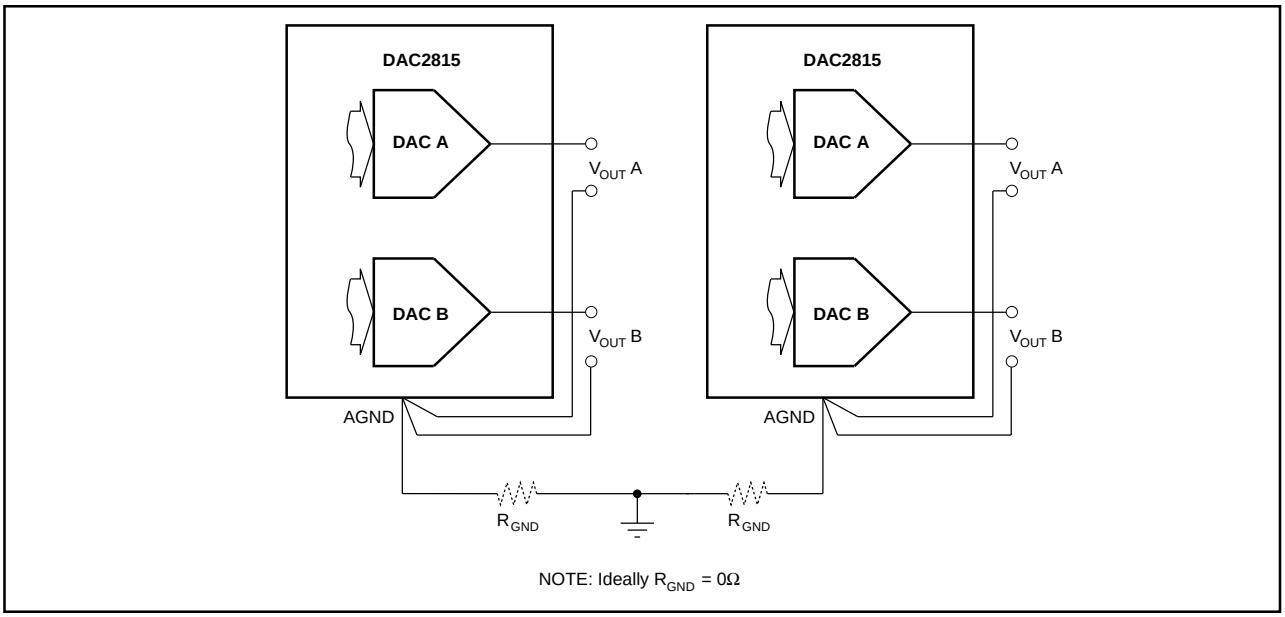


FIGURE 2. Recommended Ground Connections for Multiple DAC packages.

digital input code. This makes the resistance at V_{REF} constant (it can be driven by either a voltage or current reference). The reference can be either positive or negative polarity with a range of up to ±10V.

CMOS switches included in series with the ladder terminating resistor and the feedback resistor, R_{FB}, compensate for the temperature drift of the ladder switch ON resistance.

The output op amps are connected as transimpedance amplifiers to convert the DAC-cell output current into an output voltage. They have been specially designed and compensated for precision and fast settling in this application.

POWER SUPPLY CONNECTIONS

The DAC2815 is specified for operation with power supplies of V_L = +5V and V_S = either ±12V or ±15V. Even with the V_S supplies at ±11.4V the DACs can swing a full ±10V. Power supply decoupling capacitors (1µF tantalum) should be located close to the DAC power supply connections.

Separate digital and analog ground pins are provided to permit separate current returns. They should be connected together at one point. Proper layout of the two current returns will prevent digital logic switching currents from degrading the analog output signal. The analog ground current is code dependent so the impedance to the system reference ground must be kept to a minimum. Connect DACs as shown in Figure 2 or use a ground plane to keep ground impedance less than 0.1Ω for less than 0.1LSB error.

–10V REFERENCE

An internal inverting amplifier (Gain = –1.0V/V) is provided to invert the +10V reference. Connect $+V_{REF}$ Out to Inv In for a –10V reference at Inv Out.

OUTPUT RANGE CONNECTIONS

±10V Output Range

For a ±10V bipolar outputs connect the DAC2815 as shown in Figure 3. Connect the MODE to logic high (+5V) for reset to bipolar zero. With MODE connected low (GND) reset will be to –Full-Scale.

0 To +10V Output Range

For 0 to +10V unipolar outputs connect the DAC2815 as shown in Figure 4. Connect the MODE to logic low (GND) for reset to unipolar zero.

0 To –10V Output Range

For 0 to –10V unipolar outputs connect the DAC2815 as shown in Figure 5. Connect the MODE to logic low (GND) for reset to unipolar zero.

CONNECTION TO DIGITAL BUS

DAC2815s can easily be connected to a µprocessor bus. Decode your address lines to derive the control signals shown in Figure 6. Only one $\overline{\text{LATCH}}$ signal is required for a system where all DAC2815s are updated simultaneously. If you want to update DAC2815s independently, use separate $\overline{\text{LATCH}}$ signals. The $\overline{\text{LATCH}}$ and $\overline{\text{WRITE}}$ signals can be brought low simultaneously to update the DAC registers with the same processor instruction that writes the final 8-bit data word the DAC input registers.

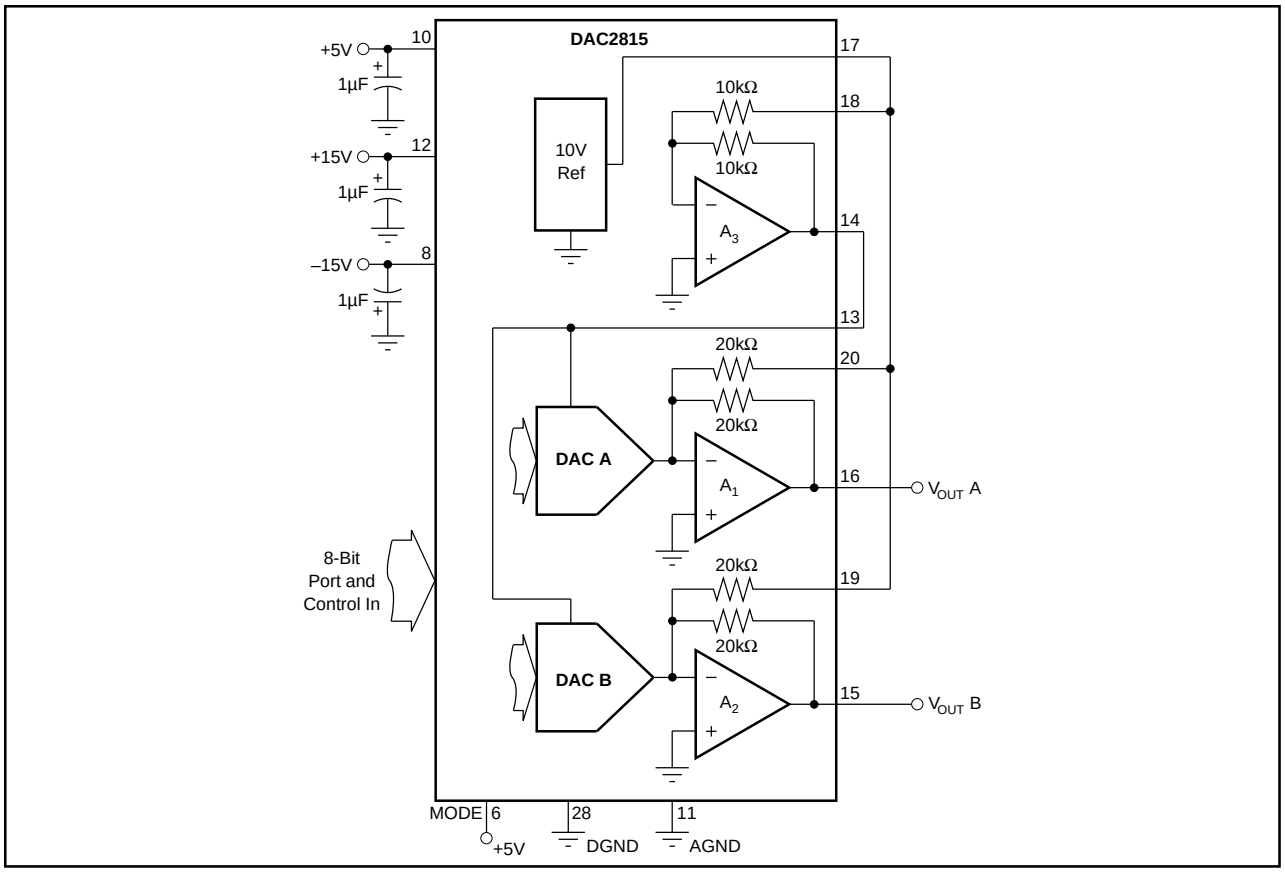


FIGURE 3. Analog Connections for ±10V DAC Output.

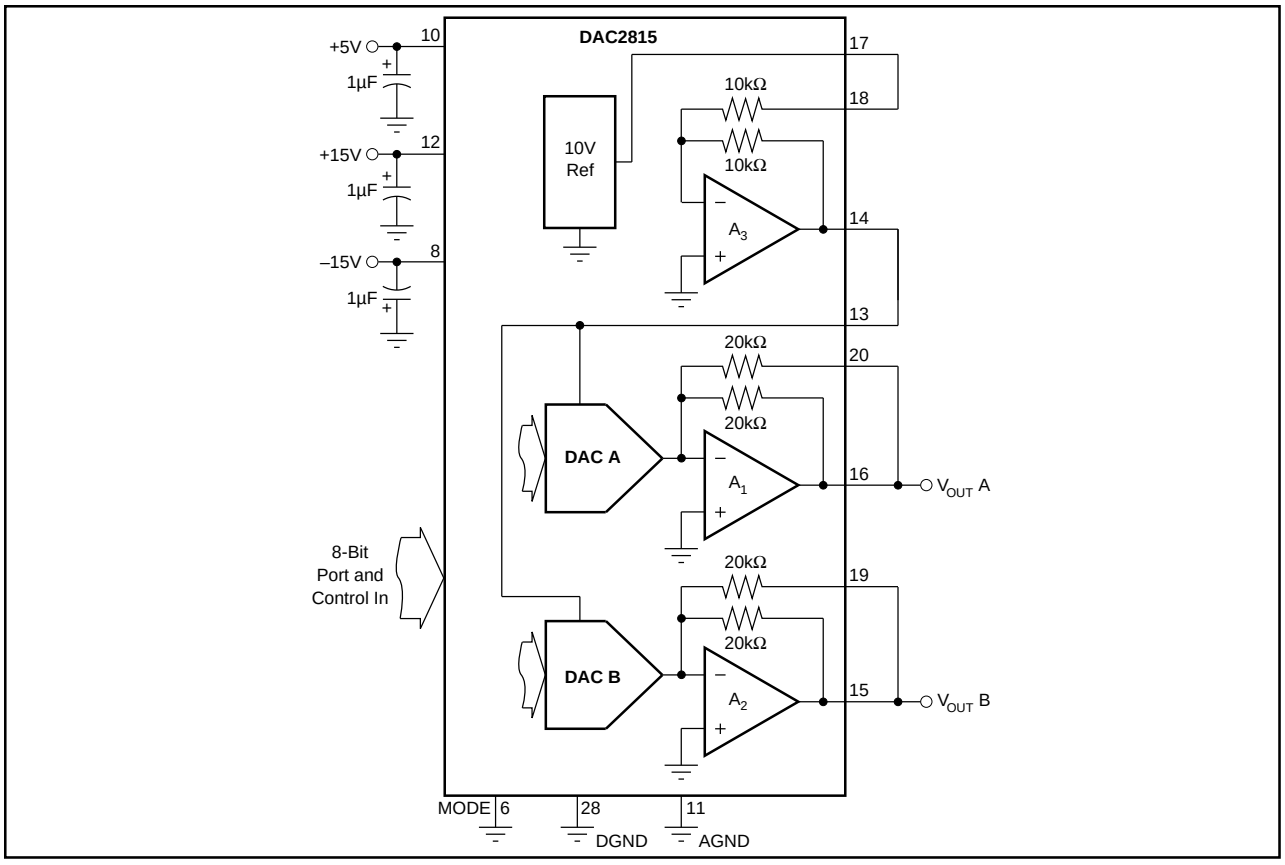


FIGURE 4. Analog Connections for 0 to +10V DAC Output.

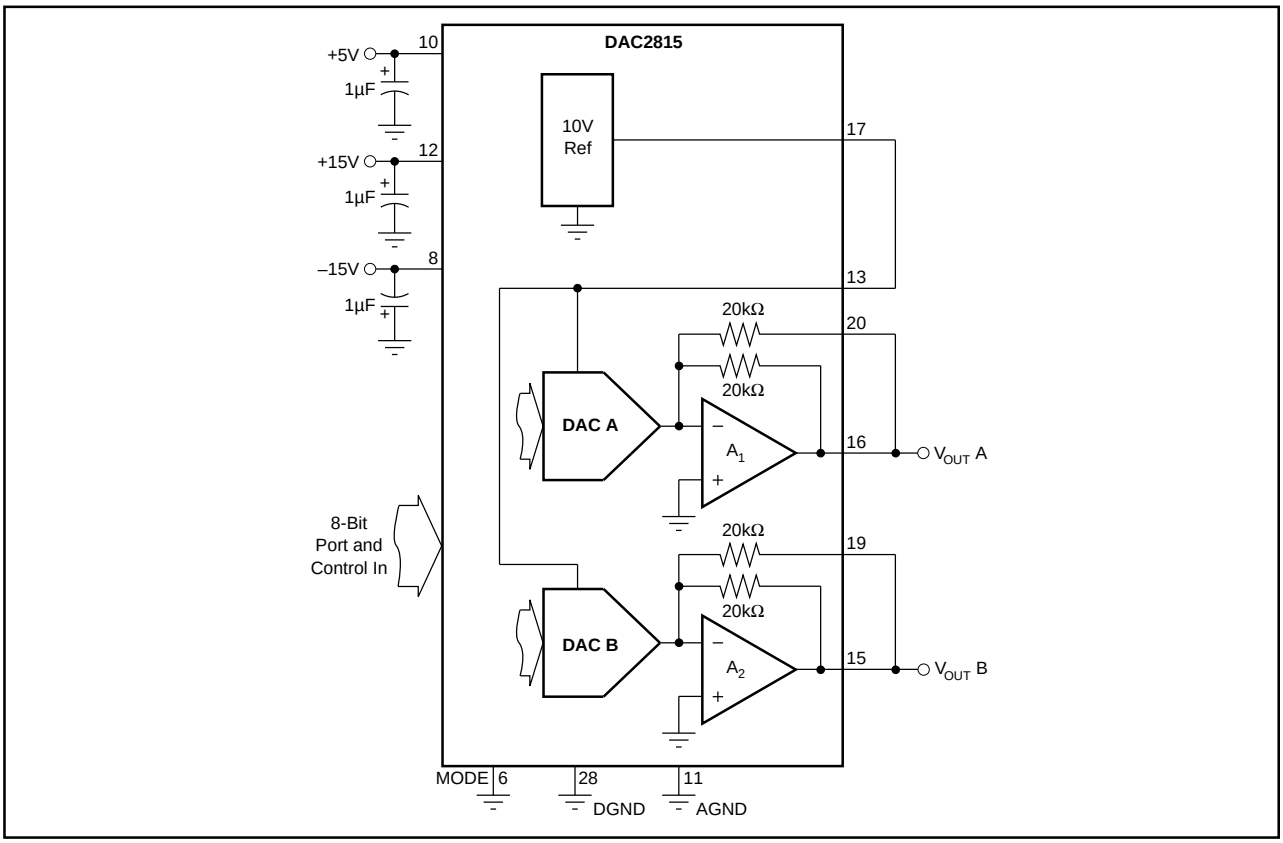


FIGURE 5. Analog Connections for 0 to –10V DAC Output.

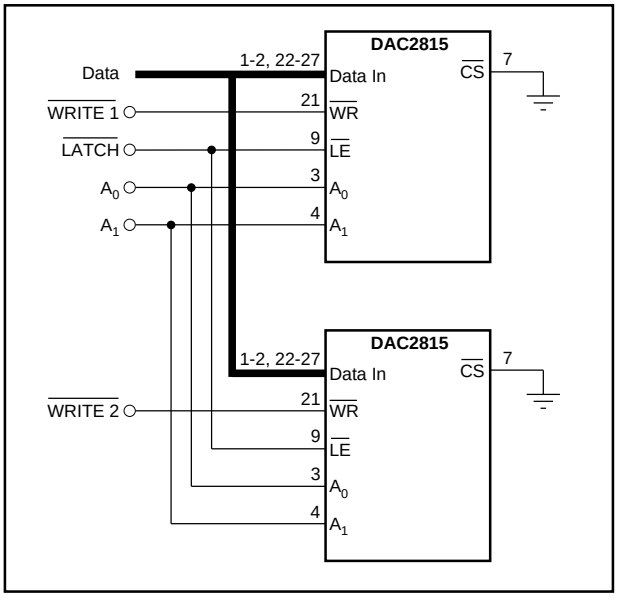


FIGURE 6. Logic Connection for Multiple DAC2815 Packages.