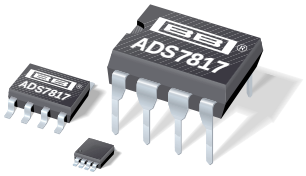
BURR-BROWN®



ADS7817

12-Bit Differential Input Micro Power Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- BIPOLAR INPUT RANGE
- TRUE DIFFERENTIAL INPUT
- 200kHz SAMPLING RATE
- MICRO POWER: 2.3mW at 200kHz
- POWER DOWN: 3µA Max
- AVAILABLE IN 8-LEAD MSOP PACKAGE
- SERIAL INTERFACE
- AC COMMON-MODE REJECTION

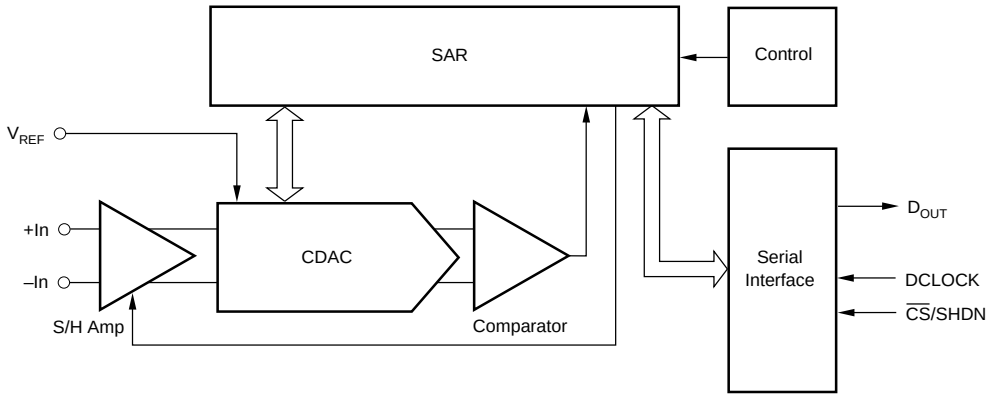
APPLICATIONS

- TRANSDUCER INTERFACE
- BATTERY OPERATED SYSTEMS
- REMOTE DATA ACQUISITION
- ISOLATED DATA ACQUISITION
- AC MOTOR CONTROL

DESCRIPTION

The ADS7817 is a 12-bit, 200kHz sampling analog-to-digital converter that features a high impedance fully differential analog input. The reference voltage can be varied from 100mV to 2.5V, with a corresponding input-referred resolution between 49µV and 1.22mV.

The differential input, low power, automatic power down, and small size make the ADS7817 ideal for direct connection to transducers in battery operated systems, remote data acquisition, or multi-channel applications. The ADS7817 is available in an 8-pin plastic mini-DIP, an 8-lead SOIC, or an 8-lead MSOP package.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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PDS-1369A
Printed in U.S.A., March, 1997

SPECIFICATIONS

At –40°C to +85°C, $+V_{CC}$ = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 200kHz, f_{CLK} = 16 • f_{SAMPLE}, –In = +2.5V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7817			ADS7817B			ADS7817C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT											
Full-Scale Input Span	+In – (–In)	$–V_{REF}$		$+V_{REF}$	*		*	*		*	V
Absolute Input Voltage	+In	–0.3		V_{CC} +0.3	*		*	*		*	V
	–In	–0.3		4	*		*	*		*	V
Capacitance			15			*			*		pF
Leakage Current			±1			*			*		µA
SYSTEM PERFORMANCE											
Resolution			12			*			*		Bits
No Missing Codes		11			12			*			Bits
Integral Linearity Error			±1	±2		±0.8	±2		±0.5	±1	LSB[1]
Differential Linearity Error			±1	±2		±0.7	±1		±0.4	±1	LSB
Offset Error			±1	±6		*	*		*	*	LSB
Gain Error			±0.5	±4		*	*		*	*	LSB
Noise			63			*			*		µVrms
Common-Mode Rejection			80			*			*		dB
Power Supply Rejection			82			*			*		dB
SAMPLING DYNAMICS											
Conversion Time				12			*			*	Clk Cycles
Acquisition Time		1.5			*			*			Clk Cycles
Throughput Rate				200			*			*	kHz
DYNAMIC CHARACTERISTICS											
Total Harmonic Distortion	V_{IN} = 5.0Vp-p at 1kHz		–83			*			*		dB
	V_{IN} = 5.0Vp-p at 5kHz		–81			*			*		dB
SINAD	V_{IN} = 5.0Vp-p at 1kHz		71			*			*		dB
Spurious Free Dynamic Range	V_{IN} = 5.0Vp-p at 1kHz		86			*			*		dB
REFERENCE INPUT											
Voltage Range		0.1		2.5	*		*	*		*	V
Resistance	$\overline{CS}$ = V_{CC}		5			*			*		GΩ
	$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			*			*		GΩ
Current Drain	At Code FF8h		20	100		*	*		*	*	µA
	f_{SAMPLE} = 12.5kHz		1.3	20		*	*		*	*	µA
	$\overline{CS}$ = V_{CC}		0.001	3		*	*		*	*	µA
DIGITAL INPUT/OUTPUT											
Logic Family			CMOS			*			*		
Logic Levels:											
V_{IH}	I_{IH} = +5µA	3		$+V_{CC}$ +0.3	*		*	*		*	V
V_{IL}	I_{IL} = +5µA	–0.3		0.8	*		*	*		*	V
V_{OH}	I_{OH} = –250µA	3.5			*			*			V
V_{OL}	I_{OL} = 250µA			0.4			*			*	V
Data Format			Binary Two's Complement				*			*	
POWER SUPPLY REQUIREMENTS											
V_{CC}	Specified Performance	4.75		5.25	*		*	*		*	V
Quiescent Current			460	800		*	*		*	*	µA
	f_{SAMPLE} = 12.5kHz[2, 3]		40			*			*		µA
	f_{SAMPLE} = 12.5kHz[3]		330			*			*		µA
Power Down	$\overline{CS}$ =V_{CC}, f_{SAMPLE} = 0Hz			3			*			*	µA
TEMPERATURE RANGE											
Specified Performance		–40		+85	*		*	*		*	°C

* Specifications same as grade to the left.

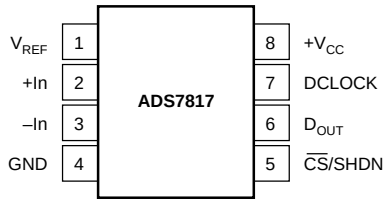
NOTE: (1) LSB means Least Significant Bit, with V_{REF} equal to +2.5V, one LSB is 1.22mV. (2) f_{CLK} = 3.2MHz, $\overline{CS}$ = V_{CC} for 251 clock cycles out of every 256. (3) See the Power Dissipation section for more information regarding lower sample rates.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_{CC}$	+6V
Analog Input	–0.3V to ($+V_{CC}$ + 0.3V)
Logic Input	–0.3V to ($+V_{CC}$ + 0.3V)
Case Temperature	+100°C
Junction Temperature	+150°C
Storage Temperature	+125°C
External Reference Voltage	+5.5V

NOTE: (1) Stresses above these ratings may permanently damage the device.

PIN CONFIGURATION



8-Pin PDIP,
8-Lead SOIC,
8-Lead MSOP

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	V_{REF}	Reference Input.
2	+In	Non Inverting Input.
3	–In	Inverting Input.
4	GND	Ground.
5	$\overline{CS}$/SHDN	Chip Select when LOW, Shutdown Mode when HIGH.
6	D_{OUT}	The serial output data word is comprised of 12 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of $\overline{CS}$ enables the serial output. After one null bit the data is valid for the next 12 edges.
7	DCLOCK	Data Clock synchronizes the serial data transfer and determines conversion speed.
8	$+V_{CC}$	Power Supply.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL LINEARITY ERROR (LSB)	TEMPERATURE RANGE	PACKAGE	PACKAGE DRAWING NUMBER[1]
ADS7817P	±2	±2	–40°C to +85°C	Plastic DIP	006
ADS7817U	±2	±2	–40°C to +85°C	SOIC	182
ADS7817E	±2	±2	–40°C to +85°C	MSOP	337
ADS7817PB	±2	±1	–40°C to +85°C	Plastic DIP	006
ADS7817UB	±2	±1	–40°C to +85°C	SOIC	182
ADS7817EB	±2	±1	–40°C to +85°C	MSOP	337
ADS7817PC	±1	±1	–40°C to +85°C	Plastic DIP	006
ADS7817UC	±1	±1	–40°C to +85°C	SOIC	182
ADS7817EC	±1	±1	–40°C to +85°C	MSOP	337

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

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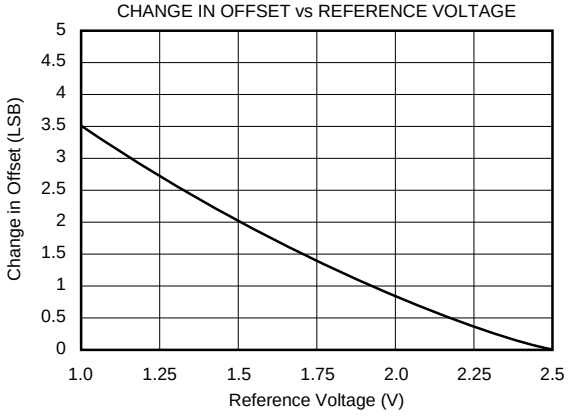
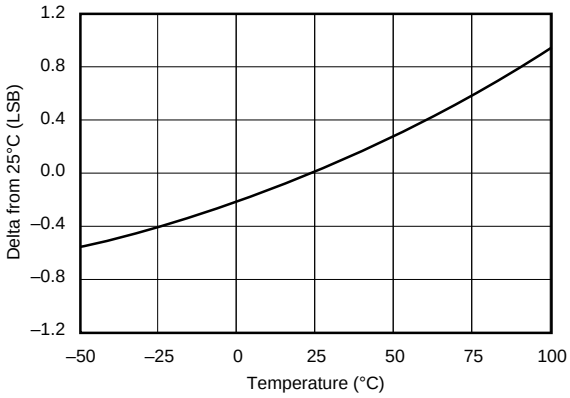
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE}, –In = +2.5V, unless otherwise specified.

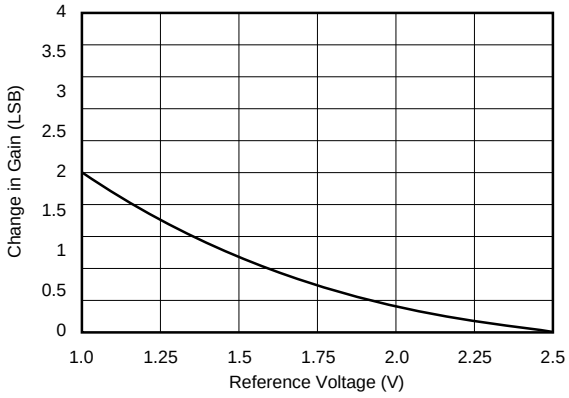
CHANGE IN OFFSET vs REFERENCE VOLTAGE



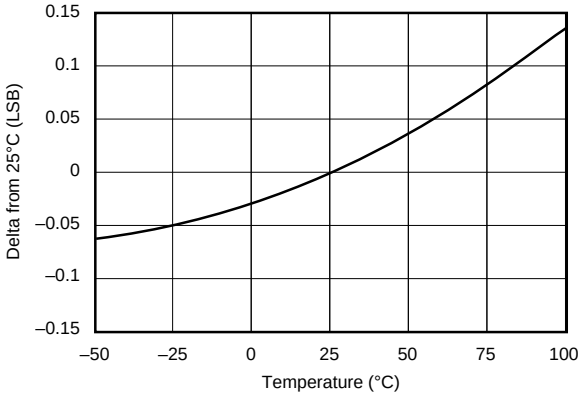
CHANGE IN OFFSET vs TEMPERATURE



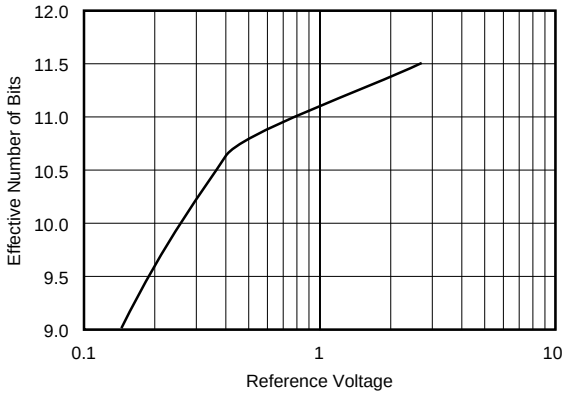
CHANGE IN GAIN vs REFERENCE VOLTAGE



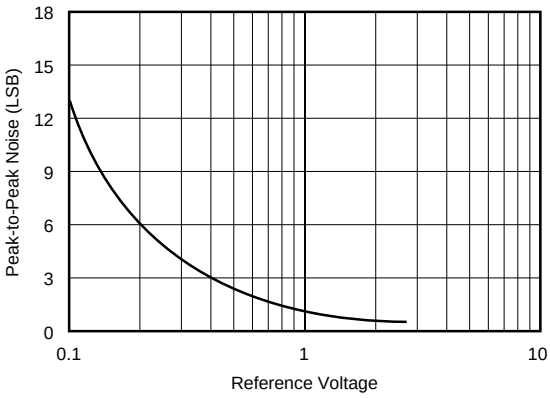
CHANGE IN GAIN vs TEMPERATURE



EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE



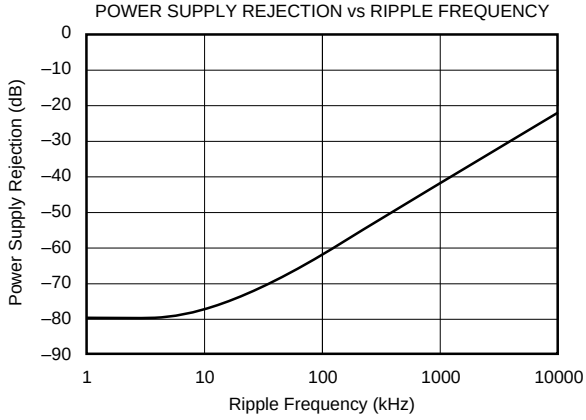
PEAK-TO-PEAK NOISE vs REFERENCE VOLTAGE



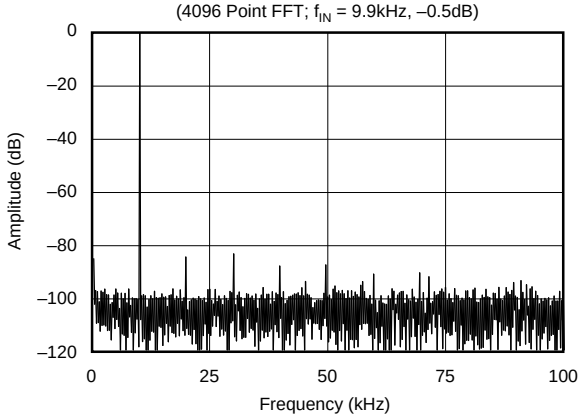
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE}, –In = +2.5V, unless otherwise specified.

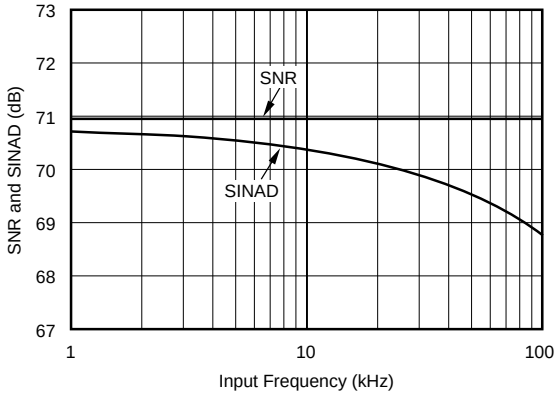
POWER SUPPLY REJECTION vs RIPPLE FREQUENCY



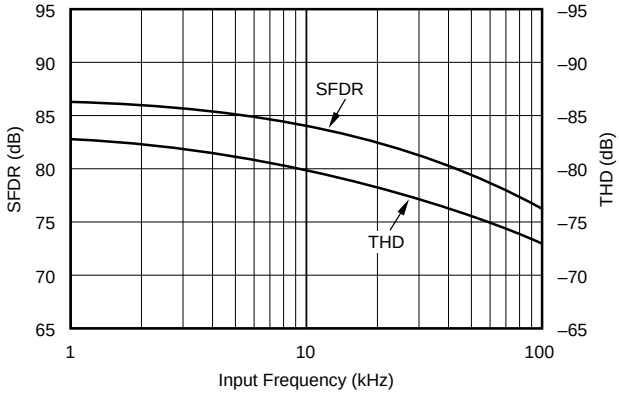
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 9.9kHz, –0.5dB)



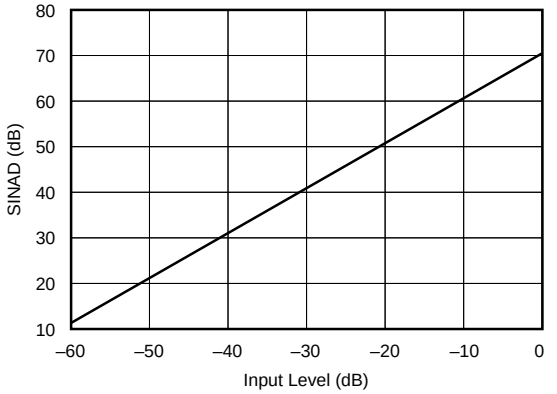
SIGNAL-TO-NOISE RATIO AND
SIGNAL-TO-(NOISE+DISTORTION)
vs INPUT FREQUENCY



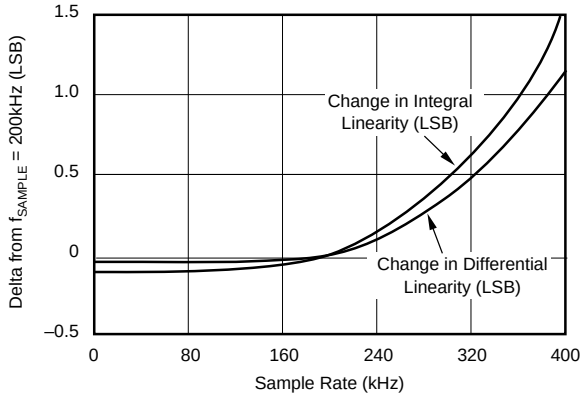
SPURIOUS FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY



SIGNAL-TO-(NOISE+DISTORTION)
vs INPUT LEVEL



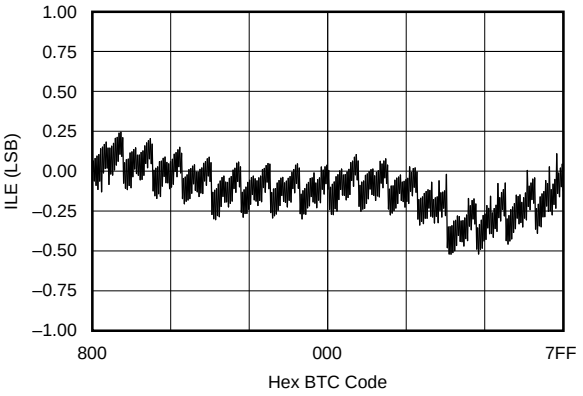
CHANGE IN INTEGRAL LINEARITY and DIFFERENTIAL
LINEARITY vs SAMPLE RATE



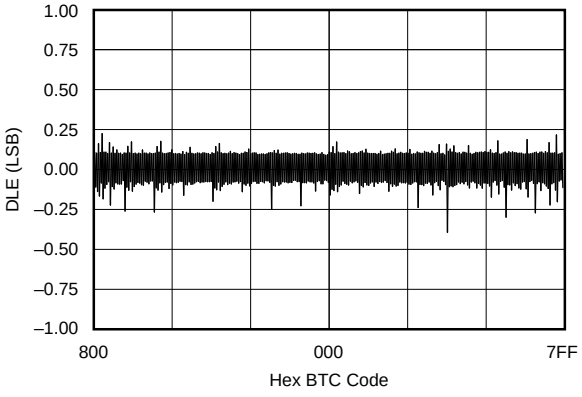
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE}, –In = +2.5V, unless otherwise specified.

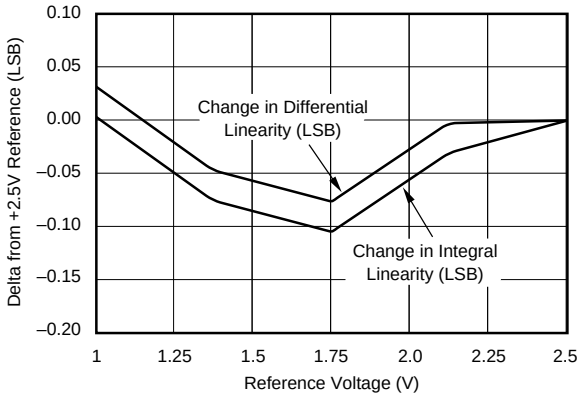
INTEGRAL LINEARITY ERROR vs CODE



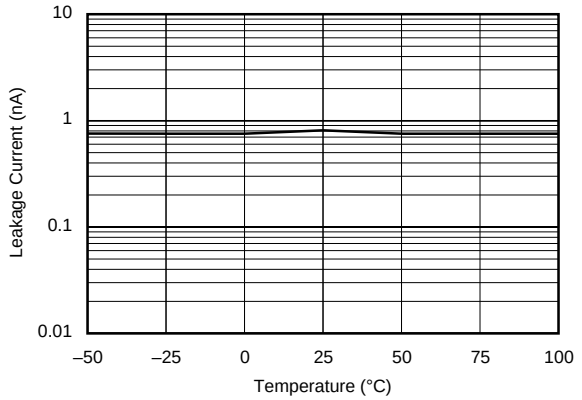
DIFFERENTIAL LINEARITY ERROR vs CODE



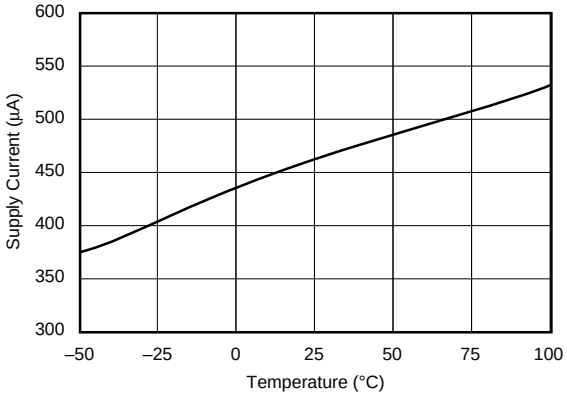
CHANGE IN INTEGRAL LINEARITY AND DIFFERENTIAL LINEARITY vs REFERENCE VOLTAGE



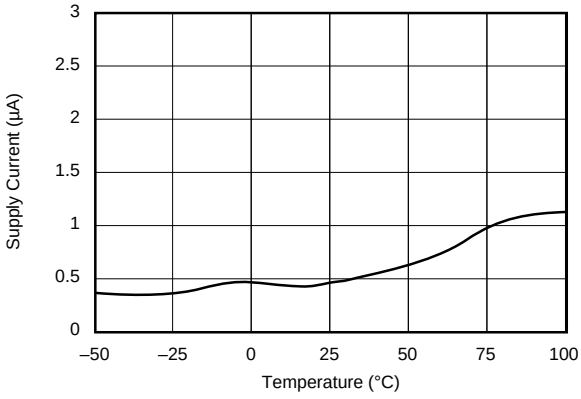
INPUT LEAKAGE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



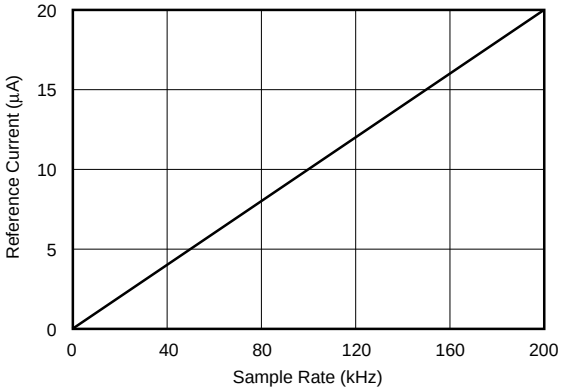
POWER DOWN SUPPLY CURRENT vs TEMPERATURE



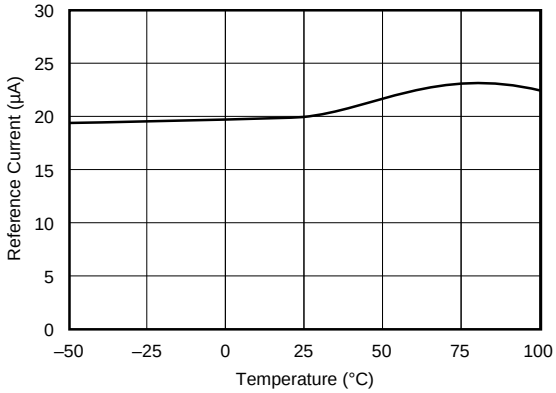
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = +5V, V_{REF} = +2.5V, f_{SAMPLE} = 200kHz, and f_{CLK} = 16 • f_{SAMPLE}, –In = +2.5V, unless otherwise specified.

REFERENCE CURRENT vs SAMPLE RATE
(Code = FF8h)



REFERENCE CURRENT vs TEMPERATURE
(Code = FF8h)



THEORY OF OPERATION

The ADS7817 is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution which inherently includes a sample/hold function. The converter is fabricated on a 0.6µ CMOS process. The architecture and process allow the ADS7817 to acquire and convert an analog signal at up to 200,000 conversions per second while consuming very little power.

The ADS7817 requires an external reference, an external clock, and a single +5V power source. The external reference can be any voltage between 100mV and 2.5V. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS7817.

The external clock can vary between 10kHz (625Hz throughput) and 3.2MHz (200kHz throughput). The duty cycle of the clock is essentially unimportant as long as the minimum high and low times are at least 150ns. The minimum clock frequency is set by the leakage on the capacitors internal to the ADS7817.

The analog input is provided to two input pins: +In and –In. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the D_{OUT} pin is for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS7817 after the conversion is complete and to obtain the serial data least significant bit first. See the Digital Interface section for more information.

ANALOG INPUT

The analog input is bipolar and fully differential. There are two general methods of driving the analog input of the ADS7817: single-ended or differential (see Figure 1). When the input is single-ended, the –In input is held at a fixed voltage. The +In input swings around the same voltage and the peak-to-peak amplitude is 2 • V_{REF}. The value of V_{REF} determines the range over which the common voltage may vary (see Figure 2).

When the input is differential, the amplitude of the input is the difference between the +In and –In input, or: +In – (–In). A voltage or signal is common to both of these inputs. The peak-to-peak amplitude of each input is V_{REF} about this common voltage. However, since the inputs are 180° out of phase, the peak-to-peak amplitude of the difference voltage is 2 • V_{REF}. The value of V_{REF} also determines the range of the voltage that may be common to both inputs (see Figure 3).

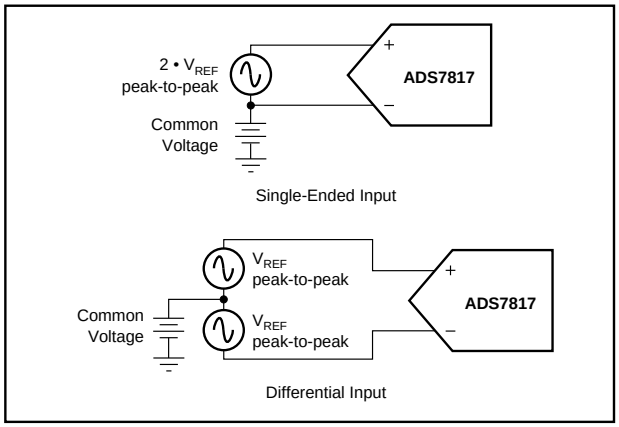


FIGURE 1. Methods of Driving the ADS7817: Single-Ended or Differential.

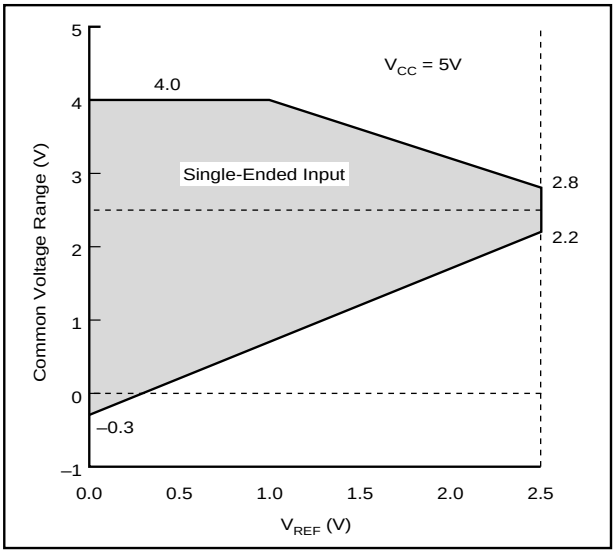


FIGURE 2. Single-Ended Input: Common Voltage Range vs V_{REF}.

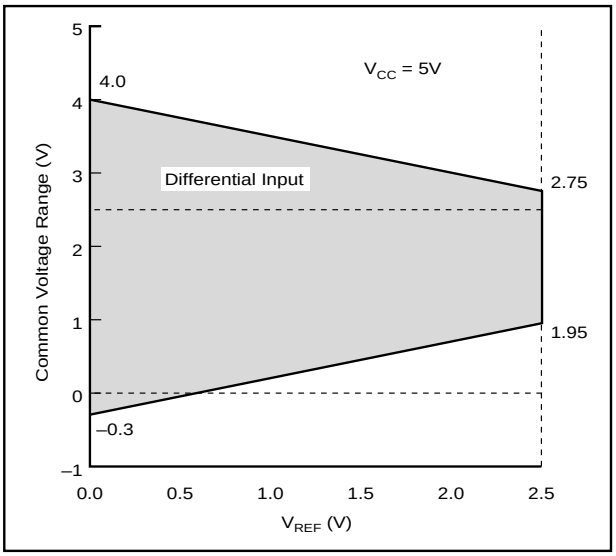


FIGURE 3. Differential Input: Common Voltage Range vs V_{REF}.

In each case, care should be taken to ensure that the output impedance of the sources driving the +In and –In inputs are matched. If this is not observed, the two inputs could have different settling times. This may result in offset error, gain error, and linearity error which change with both temperature and input voltage. If the impedance cannot be matched, the errors can be lessened by giving the ADS7817 more acquisition time.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, and source impedance. Essentially, the current into the ADS7817 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (15pF) to a 12-bit settling level within 1.5 clock cycles. When the converter goes into the hold mode or while it is in the power down mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. The +In input should always remain within the range of GND –300mV to V_{CC} +300mV. The –In input should always remain within the range of GND –300mV to 4V. Outside of these ranges, the converter's linearity may not meet specifications.

REFERENCE INPUT

The external reference sets the analog input range. The ADS7817 will operate with a reference in the range of 100mV to 2.5V. There are several important implications of this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to two times the reference voltage divided by 4096. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. The typical performance curves of "Change in Offset vs Reference Voltage" and "Change in Gain vs Reference Voltage" provide more information.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 2.5V reference, the internal noise of the converter typically contributes only 0.52 LSB peak-to-peak of potential error to the output code. When the external reference is 100mV, the potential error contribution from the internal noise will be 25 times larger—13 LSBs. The errors due to the internal noise are gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult the typical performance curves "Effective Number of Bits vs Reference Voltage" and "Peak-to-Peak Noise vs Reference Voltage." Note that the effective number of bits (ENOB) figure is calculated based on the converter's signal-to-(noise + distortion) with a 1kHz, 0dB input signal. SINAD is related to ENOB as follows: SINAD = 6.02 • ENOB + 1.76.

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to external sources of error such as nearby digital signals and electromagnetic interference.

The current that must be provided by the external reference will depend on the conversion result. The current is lowest at negative full-scale (800h) and is typically 15µA at a 200kHz conversion rate (25°C). For the same conditions, the current will increase as the analog input approaches positive full scale, reaching 25µA at an output result of 7FFh. The current does not increase linearly, but depends, to some degree, on the bit pattern of the digital output.

The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce the overall current drain from the reference. The reference current changes only slightly with temperature. See the curves, "Reference Current vs Sample Rate" and "Reference Current vs Temperature" in the Typical Performance Curves section for more information.

DIGITAL INTERFACE

SERIAL INTERFACE

The ADS7817 communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface as shown in Figure 4 and Table I. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems will capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample TIme	1.5		2.0	Clk Cycles
t_{CONV}	Conversion Time		12		Clk Cycles
t_{CYC}	Throughput Rate			200	kHz
t_{CSD}	$\overline{CS}$ Falling to DCLOCK LOW			0	ns
t_{SUCS}	$\overline{CS}$ Falling to DCLOCK Rising	30			ns
t_{hDO}	DCLOCK Falling to Current D_{OUT} Not Valid	15			ns
t_{dDO}	DCLOCK Falling to Next D_{OUT} Valid		85	150	ns
t_{dis}	$\overline{CS}$ Rising to D_{OUT} Tri-State		25	50	ns
t_{en}	DCLOCK Falling to D_{OUT} Enabled		50	100	ns
t_f	D_{OUT} Fall Time		70	100	ns
t_r	D_{OUT} Rise Time		60	100	ns

TABLE I. Timing Specifications –40°C to +85°C.

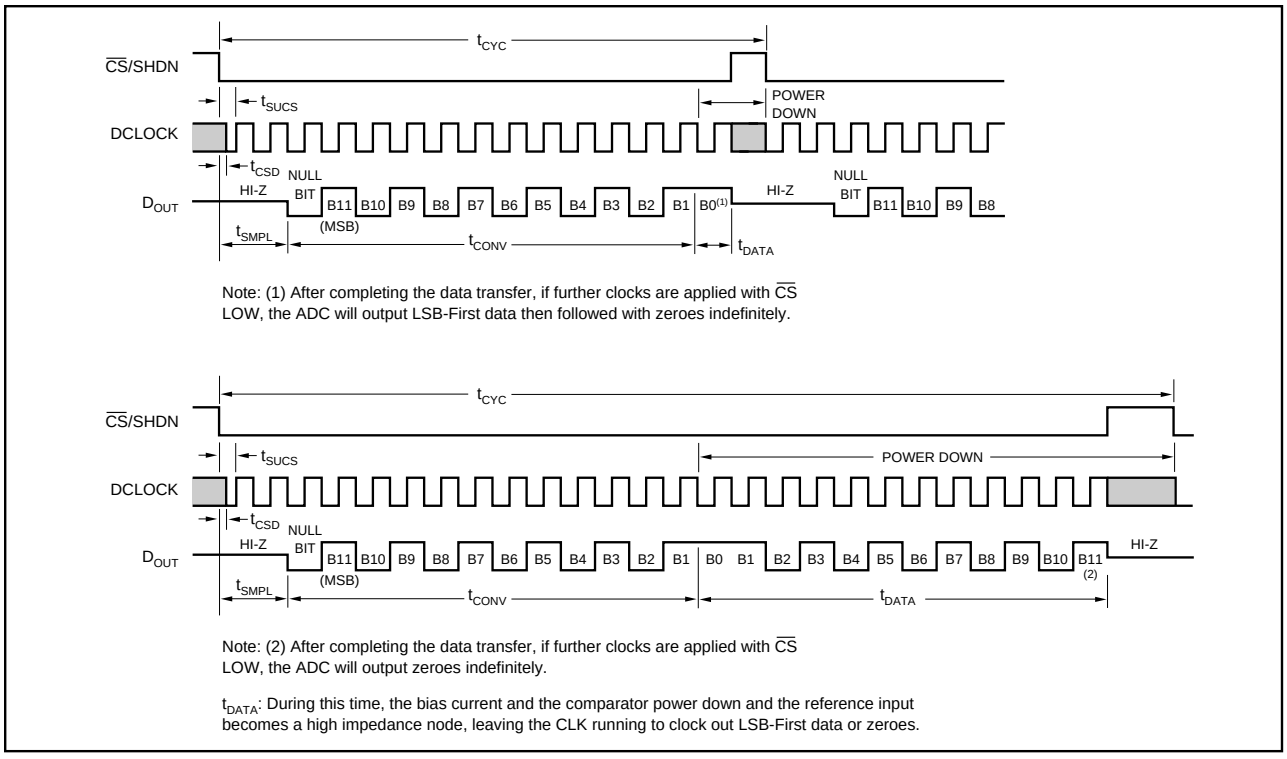


FIGURE 4. ADS7817 Basic Timing Diagrams.

A falling $\overline{CS}$ signal initiates the conversion and data transfer. The first 1.5 to 2.0 clock periods of the conversion cycle are used to sample the input signal. After the second falling DCLOCK edge, D_{OUT} is enabled and will output a LOW value for one clock period. For the next 12 DCLOCK periods, D_{OUT} will output the conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks will repeat the output data but in a least significant bit first format.

After the most significant bit (B11) has been repeated, D_{OUT} will tri-state. Subsequent clocks will have no effect on the converter. A new conversion is initiated only when $\overline{CS}$ has been taken HIGH and returned LOW.

DATA FORMAT

The output data from the ADS7817 is in Binary Two's Complement format as shown in Table II. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain error, or noise.

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT: BINARY TWO'S COMPLEMENT	
		BINARY CODE	HEX CODE
Full Scale Input Span	$2 \cdot V_{REF}$		
Least Significant Bit (LSB)	$2 \cdot V_{REF}/4096$		
+Full Scale	V_{REF} –1 LSB	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
Midscale – 1 LSB	0V – 1 LSB	1111 1111 1111	FFF
–Full Scale	$–V_{REF}$	1000 0000 0000	800

TABLE II. Ideal Input Voltages and Output Codes.

POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design allow the ADS7817 to convert at up to a 200kHz rate while requiring very little power. Still, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS7817 scales directly with conversion rate. The first step to achieving the lowest power dissipation is to find the lowest conversion rate that will satisfy the requirements of the system.

In addition, the ADS7817 is in power down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is HIGH (see Figure 1). Ideally, each conversion should occur as quickly as possible, preferably, at a 3.2MHz clock rate. This way, the converter spends the longest possible time in the power down mode. This is very important as the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components) but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously, until the power down mode is entered.

Figure 6 shows the current consumption of the ADS7817 versus sample rate. For this graph, the converter is clocked at 3.2MHz regardless of the sample rate—$\overline{CS}$ is HIGH for the remaining sample period. Figure 7 also shows current consumption versus sample rate. However, in this case, the DCLOCK period is 1/16th of the sample period—$\overline{CS}$ is HIGH for one DCLOCK cycle out of every 16.

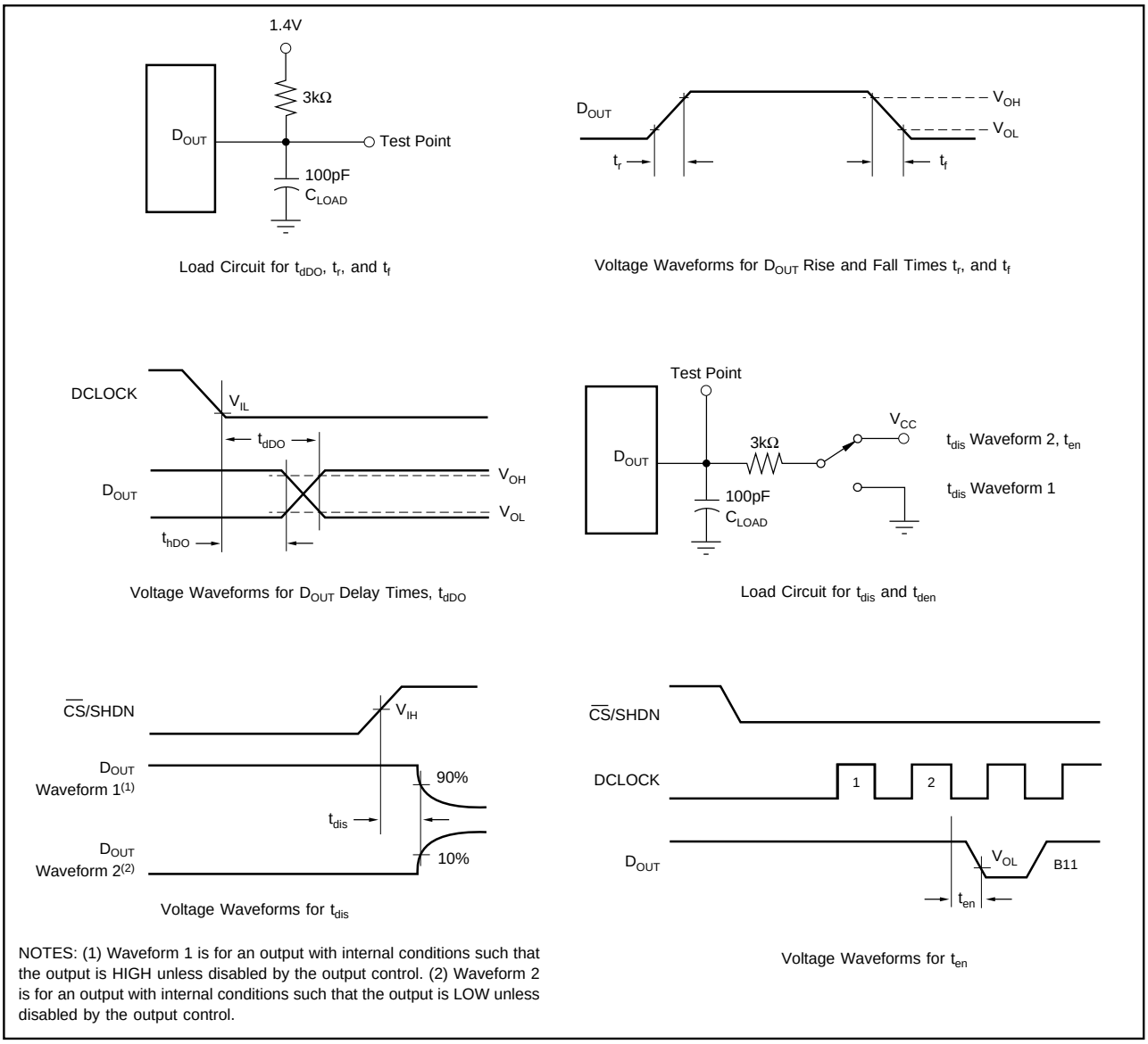


FIGURE 5. Timing Diagrams and Test Circuits for the Parameters in Table I.

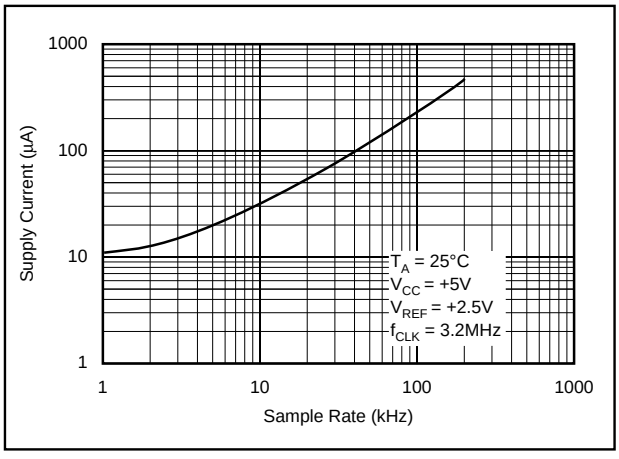


FIGURE 6. Maintaining f_{CLK} at the Highest Possible Rate Allows Supply Current to Drop Directly with Sample Rate.

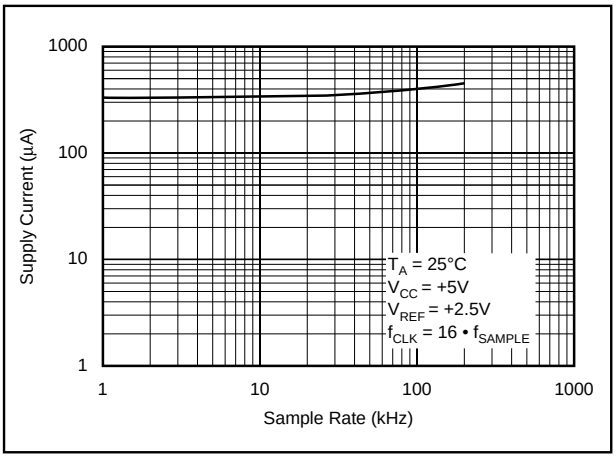


FIGURE 7. Scaling f_{CLK} Reduces Supply Current Only Slightly with Sample Rate.

There is an important distinction between the power down mode that is entered after a conversion is complete and the full power down mode which is enabled when $\overline{CS}$ is HIGH. While both power down the analog section, the digital section is powered down only when $\overline{CS}$ is HIGH. Thus, if $\overline{CS}$ is left LOW at the end of a conversion and the converter is continually clocked, the power consumption will not be as low as when $\overline{CS}$ is HIGH. See Figure 8 for more information.

By lowering the reference voltage, the ADS7817 requires less current to completely charge its internal capacitors on both the analog input and the reference input. This reduction in power dissipation should be weighed carefully against the resulting increase in noise, offset, and gain error as outlined in the Reference section.

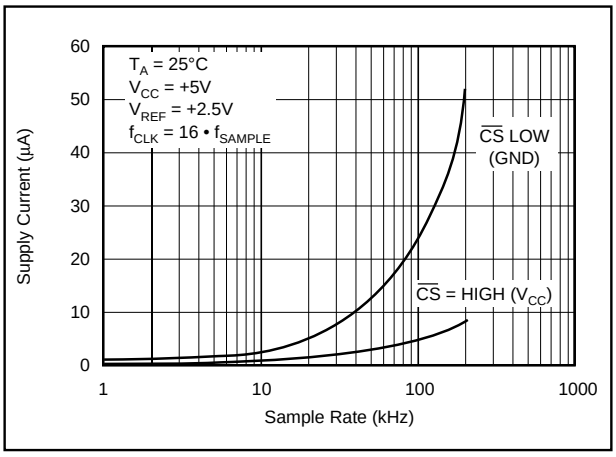


FIGURE 8. Shutdown Current is Considerably Lower with $\overline{CS}$ HIGH than when $\overline{CS}$ is LOW.

SHORT CYCLING

Another way of saving power is to utilize the $\overline{CS}$ signal to short cycle the conversion. Because the ADS7817 places the latest data bit on the D_{OUT} line as it is generated, the converter can easily be short cycled. This term means that the conversion can be terminated at any time. For example, if only 8-bits of the conversion result are needed, then the conversion can be terminated (by pulling $\overline{CS}$ HIGH) after the 8th bit has been clocked out.

This technique can be used to lower the power dissipation in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 12-bit conversion result may not be needed. If so, the conversion can be terminated after the first n-bits, where n might be as low as 3 or 4. This results in lower power dissipation in both the converter and the rest of the system, as they spend more time in the power down mode.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7817 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high. At 200kHz conversion rate, the ADS7817 makes a bit decision every 312ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 12-bit level all within one clock cycle.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an n-bit SAR converter, there are n “windows” in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high power devices, to name a few. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter’s DCLOCK signal—as the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this in mind, power to the ADS7817 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the ADS7817 package as possible. In addition, a 1 to 10µF capacitor and a 10Ω series resistor may be used to lowpass filter a noisy supply.

The reference should be similarly bypassed with a 0.1µF capacitor. Again, a series resistor and large capacitor can be used to lowpass filter the reference voltage. If the reference voltage originates from an op amp, be careful that the op-amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS7817 draws very little current from the reference on average, there are higher instantaneous current demands placed on the external reference circuitry.

Also, keep in mind that the ADS7817 offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference voltage is derived from the power supply. Any noise and ripple from the supply that is not rejected by the external reference circuitry will appear directly in the digital results. While high frequency noise can be filtered out as described in the previous paragraph, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin on the ADS7817 should be placed on a clean ground point. In many cases, this will be the “analog” ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power supply connection point. The ideal layout will include an analog ground plane for the converter and associated analog circuitry.

APPLICATION CIRCUITS

Figures 9, 10 and 11 show some typical applications circuits for the ADS7817. Figure 9 shows a low cost, low power circuit for basic data acquisition. Total power dissipation in the ADS7817 and reference circuitry is under 5mW over temperature, power supply variations, and at a 200kHz sample rate.

Figure 10 is a motor control application using three ISO130s to isolate the motor from the sensing system (three ADS7817s and a DSP56004). The ISO130 provides 10kV/µs (minimum) isolation-mode rejection, 85kHz large signal bandwidth, and a fixed gain of 8. The ADS7817's reference voltage is 1.2V and is derived from a REF1004-1.2. This gives the converter a full-scale input range of ±1.2V. Because of the gain of 8 in the ISO130, the current sense resistor should give a worst-case output voltage of less than ±150mV.

Figure 11 is a similar application that isolates the digital outputs of the three ADS7817s instead of the analog signal from the motor. Here, the reference voltage for the ADS7817 is 150mV, and the analog input of each ADS7817 is connected directly to the current sense resistor. By removing the ISO130 from the signal path, a greater signal-to-noise ratio is achieved in the sensing system. However, nine optical isolators are needed to isolate the A/D converters.

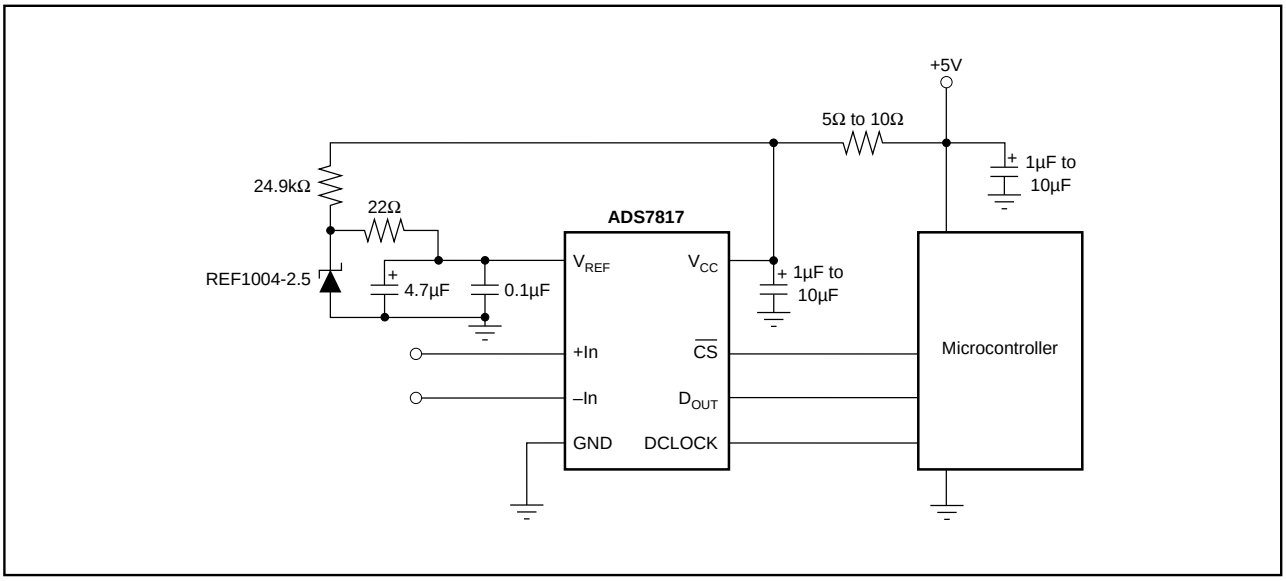


FIGURE 9. Low Cost, Low Power Data Acquisition System.

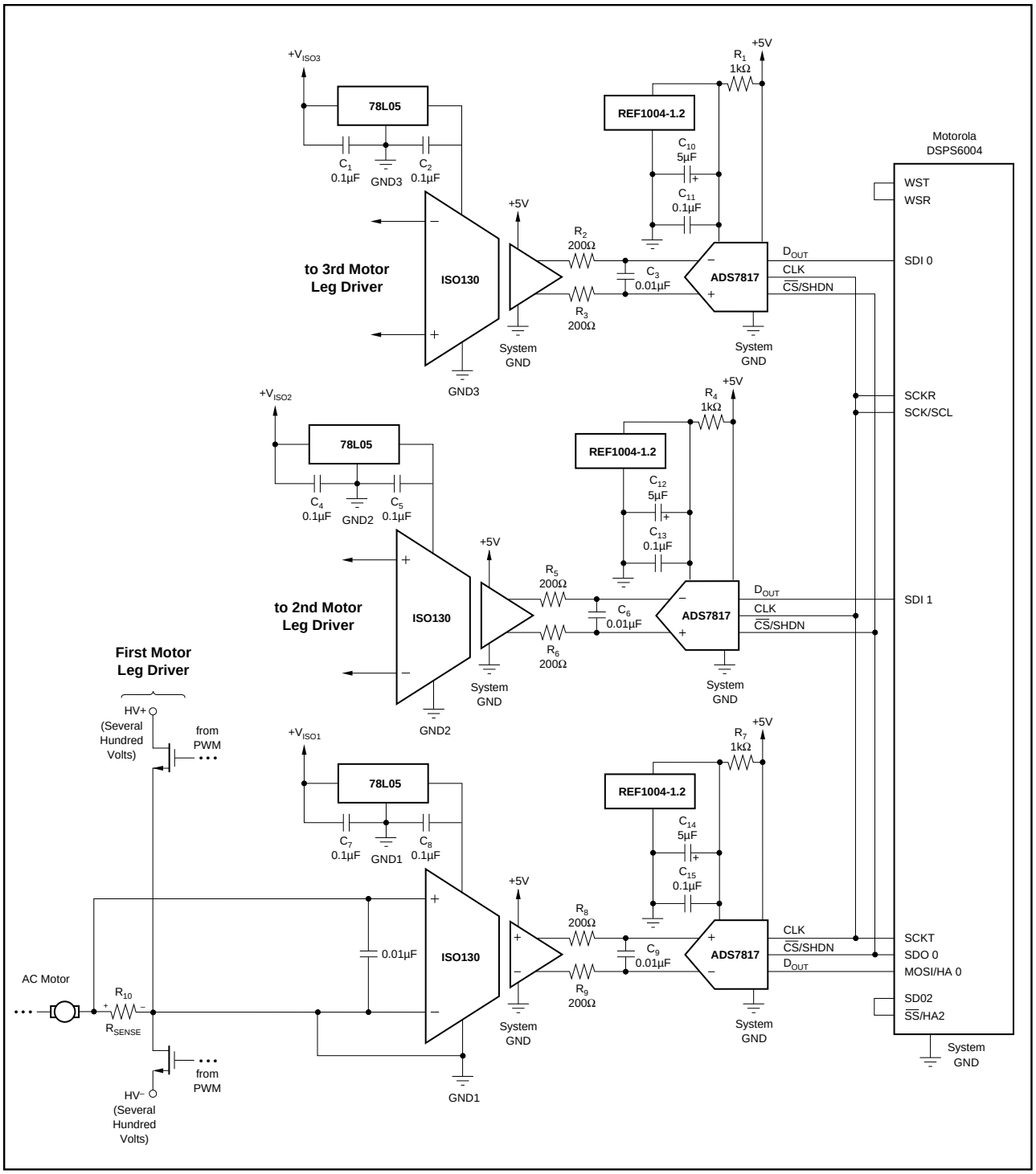


FIGURE 10. Motor Control Using the ISO130, ADS7817, and DSPS6004.

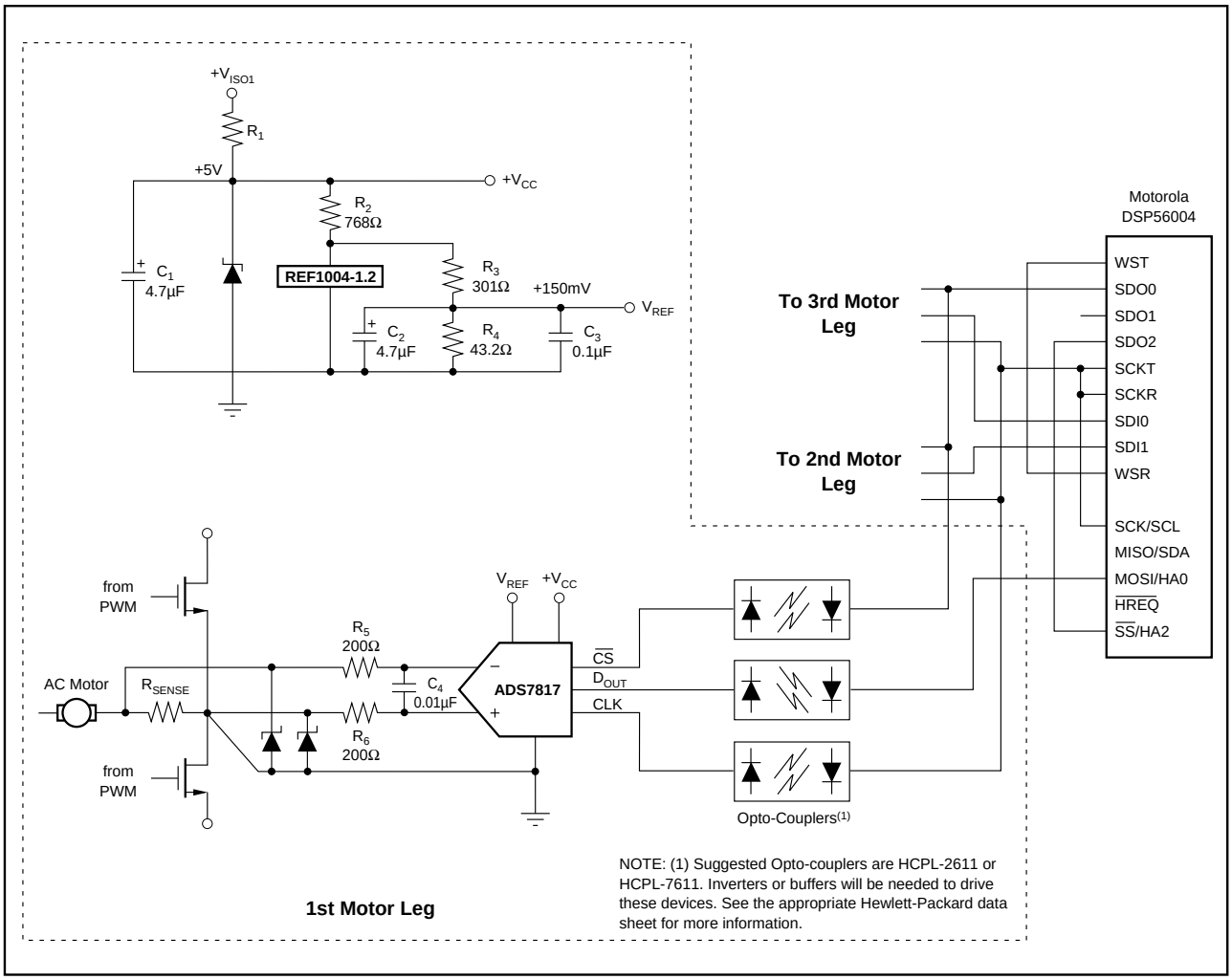


FIGURE 11. Motor Control Using an Isolated ADS7817.