

ADS7808

12-Bit 10 μ s Serial CMOS Sampling ANALOG-to-DIGITAL CONVERTER

FEATURES

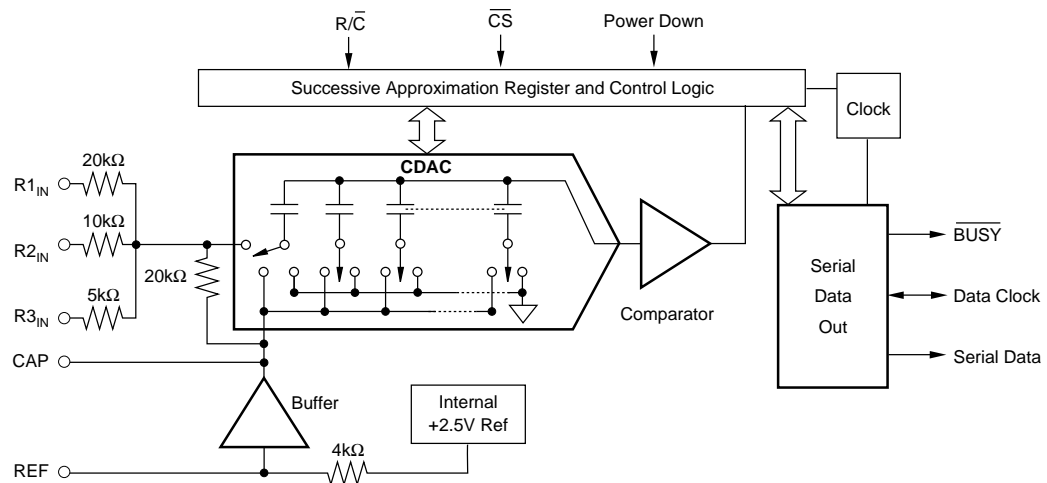
- 100kHz SAMPLING RATE
- 72dB SINAD WITH 45kHz INPUT
- $\pm 1/2$ LSB INL AND DNL
- SIX SPECIFIED INPUT RANGES
- SERIAL OUTPUT
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 16-BIT ADS7809
- USES INTERNAL OR EXTERNAL REFERENCE
- 100mW MAX POWER DISSIPATION
- 20-PIN 0.3" PLASTIC DIP AND SOIC
- SIMPLE DSP INTERFACE

DESCRIPTION

The ADS7808 is a complete 12-bit sampling analog-to-digital using state-of-the-art CMOS structures. It contains a 12-bit capacitor-based SAR A/D with S/H, reference, clock, and a serial data interface. Data can be output using the internal clock, or can be synchronized to an external data clock. The ADS7808 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7808 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including $\pm 10V$ and $0V$ to $5V$, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The 20-pin ADS7808 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial $-40^{\circ}C$ to $+85^{\circ}C$ range.



SPECIFICATIONS

ELECTRICAL

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $f_S = 100\text{kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7808P, U			ADS7808PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT Voltage Ranges Impedance Capacitance				$\pm 10\text{V}$, 0V to 5V , etc. (See Table I) See Table I				pF
THROUGHPUT SPEED Conversion Time Complete Cycle Throughput Rate	Acquire and Convert		5.7	8 10		*	*	μs μs kHz
DC ACCURACY Integral Linearity Error Differential Linearity Error No Missing Codes Transition Noise ⁽²⁾ Full Scale Error ^(3,4) Full Scale Error Drift Full Scale Error ^(3,4) Full Scale Error Drift Bipolar Zero Error ⁽³⁾ Bipolar Zero Error Drift Unipolar Zero Error ⁽³⁾ Unipolar Zero Error Drift Recovery to Rated Accuracy after Power Down Power Supply Sensitivity ($V_{\text{DIG}} = V_{\text{ANA}} = V_{\text{D}}$)	Ext. 2.5000V Ref Ext. 2.5000V Ref Bipolar Ranges Bipolar Ranges 0V to 10V Range 0V to 4V Range 0V to 5V Range Unipolar Ranges 1 μF Capacitor to CAP +4.75V < V_{D} < +5.25V		Guaranteed 0.1	± 0.9 ± 0.9 ± 0.5 ± 7 ± 2 ± 2 ± 5 ± 3 ± 3 ± 2 1		*	*	LSB ⁽¹⁾ LSB LSB % ppm/ $^\circ\text{C}$ % ppm/ $^\circ\text{C}$ mV ppm/ $^\circ\text{C}$ mV mV mV ppm/ $^\circ\text{C}$ ms LSB
AC ACCURACY Spurious-Free Dynamic Range Total Harmonic Distortion Signal-to-(Noise+Distortion) Signal-to-Noise Full-Power Bandwidth ⁽⁶⁾	$f_{\text{IN}} = 45\text{kHz}$ $f_{\text{IN}} = 45\text{kHz}$ $f_{\text{IN}} = 45\text{kHz}$ $f_{\text{IN}} = 45\text{kHz}$	80	90 -90	-80	*	*	*	dB ⁽⁵⁾ dB dB dB kHz
SAMPLING DYNAMICS Aperture Delay Aperture Jitter Transient Response Overvoltage Recovery ⁽⁷⁾	FS Step		40	Sufficient to meet AC specs 2		*	*	ns ns μs ns
REFERENCE Internal Reference Voltage Internal Reference Source Current (Must use external buffer) External Reference Voltage Range for Specified Linearity External Reference Current Drain	No Load Ext. 2.5000V Ref	2.48	2.5 1	2.52	*	*	*	V μA V μA
DIGITAL INPUTS Logic Levels V_{IL} V_{IH} I_{IL} I_{IH}	$V_{\text{IL}} = 0\text{V}$ $V_{\text{IH}} = 5\text{V}$	-0.3 +2.0		+0.8 $V_{\text{D}} + 0.3\text{V}$ ± 10 ± 10	*	*	*	V V μA μA

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SPECIFICATIONS (CONT)

ELECTRICAL

At $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $f_S = 100\text{kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$, using internal reference and fixed resistors shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7808P/U			ADS7808PB/UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL OUTPUTS								
Data Format								
Data Coding								
Pipeline Delay								
Data Clock								
Internal	EXT/ $\overline{\text{INT}}$ LOW					*		MHz
(Output Only When Transmitting Data)								
External	EXT/ $\overline{\text{INT}}$ HIGH	0.1		10	*		*	MHz
(Can Run Continually)								
V_{OL}	$I_{\text{SINK}} = 1.6\text{mA}$			+0.4			*	V
V_{OH}	$I_{\text{SOURCE}} = 500\mu\text{A}$	+4			*			V
Leakage Current	High-Z State, $V_{\text{OUT}} = 0\text{V}$ to V_{DIG}			± 5			*	μA
Output Capacitance	High-Z State			15			15	pF
POWER SUPPLIES								
Specified Performance	Must be $\leq V_{\text{ANA}}$	+4.75	+5	+5.25	*	*	*	V
V_{DIG}	+4.75	+5	+5.25	*	*	*	V	
V_{ANA}		0.3			*		mA	
I_{DIG}		16			*		mA	
I_{ANA}				100		*	*	mW
Power Dissipation: PWRD LOW	$V_{\text{DIG}} = V_{\text{ANA}} = 5\text{V}$, $f_S = 100\text{kHz}$							μW
PWRD HIGH				50				
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	$^\circ\text{C}$
Derated Performance		-55		+125	*		*	$^\circ\text{C}$
Storage		-65		+150	*		*	$^\circ\text{C}$
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		$^\circ\text{C/W}$
SOIC			75			*		$^\circ\text{C/W}$

NOTES: (1) LSB means Least Significant Bit. For the $\pm 10\text{V}$ input range, one LSB is 4.88mV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors in Figure 4. Adjustable to zero with external potentiometer. (4) For bipolar input ranges, full scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error. (5) All specifications in dB are referred to a full-scale $\pm 10\text{V}$ input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to (Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R_{1\text{IN}}$	$\pm 25\text{V}$
$R_{2\text{IN}}$	$\pm 25\text{V}$
$R_{3\text{IN}}$	$\pm 25\text{V}$
CAP	$V_{\text{ANA}} + 0.3\text{V}$ to AGND2 -0.3V
REF	Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND2	$\pm 0.3\text{V}$
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3
V_{DIG}	7V
Digital Inputs	-0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165 $^\circ\text{C}$
Internal Power Dissipation	700mW
Lead Temperature (soldering, 10s)	+300 $^\circ\text{C}$

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
ADS7808P	20-Pin Plastic DIP	222
ADS7808PB	20-Pin Plastic DIP	222
ADS7808U	20-Pin SOIC	221
ADS7808UB	20-Pin SOIC	221

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

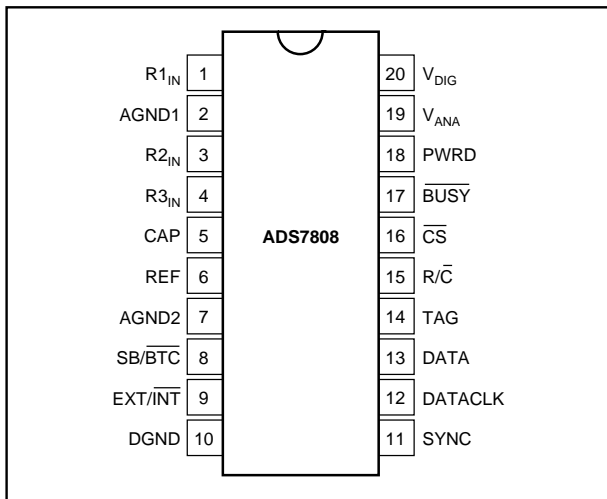
ORDERING INFORMATION

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO(dB)	SPECIFICATION TEMPERATURE RANGE ($^\circ\text{C}$)	PACKAGE
ADS7808P	± 0.9	70	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$	20-Pin Plastic DIP
ADS7808PB	± 0.45	72	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$	20-Pin Plastic DIP
ADS7808U	± 0.9	70	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$	20-Pin SOIC
ADS7808UB	± 0.45	72	-40 $^\circ\text{C}$ to +85 $^\circ\text{C}$	20-Pin SOIC

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	R _{1IN}	Analog Input. See Table I and Figure 4 for input range connections.
2	AGND1	Analog Ground. Used internally as ground reference point. Minimal current flow.
3	R _{2IN}	Analog Input. See Table I and Figure 4 for input range connections.
4	R _{3IN}	Analog Input. See Table I and Figure 4 for input range connections.
5	CAP	Reference Buffer Capacitor. 2.2μF Tantalum to ground.
6	REF	Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2μF Tantalum capacitor.
7	AGND2	Analog Ground.
8	SB/ $\overline{\text{BTC}}$	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's complement format.
9	EXT/ $\overline{\text{INT}}$	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 12 clock pulses output on DATACLK.
10	DGND	Digital Ground.
11	SYNC	Synch Output. If EXT/ $\overline{\text{INT}}$ is HIGH, either a rising edge on R/ $\overline{\text{C}}$ with $\overline{\text{CS}}$ LOW or a falling edge on $\overline{\text{CS}}$ with R/ $\overline{\text{C}}$ HIGH will output a pulse on SYNC synchronized to the external DATACLK.
12	DATACLK	Either an input or an output depending on the EXT/ $\overline{\text{INT}}$ level. Output data will be synchronized to this clock. If EXT/ $\overline{\text{INT}}$ is LOW, DATACLK will transmit 12 pulses after each conversion, and then remain LOW between conversions.
13	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/ $\overline{\text{BTC}}$. In the external clock mode, after 12-bits of data, the ADS7808 will output the level input on TAG as long as $\overline{\text{CS}}$ is LOW and R/ $\overline{\text{C}}$ is HIGH (see Figure 3.) If EXT/ $\overline{\text{INT}}$ is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
14	TAG	Tag Input for use in external clock mode. If EXT/ $\overline{\text{INT}}$ is HIGH, digital data input on TAG will be output on DATA with a delay of 12 DATACLK pulses as long as $\overline{\text{CS}}$ is LOW and R/ $\overline{\text{C}}$ is HIGH. See Figure 3.
15	R/ $\overline{\text{C}}$	Read/Convert Input. With $\overline{\text{CS}}$ LOW, a falling edge on R/ $\overline{\text{C}}$ puts the internal sample/hold into the hold state and starts a conversion. When EXT/ $\overline{\text{INT}}$ is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/ $\overline{\text{INT}}$ is HIGH, a rising edge on R/ $\overline{\text{C}}$ with $\overline{\text{CS}}$ LOW, or a falling edge on $\overline{\text{CS}}$ with R/ $\overline{\text{C}}$ HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
16	$\overline{\text{CS}}$	Chip Select. Internally OR'ed with R/ $\overline{\text{C}}$.
17	$\overline{\text{BUSY}}$	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. $\overline{\text{CS}}$ or R/ $\overline{\text{C}}$ must be HIGH when $\overline{\text{BUSY}}$ rises, or another conversion will start without time for signal acquisition.
18	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
19	V _{ANA}	Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1μF ceramic and 10μF Tantalum capacitors.
20	V _{DIG}	Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be $\leq V_{\text{ANA}}$.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT R _{1IN} VIA 200Ω TO	CONNECT R _{2IN} VIA 100Ω TO	CONNECT R _{3IN} TO	IMPEDANCE
±10V	V _{IN}	AGND	CAP	22.9kΩ
±5V	AGND	V _{IN}	CAP	13.3kΩ
±3.33	V _{IN}	V _{IN}	CAP	10.7kΩ
0V to 10V	AGND	V _{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V _{IN}	10.0kΩ
0V to 4V	V _{IN}	AGND	V _{IN}	10.7kΩ

TABLE I. Input Range Connections. See Figure 4 for complete information.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		4500	ns
t_2	$\overline{\text{BUSY}}$ Delay			65	ns
t_3	$\overline{\text{BUSY}}$ LOW			8	μs
t_4	$\overline{\text{BUSY}}$ Delay after End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		5.7	8	μs
t_7	Acquisition Time			2	μs
$t_6 + t_7$	Throughput Time		9	10	μs
t_8	$\text{R}/\overline{\text{C}}$ LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid after DATACLK LOW Delay	100	125		ns
t_{12}	External DATACLK Period	100			ns
t_{13}	External DATACLK HIGH	20			ns
t_{14}	External DATACLK LOW	30			ns
t_{15}	DATACLK HIGH Setup Time	20	$t_{12} + 5$		ns
t_{16}	$\text{R}/\overline{\text{C}}$ to $\overline{\text{CS}}$ Setup Time	10			ns
t_{17}	SYNC Delay After DATACLK HIGH	15	35		ns
t_{18}	Data Valid Delay	25	55		ns
t_{19}	$\overline{\text{CS}}$ to Rising Edge Delay	25			ns
t_{20}	Data Available after $\overline{\text{CS}}$ LOW	4.5			μs

TABLE II. Conversion and Data Timing $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

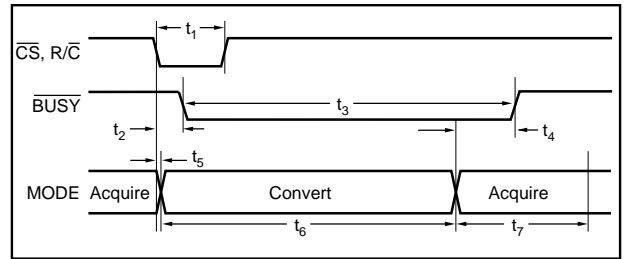


FIGURE 1. Basic Conversion Timing.

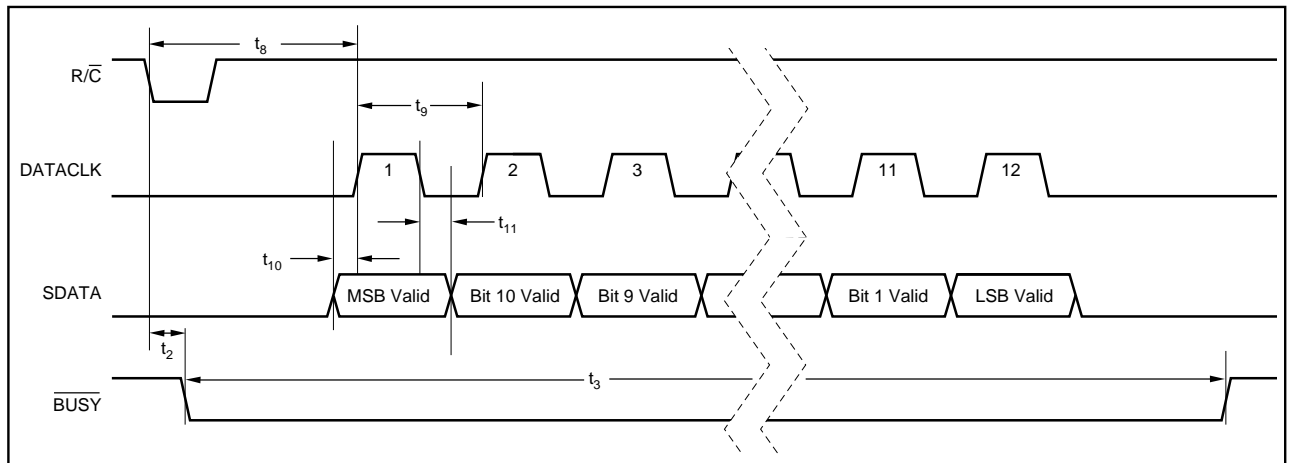


FIGURE 2. Serial Data Timing Using Internal Clock. ($\overline{\text{CS}}$, $\overline{\text{EXT/INT}}$ and $\overline{\text{TAG}}$ Tied LOW.)

SPECIFIC FUNCTION	\overline{CS}	R/\overline{C}	\overline{BUSY}	EXT/\overline{INT}	DATACLK	PWRD	SB/\overline{BTC}	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1>0	0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
	0	1>0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n-1" clocked out on DATA synchronized to 12 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1>0	0	1	1	Input	0	x	Initiates conversion "n".
	0	1>0	1	1	Input	0	x	Initiates conversion "n".
	1>0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.
	1>0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n-1" clocked out synchronized to external DATACLK. ⁽¹⁾ Conversion "n" in process.
Incorrect Conversions	0	0	0>1	x	x	0	x	\overline{CS} or R/\overline{C} must be HIGH or a new conversion will be initiated without time for acquisition.
	0	0>1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n-1" clocked out synchronized to external DATACLK. ⁽¹⁾ Conversion "n" in process.
Power Down	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

Table III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/ \overline{BTC} LOW)		STRAIGHT BINARY (SB/ \overline{BTC} HIGH)	
							HEX BINARY CODE	CODE	HEX BINARY CODE	CODE
Full-Scale Range	± 10	± 5	$\pm 3.33V$	0V to 5V	0V to 10V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	2.44mV	1.63mV	1.22mV	2.44mV	0.98mV				
+Full Scale (FS - 1LSB)	9.99512V	4.99756V	3.33171V	4.99878V	9.99756V	3.99902V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0V	0V	0V	2.5V	5V	2V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	-4.88mV	-2.44mV	-1.63mV	2.49878V	4.99756V	1.99902V	1111 1111 1111	FFF	0111 1111 1111	7FF
-Full Scale	-10V	-5V	-3.33333V	0V	0V	0V	1000 0000 0000	800	0000 0000 0000	000

Table IV. Output Codes and Ideal Input Voltages.

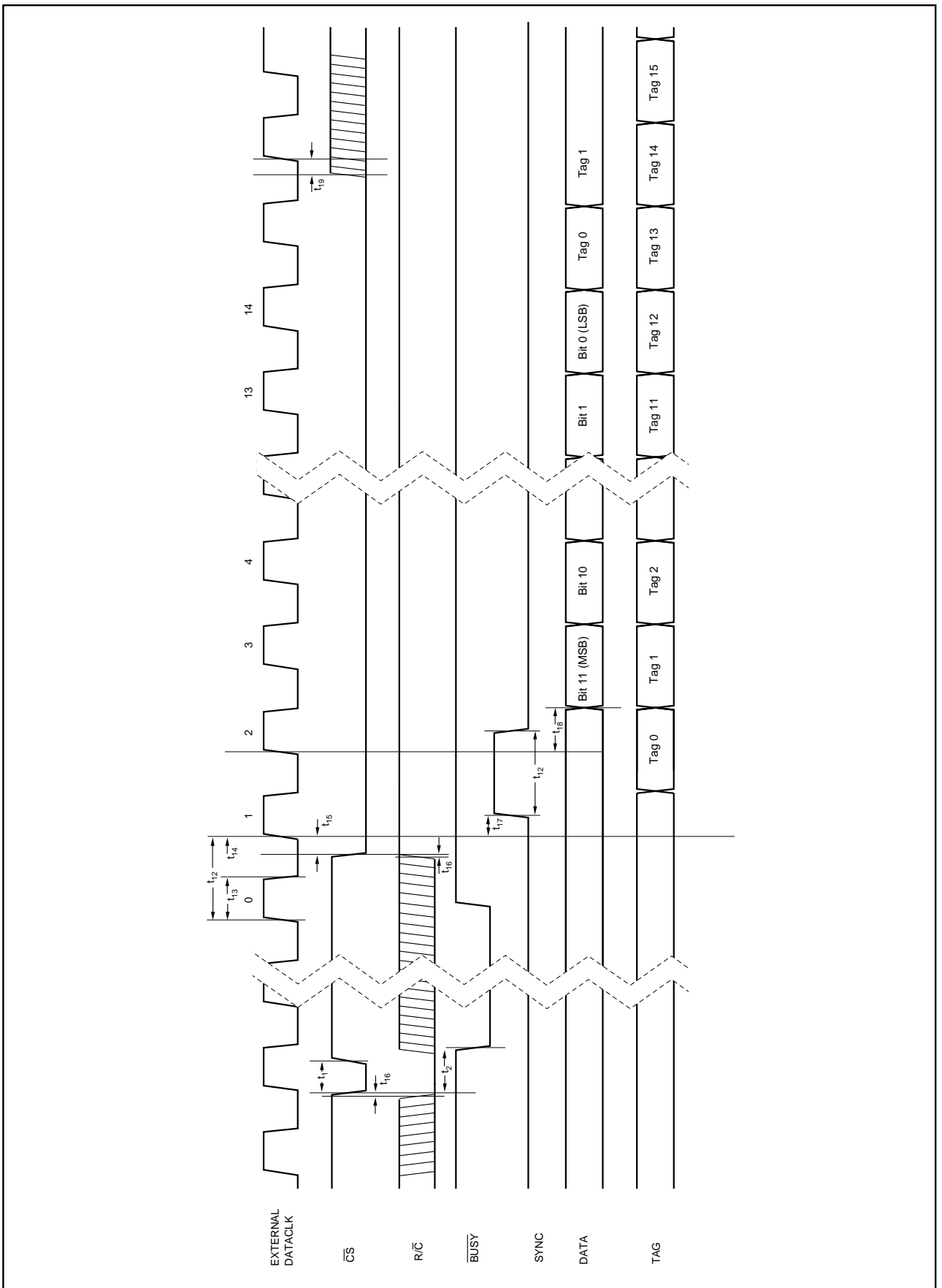


FIGURE 3a. Conversion and Read Timing with External Clock. (EXT/INT Tied HIGH). Read After Conversion.

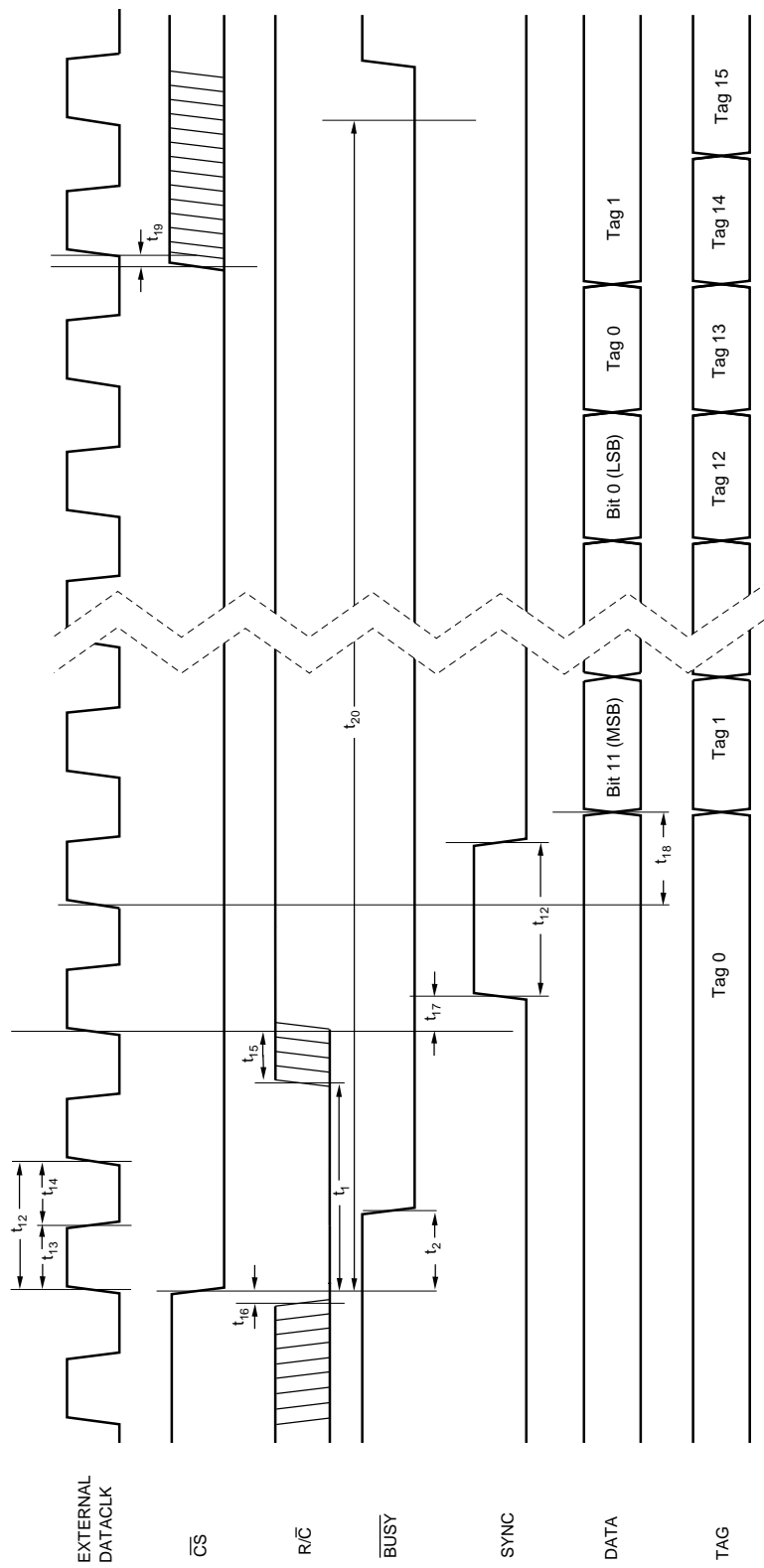


FIGURE 3b. Conversion and Read Timing with External Clock. (EXT/INT Tied HIGH.) Read During Conversion (Previous Conversion Results).

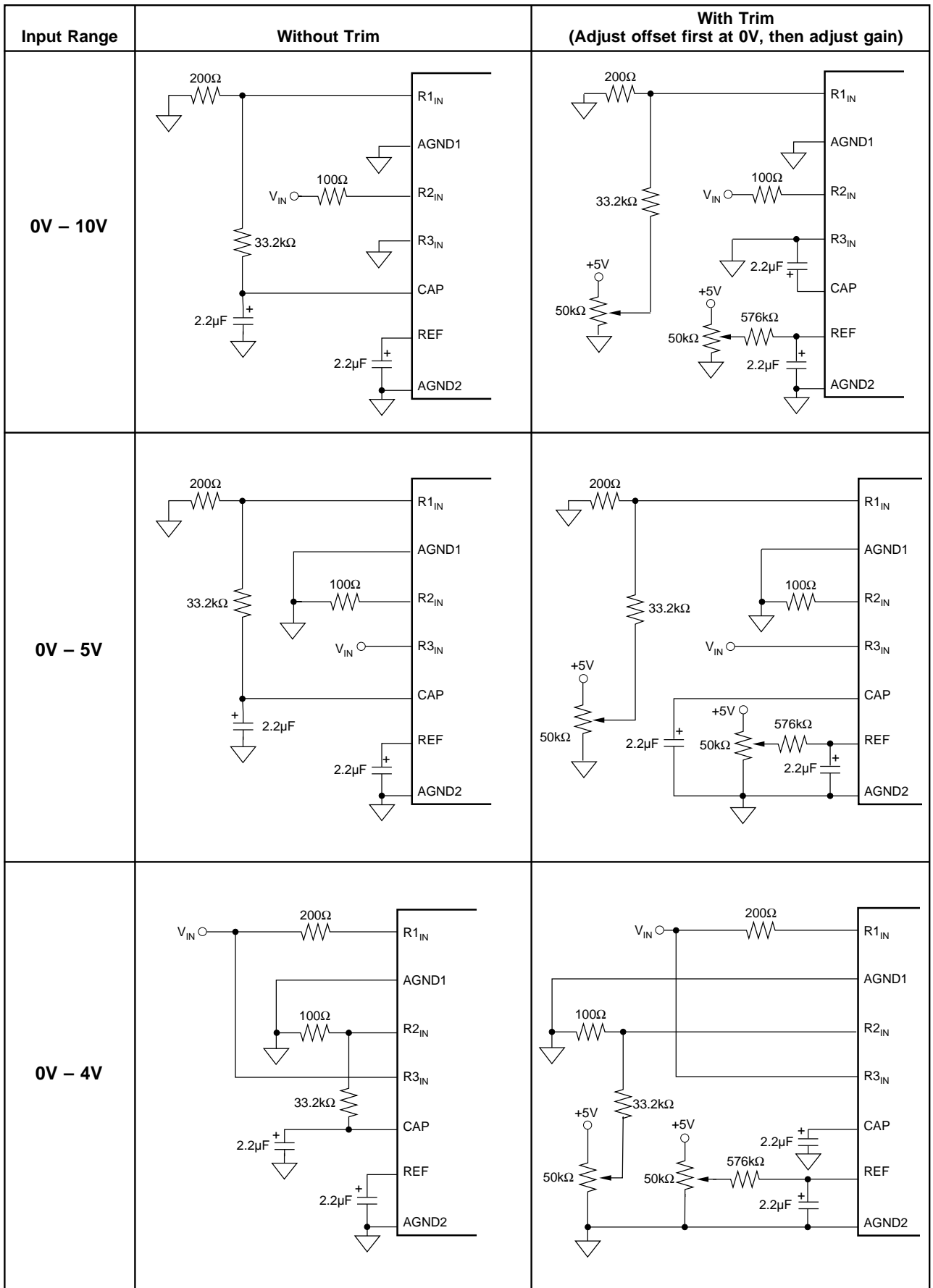


FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

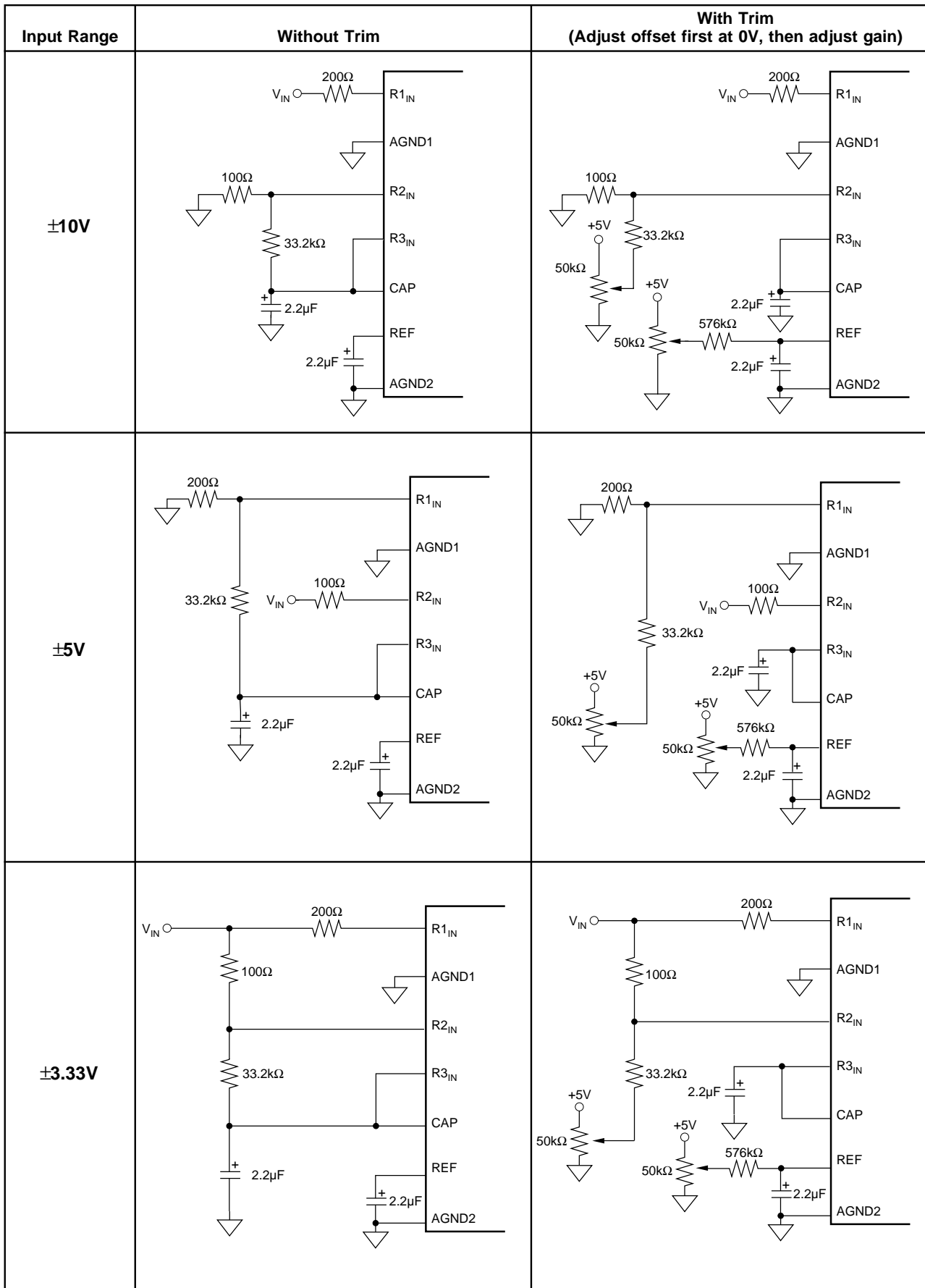


FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.