

**ADC701
SHC702**

16-Bit 512kHz SAMPLING A/D CONVERTER SYSTEM

FEATURES

- **CONVERSION RATE:** to 512kHz Over Temp
- **NO MISSING CODES AT 16 BITS**
- **SPURIOUS-FREE DYNAMIC RANGE:** 107dB
- **LOW NONLINEARITY:** $\pm 0.0015\%$
- **SELECTABLE INPUT RANGES:** $\pm 5V$, $\pm 10V$, 0 to +10V, 0 to +5V, -10V to 0
- **LOW POWER DISSIPATION:** 2.8W Typical Including Sample/Hold
- **METAL AND CERAMIC DIP PACKAGES**

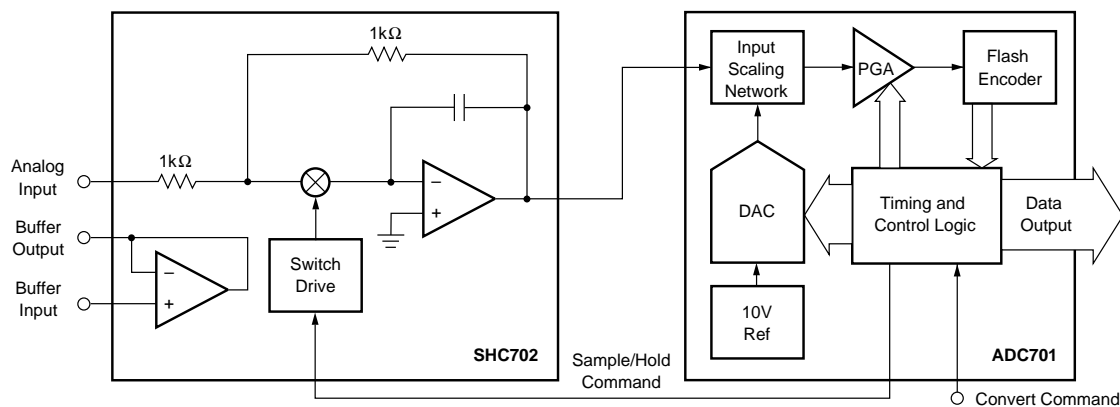
APPLICATIONS

- **MEDICAL IMAGING**
- **SONAR**
- **PROFESSIONAL AUDIO RECORDING**
- **AUTOMATIC TEST EQUIPMENT**
- **HIGH PERFORMANCE FFT SPECTRUM ANALYSIS**
- **ULTRASOUND SIGNAL PROCESSING**
- **HIGH SPEED DATA ACQUISITION**
- **REPLACES DISCRETE MODULAR ADCs**

DESCRIPTION

The ADC701 is a very high speed 16-bit analog-to-digital converter based on a three-step subranging architecture. Outstanding dynamic performance is achieved with the SHC702 companion sample/hold amplifier. Both devices use hybrid construction for applications where reliability, small size, and low power consumption are especially important.

Excellent linearity and stability are assured through use of a new ultra-precise monolithic D/A converter and a low-drift reference circuit. Custom monolithic op amps provide very high bandwidth and low noise in all sections of the analog signal path. Logic is CMOS/TTL compatible and is designed for maximum flexibility.



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Internet: <http://www.burr-brown.com/> • FAX Line: (800) 548-6133 (US/Canada Only) • Cable: BURCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL (ADC701 ONLY)

At $T_A = +25^\circ\text{C}$, 500kHz sampling rate, $\pm V_{CC} = \pm 15\text{V}$, $\pm V_{DD1} = \pm 5\text{V}$, $+V_{DD2} = +5\text{V}$, and five-minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	ADC701JH			ADC701KH			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
INPUTS								
ANALOG								
Voltage Ranges	Unipolar Bipolar			0 to +5, 0 to +10, -10 to 0				V V
Resistance	0 to +5V Range 0 to +10V, -10 to 0, $\pm 5\text{V}$ Ranges	2.45 4.9	2.5 5	2.55 5.1	*	*	*	k Ω k Ω
Capacitance	$\pm 10\text{V}$ Range All Ranges	9.8	10 5	10.2	*	*	*	k Ω pF
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Convert Command	Start Conversion			Rising Edge				
Pulse Width	$t = \text{Conversion Period}$	50		$t - 50$	*		*	ns
TRANSFER CHARACTERISTICS								
ACCURACY								
Gain Error ⁽¹⁾	0 to +10V Range $\pm 10\text{V}$ Range		± 0.03 ± 0.03	± 0.1 ± 0.1		*	*	% %
Power Supply Sensitivity of Gain	All Ranges, All Supplies		± 0.005	± 0.1		*	*	%/V
Input Offset Error ⁽¹⁾	0 to +10V Range $\pm 10\text{V}$ Range		± 1 ± 5	± 3 ± 10		*	*	mV mV
Power Supply Sensitivity of Offset	All Ranges, All Supplies		± 0.006	± 0.1		*	*	%FSR/V
Integral Linearity Error ⁽²⁾			± 0.002	± 0.003		± 0.0012	*	%FSR ⁽³⁾
Differential Linearity Error ⁽²⁾			± 0.0006	± 0.0012		*	*	%FSR
No Missing Codes			Guaranteed			Guaranteed		
Noise	$R_{\text{SOURCE}} \leq 50\Omega$		0.6			*		LSB rms
CONVERSION CHARACTERISTICS								
Sample Rate	Unadjusted	DC		512	*		*	kHz
Conversion Time ⁽⁴⁾	Unadjusted		1.45	1.5		*	*	μs
OUTPUTS								
DIGITAL								
Logic Family				TTL-Compatible CMOS				
Data Coding	Unipolar Ranges Bipolar Ranges			Straight Binary Offset Binary				
Logic "0" Levels (V_{OL})	$I_{OL} \leq 3.2\text{mA}$		0.1	0.4		*	*	V
Logic "1" Levels (V_{OH})	$I_{OH} \leq 80\mu\text{A}$	4	4.9			*	*	V
Data Valid Setup Time Before Strobe	Both Edges	28	37			*	*	ns
INTERNAL REFERENCE								
Voltage	$R_{\text{LOAD}} \geq 5\text{k}\Omega$	+9.995	+10.000	+10.005	*	*	*	V
Current Available to External Loads		2	5		*	*	*	mA
POWER SUPPLY REQUIREMENTS								
Supply Voltages: $+V_{CC}$	Operating	+14.25	+15	+15.75	*	*	*	V
$-V_{CC}$		-14.25	-15	-15.75	*	*	*	V
$+V_{DD1}$		+4.75	+5	+5.25	*	*	*	V
$-V_{DD1}$		-4.25	-5	-6	*	*	*	V
$+V_{DD2}$		+4.25	+5	+5.25	*	*	*	V
Supply Currents: $+I_{CC}$	Operating		25	30	*	*	*	mA
$-I_{CC}$			33	45	*	*	*	mA
$+I_{DD1}$			45	55	*	*	*	mA
$-I_{DD1}$			37	50	*	*	*	mA
$+I_{DD2}$			133	150	*	*	*	mA
Power Dissipation	Nominal Voltages		1.95	2.3		*	*	W
PERFORMANCE OVER TEMPERATURE								
Specification Temperature Range	T_A Min to T_A Max	+15		+55	0		+70	$^\circ\text{C}$
Gain Error	All Ranges		± 10	± 15		*	*	ppm/ $^\circ\text{C}$
Input Offset Error	All Unipolar Ranges All Bipolar Ranges		± 1 ± 1	± 5 ± 5		*	*	ppm FSR/ $^\circ\text{C}$ ppm FSR/ $^\circ\text{C}$
Integral Linearity Error ⁽²⁾			± 0.2			*	± 0.5	ppm/ $^\circ\text{C}$
Differential Linearity Error ⁽²⁾			± 0.05			*	± 0.3	ppm/ $^\circ\text{C}$
No Missing Codes			Typical			Guaranteed		
Reference Output Drift			± 3			*	*	ppm/ $^\circ\text{C}$
Drift of Conversion Time	Unadjusted		+3	+4		*	*	ns/ $^\circ\text{C}$
Sample Rate	Unadjusted	DC		512	*		*	kHz

* Same specifications as ADC701JH.

SPECIFICATIONS

ELECTRICAL (SHC702 ONLY)

At $T_A = +25^\circ\text{C}$, 500kHz sampling rate, $\pm V_{CC} = \pm 15\text{V}$, $+V_{DD1} = +5\text{V}$, and five-minute warmup in a convection environment, unless otherwise noted.

PARAMETER	CONDITIONS	SHC702JM			UNITS
		MIN	TYP	MAX	
INPUTS (Without Input Buffer)					
ANALOG					
Voltage Range		± 10.25	± 11		V
Resistance		0.98	1	1.02	k Ω
Capacitance			3		pF
DIGITAL					
Logic Family			LSTTL		
Input Loading			2		LSTTL Loads
TRANSFER CHARACTERISTICS					
ACCURACY					
Gain	$R_{SOURCE} = 0\Omega$		-1		V/V
Gain Error	$R_{SOURCE} = 0\Omega$		± 0.02	± 0.1	%
Linearity Error	Sample Mode		± 0.0003		%FSR
Offset Error	Sample Mode		± 0.5	± 3	mV
Charge Offset (Pedestal) Error	Sample/Hold Mode, $R_{SOURCE} \leq 50\Omega$		± 0.5	± 5	mV
Droop Rate	Hold Mode		± 0.2	± 2	$\mu\text{V}/\mu\text{s}$
Dynamic Nonlinearity	Sample/Hold Mode		± 0.0005		%FSR
Power Supply Sensitivity	Offset Plus Charge Offset, All Supplies		± 0.003		%FSR/V
DYNAMIC CHARACTERISTICS					
Acquisition Time	10V Step to $\pm 150\mu\text{V}$		600		ns
	5V Step to $\pm 150\mu\text{V}$		500		ns
Sample-to-Hold Settling Time ⁽⁵⁾	to $\pm 150\mu\text{V}$		120		ns
Aperture Delay Time			20		ns
Aperture Uncertainty (Jitter)			10	25	ps rms
Slew Rate			150		V/ μs
Small Signal Bandwidth	$V_{IN} = \pm 1\text{V}$		3.1		MHz
Full-Power Bandwidth	$V_{IN} = \pm 10\text{V}$		2		MHz
Feedthrough Rejection	Hold Mode, 10Vp-p Square Wave Input		0.001		%
OUTPUT					
Voltage Range	$R_{LOAD} \geq 1\text{k}\Omega$	± 10.25	± 11		V
Output Current		± 40			mA
Short Circuit Protection	$R_{LOAD} = 0\Omega$		Indefinite		
Output Impedance	DC		0.01	0.1	Ω
INPUT BUFFER CHARACTERISTICS					
INPUT					
Impedance			$10^{13} 3$		ΩpF
Bias Current	$V_{IN} = \pm 10\text{V}$		± 2	± 15	pA
Offset Voltage	$R_{SOURCE} \leq 10\text{k}\Omega$		± 0.3	± 1.5	mV
Voltage Range		± 10.25	± 11		V
DYNAMIC CHARACTERISTICS					
Slew Rate		20	35		V/ μs
Full-Power Bandwidth	$V_{IN} = \pm 10\text{V}$		570		kHz
Settling Time	10V Step to $\pm 150\mu\text{V}$		1.7		μs
OUTPUT					
Output Current		± 15	± 20		mA
Short Circuit Protection	$R_{LOAD} = 0\Omega$		Indefinite		
POWER SUPPLY REQUIREMENTS					
Voltage: $+V_{CC}$	Operating	+13.5	+15	+16.5	V
$-V_{CC}$		-13.5	-15	-16.5	V
$+V_{DD1}$		+4.75	+5	+5.25	V
Current: $+I_{CC}$	Operating		33	40	mA
$-I_{CC}$			18	25	mA
$+I_{DD1}$			5	10	mA
Power Dissipation	Nominal Voltages		790	950	mW
PERFORMANCE OVER TEMPERATURE					
Specification Temperature Range	T_A Min to T_A Max	0		+70	$^\circ\text{C}$
Sample/Hold Gain Error	$R_{SOURCE} = 0\Omega$		± 1	± 5	ppm/ $^\circ\text{C}$
Sample/Hold Offset Error	$R_{SOURCE} \leq 50\Omega$		± 10	± 30	$\mu\text{V}/^\circ\text{C}$
Sample/Hold Charge Offset Error	$R_{SOURCE} \leq 50\Omega$		± 10	± 80	$\mu\text{V}/^\circ\text{C}$
Droop Rate				± 50	$\mu\text{V}/\mu\text{s}$
Buffer Offset Error	$R_{SOURCE} \leq 10\text{k}\Omega$		± 3	± 15	$\mu\text{V}/^\circ\text{C}$

NOTES: (1) Adjustable to zero. Tested and guaranteed for 0 to +10V and $\pm 10\text{V}$ ranges only. (2) Peak-to-peak based on 99.9% of all codes. (3) FSR means full-scale range and depends on the input range selected. (4) ADC conversion time is defined as the time that the Sample/Hold must remain in the Hold mode; i.e., the duration of the Sample/Hold command. This time must be added to the Sample/Hold acquisition time to obtain the total system throughput time. (5) Given for reference only — this time overlaps with the ADC701 conversion time and does not affect system throughput rate.

SPECIFICATIONS

ELECTRICAL (COMBINED ADC701/SHC702)

At $T_A = +25^\circ\text{C}$, 500kHz sampling rate, $\pm V_{CC} = \pm 15\text{V}$, $\pm V_{DD1} = \pm 5\text{V}$, $+V_{DD2} = +5\text{V}$, and five-minute warmup in a convection environment, $\pm 5\text{V}$ input range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Sample Rate	Unadjusted	DC		512	kHz
Dynamic Nonlinearity			± 0.002		%FSR
Total Harmonic Distortion (THD)	$f_{IN} = 20\text{kHz}$ (-0.3dB)		-103		dB
	$f_{IN} = 199\text{kHz}$ (-0.2dB)		-82		dB
Spurious-Free Dynamic Range (SFDR)	$f_{IN} = 20\text{kHz}$ (-0.3dB)		107		dB
	$f_{IN} = 199\text{kHz}$ (-12dB)		94		dB
Two-Tone Intermodulation Distortion (IMD)	$f_1 = 195\text{kHz}$ (-6.5dB), $f_2 = 200\text{kHz}$ (-6.5dB)		-81		dBC
	$f_1 = 195\text{kHz}$ (-12.5dB), $f_2 = 200\text{kHz}$ (-12.5dB)		-86		dBC
Signal-to-Noise Ratio (SNR)	$f_{IN} = 5\text{kHz}$ (-0.5dB)		93		dB
Total Power Dissipation	Operating		2.8	3.25	W

ADC701 PIN ASSIGNMENTS

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Bit 1/9 (Bit 1 = MSB)	40	$-V_{DD1}$ (-5V) Analog
2	Bit 2/10	39	Common (Analog)
3	Bit 3/11	38	$+V_{DD1}$ ($+5\text{V}$) Analog
4	Bit 4/12	37	Reference (Gain) Adjust
5	Bit 5/13	36	$+10\text{V}$ Reference Output ⁽²⁾
6	Bit 6/14	35	Common (Reference)
7	Bit 7/15	34	DNC
8	Bit 8/16	33	Common (Analog)
9	Clip Detect Output	32	$+10\text{V}$ Reference Input ⁽²⁾
10	$+V_{DD2}$ ($+5\text{V}$) Digital	31	Input D ⁽¹⁾
11	Common (Digital)	30	Input C ⁽¹⁾
12	Data Strobe	29	Common (Signal)
13	High/Low Byte Select	28	Input B ⁽¹⁾
14	Convert Command	27	Input A ⁽¹⁾
15	Sample/Hold Control ⁽³⁾	26	$-V_{CC}$ (-15V) Analog
16	Common (Digital)	25	Common (Power)
17	Common (Digital)	24	$+V_{CC}$ ($+15\text{V}$) Analog
18	Clock Adjust	23	DNC ⁽⁴⁾
19	Common (Digital)	22	Offset Adjust
20	$+V_{DD2}$ ($+5\text{V}$) Digital	21	Offset Adjust

NOTES: (1) Refer to Input Connection Table. (2) Reference Input is normally connected to Reference Output, unless an external 10V reference is used. (3) Sample/Hold Control goes high to activate Hold mode. (4) DNC = Do Not Connect.

PACKAGING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
ADC701JH	Metal and Ceramic	230
ADC701KH	Metal and Ceramic	230

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ADC701 ORDERING INFORMATION

ADC701 () H	
Basic Model Number	_____
Performance Grade Code	_____
K: 0°C to $+70^\circ\text{C}$ Ambient Temperature	
J: $+15^\circ\text{C}$ to $+55^\circ\text{C}$ Ambient Temperature	
Package Code	_____
H: Metal and Ceramic	

ADC701 ABSOLUTE MAXIMUM RATINGS

$\pm V_{CC}$	$\pm 18\text{V}$
$\pm V_{DD1}$, $+V_{DD2}$	$\pm 7\text{V}$, $+7\text{V}$
Analog Input	$\pm V_{CC}$
Logic Input	-0.5V to $(+V_{DD2} + 0.3\text{V})$
Logic Output	$\pm 25\text{mA}$
Case Temperature	$+150^\circ\text{C}$
Junction Temperature	$+165^\circ\text{C}$
Storage Temperature	-65°C to $+165^\circ\text{C}$
Power Dissipation	3W
Stresses above these ratings may permanently damage the device.	

ADC701 OUTPUT CODING

INPUT LEVEL (Exact Center of Code)	NOMINAL INPUT VOLTAGE TO ADC701 (Multiply by -1 for SHC702 Input Voltage)			OUTPUT CODE (1 = Logic High)		CLIP DETECT
	0-10V RANGE (1LSB \approx 153 μ V)	\pm 10V RANGE (1LSB \approx 05 μ V)	\pm 5V RANGE (1LSB \approx 153 μ V)	MSB	LSB	
Underrange -FS -FS + 1LSB	< -76 μ V 0V +153 μ V	< -10.000153V -10V -9.999695V	< -5.000076V -5V -4.999847V	0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0000 0001		1 0 0
-3/4FS -1/2FS -1/4FS	+1.25V +2.5V +3.75V	-7.5V -5V -2.5V	-3.75V -2.5V -1.25V	0010 0000 0000 0000 0100 0000 0000 0000 0110 0000 0000 0000		0 0 0
-1LSB Mid-Scale +1LSB	+4.999847V +5V +5.000153V	-305 μ V 0V +305 μ V	-153 μ V 0V +153 μ V	0111 1111 1111 1111 1000 0000 0000 0000 1000 0000 0000 0001		0 0 0
+1/4FS +1/2FS +3/4FS	+6.25V +7.5V +8.75V	+2.5V +5V +7.5V	+1.25V +2.5V +3.75V	1010 0000 0000 0000 1100 0000 0000 0000 1110 0000 0000 0000		0 0 0
+FS -2LSB +FS - 1LSB Overrange	+9.999695V +9.999847V > +9.999924V	+9.99939V +9.999695V > +9.999847V	+4.999695V +4.999847V > +4.999924V	1111 1111 1111 1110 1111 1111 1111 1111 1111 1111 1111 1111		0 0 1

SHC702 PIN ASSIGNMENTS

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	Sample/Hold Output	24	+V _{CC} (+15V) Analog
2	NC ⁽³⁾	23	Common (Power)
3	NC	22	-V _{CC} (-15V) Analog
4	NC	21	Common (Analog)
5	NC	20	NC
6	NC	19	NC
7	NC	18	NC
8	NC	17	Buffer Amp Input ⁽²⁾
9	+V _{DD1} (+5V) Analog	16	NC
10	Common (Digital)	15	Common (Signal)
11	Hold Input ⁽¹⁾	14	Buffer Amp Output
12	Hold Input ⁽¹⁾	13	Analog Input

NOTES: (1) Hold mode is activated only when pin 12 is low and pin 11 is high. For normal use with ADC701, pin 12 is grounded and pin 11 is connected to ADC701 Sample/Hold control (ADC701 pin 15). (2) If the buffer amp is not used, pin 17 should be grounded. (3) NC = No Internal Connection.

PACKAGING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾
SHC702JM	24-Pin	037

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

SHC702 ORDERING INFORMATION

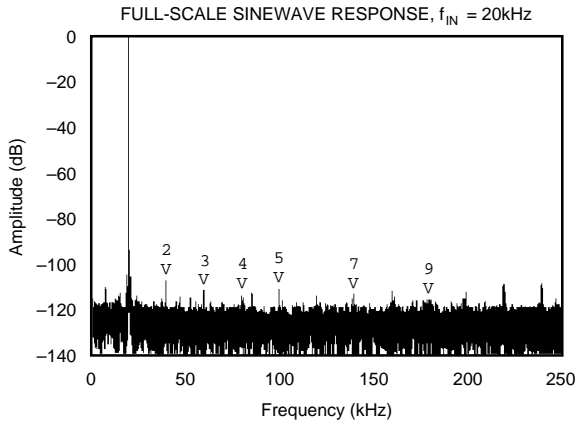
	SHC702	J	M
Basic Model Number	_____	_____	_____
Performance Grade Code	_____	_____	_____
J: 0°C to +70°C Ambient Temperature			
Package Code	_____	_____	_____
M: Metal			

SHC702 ABSOLUTE MAXIMUM RATINGS

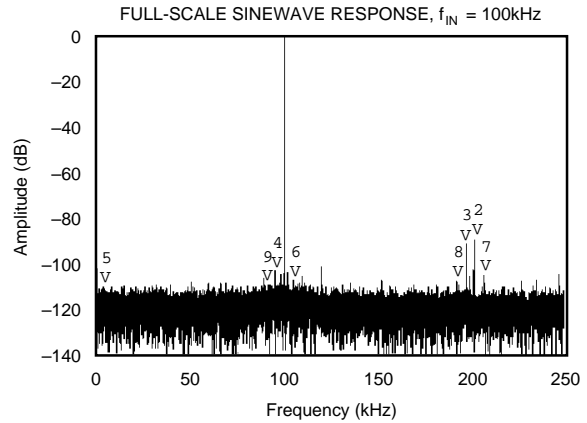
\pm V _{CC}	\pm 18V
+V _{DD1}	+7V
Analog and Buffer Inputs	\pm V _{CC}
Outputs	Indefinite Short to Common
Logic Inputs	-0.5V to (+V _{DD1} + 0.3V)
Case Temperature	+150°C
Junction Temperature	+165°C
Storage Temperature	-65°C to +165°C
Power Dissipation	1.5W
Stresses above these ratings may permanently damage the device.	

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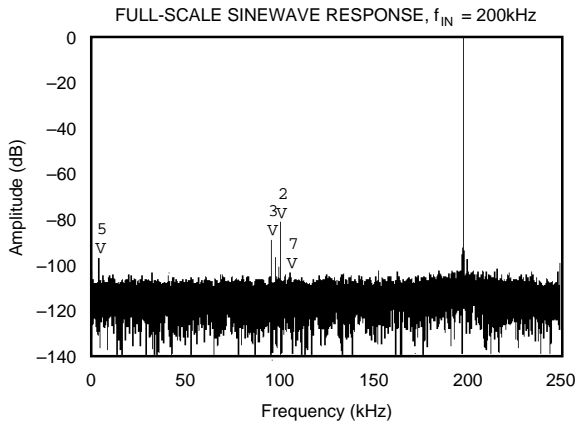
TYPICAL DYNAMIC PERFORMANCE (ADC701/SHC702)⁽¹⁾



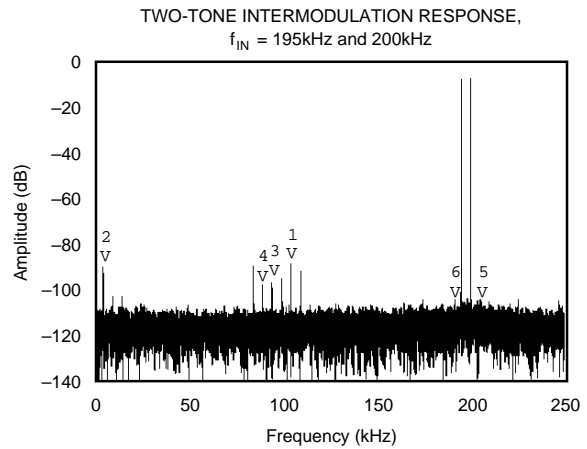
Input Frequency	19.9890136719 kHz	
Fundamental	-0.3 dB	4th Harmonic -115.6 dB
2nd Harmonic	-107.5 dB	5th Harmonic -111.2 dB
3rd Harmonic	-111.5 dB	6th Harmonic -124.5 dB



Input Frequency	100.982666016 kHz	
Fundamental	-0.5 dB	4th Harmonic -102.5 dB
2nd Harmonic	-89.1 dB	5th Harmonic -110.2 dB
3rd Harmonic	-90.5 dB	6th Harmonic -106.8 dB

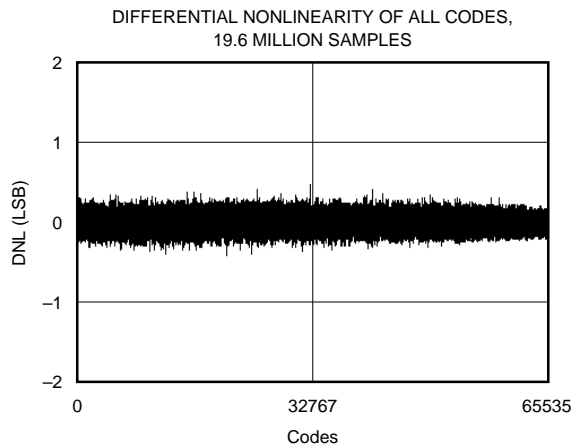


Input Frequency	199.005126953 kHz	
Fundamental	-0.7dB	4th Harmonic -111.5dB
2nd Harmonic	-81.4dB	5th Harmonic -97.0dB
3rd Harmonic	-89.4dB	6th Harmonic -112.5dB



Frequency 1	194.976806641 kHz	
Frequency 2	199.981689453 kHz	
f_1	-6.8dB	$3 > f_1 + 2f_2$ -96.0dB
f_2	-6.3dB	$4 > 2f_1 + f_2$ -96.8dB
$1 > f_1 + f_2$	-87.7dB	$5 > f_1 - 2f_2$ -104.9dB
$2 > f_1 - f_2$	-88.8dB	$6 > 2f_1 - f_2$ -109.0dB

NOTE: (1) For figures above, sampling rate = 500.000000000kHz. 16,384 point FFT, non-windowed. Noise floor limited by synthesized generators.



THEORY OF OPERATION

The ADC701 uses a three-step subranging architecture, meaning that the analog-to-digital conversion is performed in three passes which constitute coarse, medium and fine approximations of the input signal. Refer to Figures 1 and 2 for simplified block diagrams of the system.

Before the input signal is presented to the ADC, it must be sampled with high linearity and low aperture error by the sample/hold amplifier.

In the SHC702, the sampling switch is placed at the summing junction (virtual ground) of a high speed FET amplifier (Figure 1). This arrangement maintains constant charge injection independent of the signal amplitude, which is critically important for good linearity performance. The sampling switch itself is a high speed DMOS FET whose gate is driven from a fast-slewing control signal, thus minimizing the time aperture between the fully closed (sample mode) and the fully open (hold mode) states of the switch. The signal voltage is held across the feedback capacitor, forcing the op-amp to maintain a constant output voltage for the duration of the A/D conversion. Feedthrough from the input, already low due to the MOSFET's low capacitance, is further reduced by clamping the summing point to ground with another FET.

The ADC701 input voltage is converted to a current through the input scaling resistors (Figure 2), and this current is applied to the summing junction (virtual ground) of error amplifier A_1 . The current output of the DAC (0 to 2mA) is also applied to the summing point. If bipolar operation is selected, the 10V reference output is applied to input D, creating a 1mA offset current which sums with the input current.

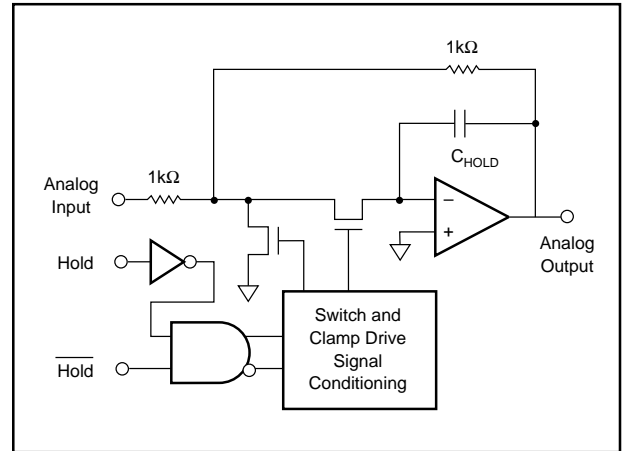


FIGURE 1. Simplified Block Diagram of the SHC702.

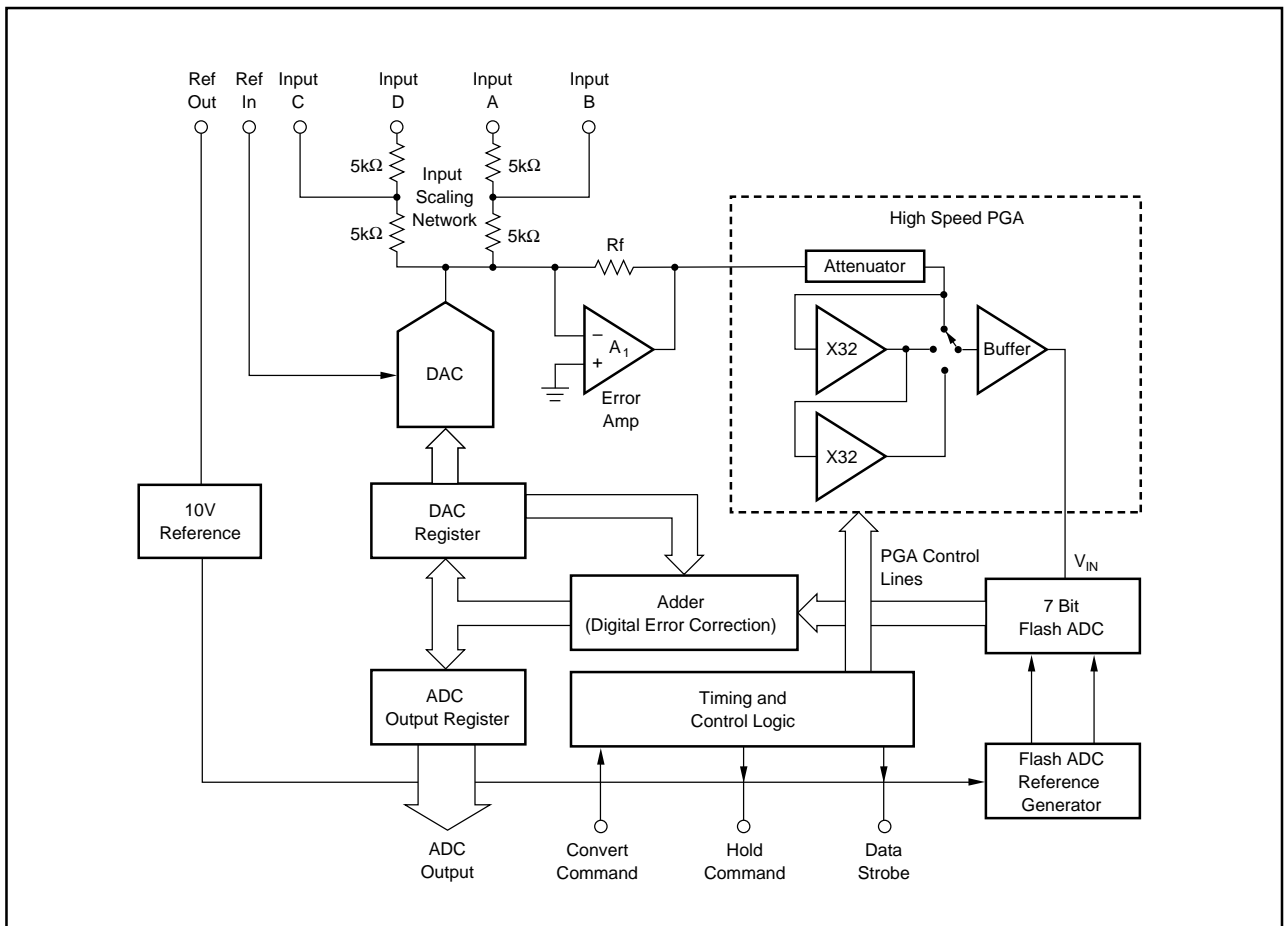


FIGURE 2. Simplified Block Diagram of the ADC701.

At the beginning of each conversion, the DAC is reset to mid-scale so that its output current is exactly 1mA. This 1mA is subtracted from the input signal current. The difference current flows through Rf and appears as an error voltage at the output of A₁.

During the first pass, the programmable gain amplifier (PGA) is set to unity gain, which matches the error voltage range to the input range of the flash ADC. The error signal is digitized to 7-bit resolution by the flash ADC, creating a coarse approximation of the digital output value, which is then applied to the DAC.

Since the DAC output is now approximately equal to the input signal current, the remaining difference current flowing through Rf is small—ideally less than 1/128 of full scale, which is due to the built-in quantizing uncertainty of the 7-bit flash ADC. However, other sources of error (e.g., integral and differential nonlinearity of the flash ADC, gain and offset of the PGA, settling and noise errors throughout the signal path) cause the possible error range to be significantly greater. In fact, the ADC701 is designed to handle remainder signals up to 1/32 of full scale, which is four times the “ideal” value.

Therefore, the PGA is set during the second pass to a gain of 32, allowing the small remainder signal to match the full range of the flash ADC. This is again digitized to 7-bit resolution and added to the previous result to create the “medium” approximation of the input signal. Because the full-scale range of the flash represents 1/32 of the input signal’s full range, the 7-bit flash output is shifted right by 5 bits before being added to the original 7-bit “coarse” result, creating a 12-bit word. There is an overlap of two bits because the two least significant bits of the first-pass result correspond to the two most significant bits of the second-pass result. This overlap in the adder is called “digital error correction”—the mechanism that allows nonideal remainders from the first pass to be corrected in the second pass.

The 12-bit approximation is applied once again to the DAC, causing the remaining difference current to become yet smaller. For the third pass, the PGA’s gain is increased by another factor of 32, and the remainder is again digitized by the flash ADC.

At this point in the conversion, all of the necessary data has been latched and it is no longer necessary to hold the analog signals from the sample/hold or the DAC. From a systems perspective, the conversion is now complete because the sample/hold is released to begin acquiring the next input sample and the DAC is reset to mid-scale for the next conversion. Meanwhile, the final result from the flash is added to the previous 12-bit result. Again there is a two-bit overlap to allow for error correction. The adder output is monitored to prevent a digital “rollover” condition, so that the ADC clips properly at the signal extremes. The upper sixteen bits of the final adder result are stored in the ADC’s output register, ready to be presented in byte-sequential form at the eight output data lines. The overrange or “clip” condition can also be detected externally by monitoring pin 9. Refer to the section on ADC701 Digital I/O for further detail.

INSTALLATION AND OPERATING INSTRUCTIONS

The ADC701/SHC702 combination is designed to be easy to use in a wide variety of applications, without sacrificing flexibility of the analog and digital interface.

SHC702 INTERFACE

The connection diagram (Figure 3) shows the basic hookup. At the SHC702 input, the user may opt to connect the built-in FET buffer amplifier. The buffer is most useful in multi-channel applications where the signal bandwidth is less than 100kHz. In those applications, it serves to isolate the multiplexer output from the 1kΩ input impedance of the sample/hold. For higher frequency applications and for any system that does not require the very high impedance, the best results (lowest noise and distortion) will be achieved by driving the SHC702’s analog input directly. If the buffer is not used, its input should be grounded to avoid random noise pickup and saturation of the buffer op amp.

Only two connections are required between the SHC702 and the ADC701: SHC702 analog output to ADC701 input(s) and the digital Hold Command from the ADC701 to the SHC702. As always, it is best to avoid routing these analog and digital lines along parallel traces. Although the placement of the SHC702 relative to the ADC is not extremely critical, one good approach is to mount the SHC along one end of the ADC package as shown in Figure 4. This minimizes the length of the interconnections and keeps the digital lines well away from sensitive analog signals.

ADC701 INPUT CONNECTIONS

The ADC input network has four separate terminals, allowing many different input ranges. These should be connected as indicated in Table I. Most users will take advantage of the ADC701’s built-in reference circuit, which has very low noise and excellent temperature stability. To use the internal reference, it is only necessary to connect pin 36 (Reference Output) to pin 32 (Reference Input). To use an external 10V reference (to cause the ADC gain to track a system reference, for example), pin 36 is left unconnected and the external reference is applied to pin 32. If required, the ADC701 will typically accommodate a five to ten percent variation in the 10V reference. External references should have very low noise to avoid degrading the excellent signal-to-noise ratio (SNR) of the ADC701.

INPUT RANGE	CONNECT V _{IN} TO	CONNECT Ref In TO
0 to +10V	Input A and Input D	—
±10V	Input A	Input D
±5V	Input A and Input B	Input D
-10V to 0	Input A and Input B	Input C and Input D
0 to +5V	Input B and Input C	—

TABLE I. ADC701 Input Connection Table.

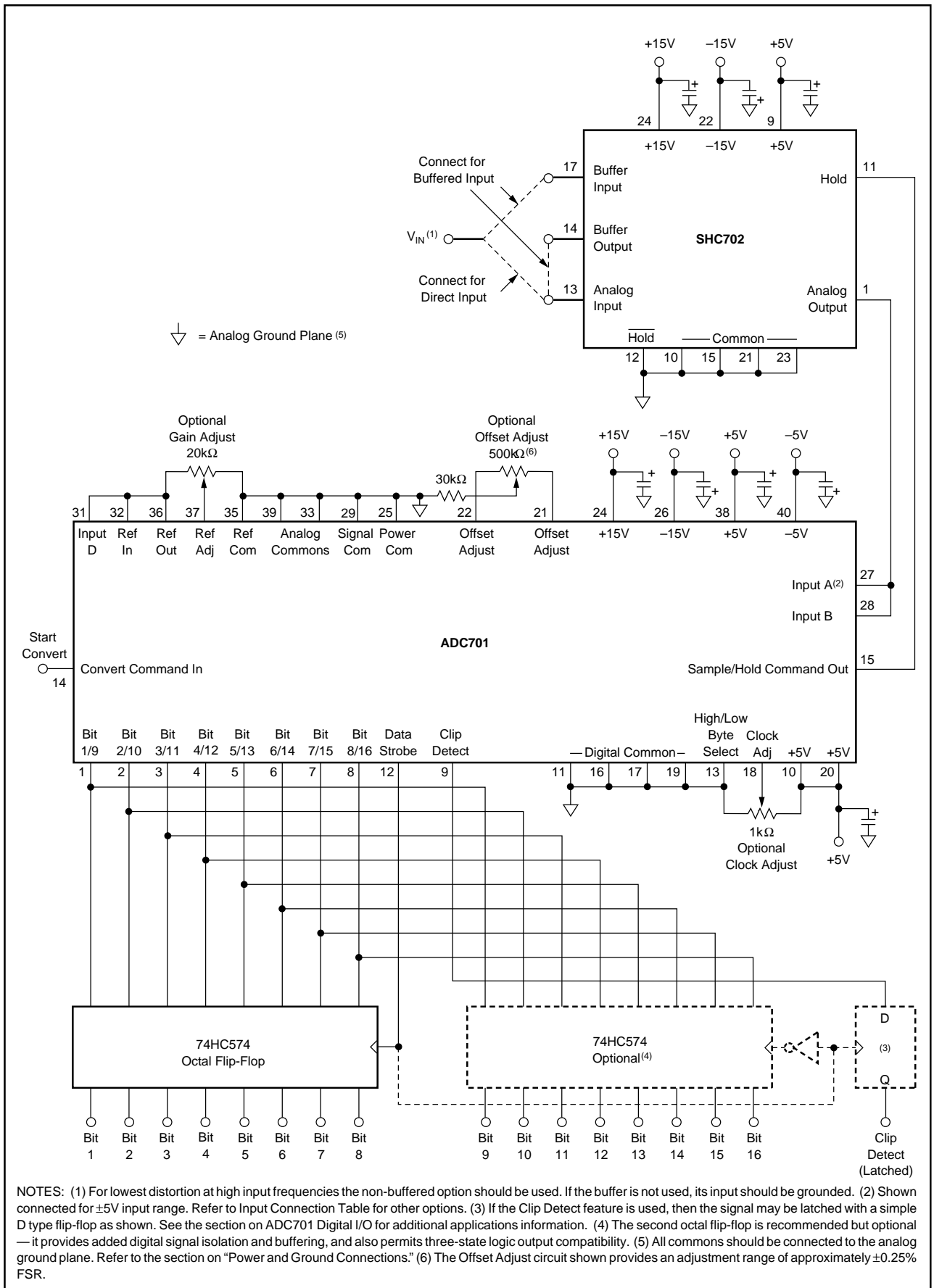


FIGURE 3. ADC701/SHC702 Connection Diagram.

OFFSET, GAIN AND CONVERSION SPEED ADJUSTMENTS (OPTIONAL)

Adjustment of the reference voltage is the most straightforward way to adjust the ADC gain. For the internal reference, this is accomplished by connecting a 20k Ω potentiometer as shown in Figure 3. This will provide a gain trim range of about $\pm 3\%$. It is also possible to use external series or parallel resistance in the input network, but that is more cumbersome and usually will degrade the gain stability over temperature due to tempco (temperature coefficient) mismatches among the resistors.

ADC offset may be adjusted by connecting a 500k Ω potentiometer to pins 21 and 22, with the wiper connected through a series 30k Ω resistor to ground as shown in Figure 3. This will provide an offset trim range of approximately $\pm 0.25\%$ FSR. For a larger trim range of offset or gain, it is recommended that trims be accomplished elsewhere in the system.

The Clock Adjust input (pin 18) is intended primarily for small adjustments of the conversion time. However, this will rarely be necessary because the ADC701 is guaranteed to convert up to 512kHz over the specified temperature range without external clock adjustment.

POWER AND GROUND CONNECTIONS

Experience with testing and applying the ADC701 shows that it will perform well in most board layouts, provided that appropriate care is taken with grounding and bypassing.

Power supplies may be shared between the ADC701, SHC702 and other analog circuitry without difficulty. It is recommended that each power pin be locally bypassed to the ground plane with a high quality tantalum capacitor of at least 1 μ F. If at all possible, power should be derived from well-regulated linear supplies—switching power supplies will require much more effort for proper decoupling and are not recommended for this or any high performance wide-band analog system.

The +5V Digital supply pins, though not as sensitive to noise as the +5V Analog pin, should nonetheless be kept as quiet as possible. If the system digital supply is noisy, then it is best to use the system +5V analog supply for all of the +5V connections on the ADC701 and SHC702 rather than trying to separate them. If only one +5V supply is available and it is shared with other system logic, then extra bypassing and/or supply filtering may be required.

The -5V supply will operate with any voltage between -4.75 and -6V. If -5V is not available from the system supplies, then an industry-standard 7905 regulator may be used to derive -5V from the -15V supply.

All ground pins on both the ADC701 and the SHC702 should be connected directly to a common ground plane. This is true for both analog and digital grounds. However, it is also helpful to recognize where the digital ground currents flow in the system, and to provide PC board return paths for potentially troublesome digital currents in addition

to the ground plane connections. For example, the ADC701 output data lines will sink current (statically and/or dynamically) when in the low state. This current comes from the power supply that runs the interface logic, and so must return to that supply's ground. If the ground termination is placed such that this digital current will flow away from the ADC701, then the existing ground plane will suffice to carry the current. On the other hand, if the ground termination must be placed such that the digital current flows across the ADC or SHC layout, then it would be advisable to break the analog ground plane under the package (to stop the flow of current across the package) and to provide a separate trace (several centimeters wide) on another PC board layer to carry the digital return current from pins 11 and 19 to the termination point. If the ADC701 must interface into a fairly noisy digital environment, then another approach is to keep the first layer of latches and/or buffers connected to the ADC701 power and ground planes, so that the ADC itself is connected to "quiet" circuits with short return paths. This transfers the interface problem to the outputs of the latches, where it can be managed with less impact on the analog components.

PHYSICAL INSTALLATION

The packages may be soldered directly into a PC board or mounted in low-profile machined pin sockets with good results. Use of tall (long lead length) sockets, adapters or headers is not recommended unless a local ground plane and bypass capacitors can be mounted directly under the packages.

In a room-temperature environment or inside an enclosure with moderate airflow, the ADC701 and SHC702 normally do not require heat-sinking. However, to keep the devices running as cool as possible, it is helpful to install a thin heat-transfer plate under the packages to conduct heat into the ground plane. The plate may be made from metal (copper, aluminum or steel) or from a special heat-conductive material such as Sil-Pad⁽¹⁾. The Sil-Pad material has the advantage of being electrically insulating and somewhat pliable, so that it will tend to distribute pressure evenly and conform to the package—an advantage in systems where the board may be flexed or subjected to vibration.

PC BOARD LAYOUT

An optimized layout has been designed for the DEM-ADC701-E demonstration fixture. For information concerning the demo board and the layout, contact your local sales representative.

ADC701 Digital I/O

Refer to the timing diagram, Figure 4. The conversion process is initiated by a rising edge on the Convert Command input. This will immediately bring the sample/hold command output to a logic high state (Hold mode).

After the ADC701 conversion is completed (approximately 1.5 μ s after the convert command edge), the Sample/Hold Command falls to a low state, enabling the sample/hold to begin acquisition of the next input sample. However, the ADC701 internal clock continues to run so that the output data may be processed.

There are two methods of reading data from the ADC:

1. Strobed Output—This will usually be the easiest and fastest method. The data are presented sequentially as high and low bytes of the total 16-bit word. The sequence High-Low or Low-High is controlled by the state of the High/Low Byte Select input. The first byte is valid on the rising edge of the Data Strobe output; the second byte is valid on the falling edge.
2. Polled output—With this method, data strobes will occur as described above, but they are ignored by the user. Instead, the user waits until the Data Strobe output falls, and then manually selects high and low output data by means of the High/Low Byte Select input. This polling procedure may be carried out during the subsequent ADC conversion cycle, but two precautions must be observed: First, the user should avoid switching the High/Low Byte Select immediately before or after the next convert command. This will prevent digital switching noise from coupling into the system at the instant of analog sampling. Second, the polling sequence must be completed before the ADC begins to strobe out data from the subsequent conversion.

OPTIONS FOR STROBED OUTPUT

There are several ways in practice to implement the logic interface. Figure 3 shows the simplest configurations. In order to convert the ADC701's byte-sequential data into 16-bit parallel form, the minimum requirement is for one single octal flip-flop, such as a 74HC574 or equivalent. This will latch the first byte on the rising edge of the ADC701 Data Strobe. Then the second byte becomes valid, and all 16 bits may be strobed to the outside system on the falling edge of the Data Strobe.

For better noise isolation of the ADC701 from the digital system, or if full three-state capability is required for the 16 output lines, a second octal flip-flop can be added as shown in the dashed lines of Figure 3. This will also require an inverter to convert the falling Data Strobe edge into a rising clock edge for the second flip-flop IC.

If it is desirable to have all 16 output lines change simultaneously (for example when driving a D/A converter), then a third octal flip-flop (not shown in Figure 3) may be added to re-latch the output of the first byte. By driving that device's clock also from the inverted Data Strobe, fully synchronous switching of the 16 output bits will be achieved.

USING THE CLIP DETECT OUTPUT

The ADC701 provides a built-in Clip Detect signal on pin 9 which indicates an ADC overrange or underrange condition. The Clip Detect signal is only valid when the High Byte becomes valid as shown in Figure 4. Therefore, the simplest way to latch the Clip Detect signal is to provide an extra flip-flop which is clocked on the same strobe edge as the High Byte flip-flop. Such a setup is illustrated in Figure 3. The Clip Detect signal remains at logic 0 under normal conditions, and indicates a clip condition by rising to a logic 1.

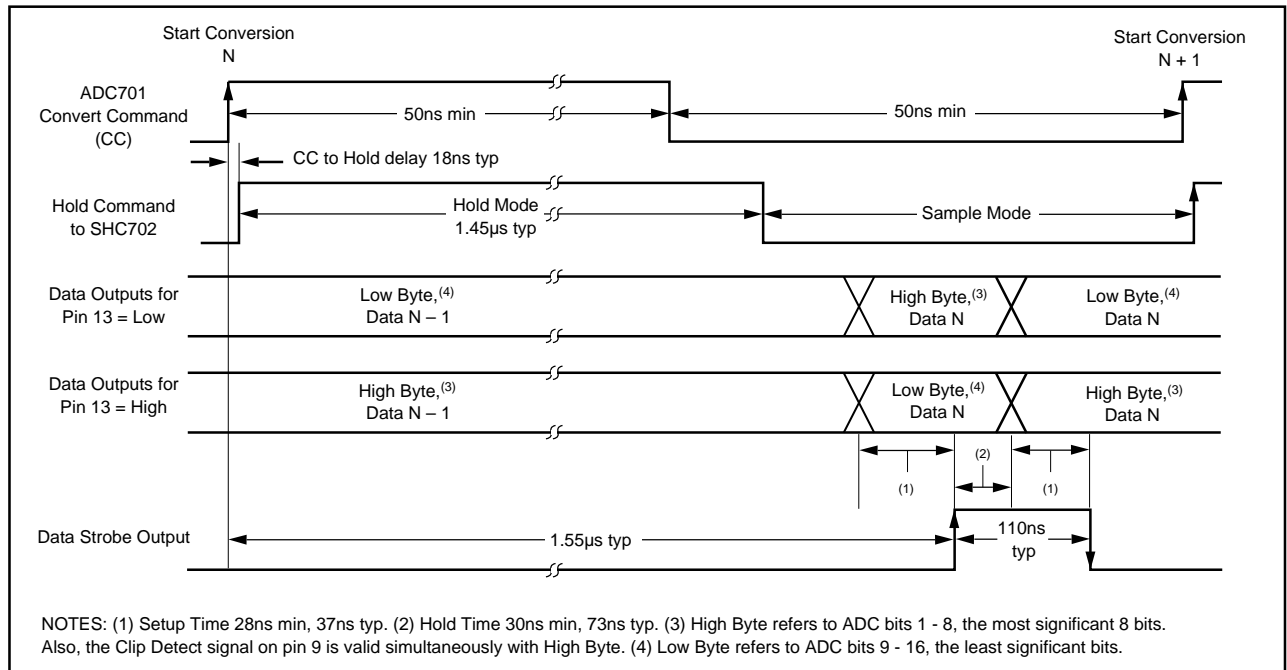


FIGURE 4. ADC701 Interface Timing Diagram.

The latched version of Clip Detect may be used to generate an interrupt to the user's system computer, which would then launch a service routine to generate the appropriate alarms or corrective action. Another possible application would be to stretch the pulse using a monostable so that it would be easily visible when driving an LED warning lamp.

In some systems, it may be desirable to provide separate latched outputs for Underrange and Overrange. These conditions may be separately detected by using simple logic to implement the boolean equations:

$$\text{Underrange} = \text{Clip Detect AND } \overline{\text{Anybit}}$$

$$\text{Overrange} = \text{Clip Detect AND Anybit}$$

where "Anybit" is any one of the data output bits.

The Underrange and Overrange signals would then be latched into two separate flip-flops. A simple solution using a single '74 dual flip-flop and a single '00 quad NAND provides enough logic to implement the logic equations, with a spare NAND gate left over to use for creating the inverted Data Strobe signal.

USING THE ADC701 AT MAXIMUM CONVERSION RATES

The ADC701 is guaranteed to accept Convert commands at a rate of DC to 512kHz over the specified operating temperature range. At a conversion rate of 500kHz, the total throughput time of 2μs allows for the 1.5μs ADC conversion time plus 500ns for the digital output timing and sample/hold acquisition time.

If the user tries to exceed the maximum conversion rate by a large amount, the Convert Command of conversion N+1 will occur before the Data Strobe has fallen from conversion N. In such a situation, the ADC701 will simply ignore every other Convert command so the actual conversion rate will become half of the Convert command rate. Otherwise, the conversion will proceed normally. Note that the ADC timing slows down at high temperatures, so the frequency at which this occurs will vary with temperature—although it is still guaranteed to be greater than 512kHz over the specified temperature range.

Another consideration for operation at very high rates is that the sample/hold acquisition time becomes shorter as the conversion rate is increased. Users will note that the available acquisition time becomes less than 550ns at rates above 500kHz, which is less than the typical SHC702 acquisition time for a 10V step to 150μV accuracy. However, the signal degradation is gradual as the acquisition time is shortened—even at 512kHz, there is enough time to acquire a 5V step to better than 500μV. Also, most signal processing environments do not contain full-power signals at the Nyquist frequency, but rather show a rolloff of signal power at high frequencies. If the ability to acquire extremely large input changes at extremely high conversion rates is of paramount importance, the user may elect to use a Burr-Brown model SHC803 sample/hold instead—it is pin compatible with the SHC702 and provides much faster acquisition time at the expense of some extra noise and higher distortion at low input frequencies.

TESTING THE ADC701/SHC702

The ADC701 and SHC702 together form a very high performance converter system and careful attention to test techniques is necessary to achieve accurate results. Spectral analysis by application of a Fast Fourier Transform (FFT) to the ADC digital output is the best method of examining total system performance. Attempts to evaluate the system by analog reconstruction through a D/A converter will usually prove unsatisfactory; assuming that the static and dynamic distortions of the D/A can be brought below the required level (-110dB), the performance will still be beyond the range of presently available spectrum analyzers.

Even when the analysis is done using FFT techniques, several key issues must be addressed. First, the parameters of the FFT need to be adequate to perform the analysis and extract meaningful data. Second, the proper selection of test frequencies is critical for good results. Third, the limitations of commercial signal generators must be considered. These three points are addressed in later sections. Finally, the test board layout must follow the recommendations discussed on pages 8 through 10.

DYNAMIC PERFORMANCE DEFINITIONS

1. Total Harmonic Distortion (THD):

$$10 \log \frac{\text{Harmonic Power (first 9 harmonics)}}{\text{Sinewave Signal Power}}$$

2. Signal-to-Noise Ratio (SNR):

$$10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise Power}}$$

3. Intermodulation Distortion (IMD):

$$10 \log \frac{\text{IMD Product Power (RMS sum; to 3rd-order)}}{\text{Sinewave Signal Power}}$$

4. Spurious-Free Dynamic Range (SFDR):

$$10 \log \frac{\text{Power of Peak Spurious Component}}{\text{Sinewave Signal Power}}$$

IMD is referred to the larger of the test signals f_1 or f_2 —**not** to the total signal power, which would result in a number approximately 6dB "better." The zero frequency bin (DC) is not included in these calculations—it represents total offset of the ADC, SHC and test equipment and is of little importance in dynamic signal processing applications.

FFT Parameters

Accurate FFT analysis of 16-bit systems requires adequate computing hardware and software. The FFT length (number of points) should be relatively large—at least 4K and preferably 16K or larger. There are several reasons for this:

1. The converter itself has 64K codes. Ideally, the test would guarantee that all codes are tested at least once. Practically speaking, however, that would require immensely long FFTs (>>64K points) or averaging of a large number of smaller FFTs. By using an FFT length of 4K or greater and proper selection of the test frequencies, a very good statistical picture of the ADC performance will be obtained which shows the effect of any defects in the transfer function.
2. The noise floor of the output spectrum is not low enough if less than 4K points are taken. Shorter FFTs have fewer bins to cover the output spectrum, so a larger fraction of the total system noise appears in each bin. Although the SNR of the ADC701/SCH702 system is in the range of -93dB, the noise level of the available generators may increase the total measured noise power to -80dB. Every doubling of the FFT length will spread the noise power among twice as many bins, resulting in a 3dB reduction of the spectral noise floor. In order to resolve spurious components that are at the level of -110dB, an average noise floor of less than -113dB would be barely adequate. This requires at least 2048 bins in the output half-spectrum, corresponding to a 4K-point FFT. Even at this level, it will be difficult or impossible to separate higher order harmonics in the ADC701 response from the average noise level, indicating that longer FFTs are desirable.
3. Following the guidelines for test frequency selection which are outlined in the next section, it becomes clear that longer FFTs allow a much wider choice of test frequencies without concern for sophisticated data windowing or code coverage problems.

Besides the consideration of FFT length, it is important to realize that the FFT calculations must be performed with high-precision arithmetic. The use of 32-bit fixed or floating point calculations will generally be inadequate because the noise floor due to calculation errors alone will interfere with the ADC performance data. Unfortunately, this consideration precludes the use of most DSP accelerator boards and similar hardware. In order to preserve the full dynamic range of the ADC output, it is best to use standard 64- or 80-bit arithmetic. To avoid excessively long calculation times, the FFT algorithm should be written in an efficiently compiled language and make use of techniques such as trigonometric look-up tables in software and dedicated floating-point coprocessors in hardware. There are several commercial software packages available from Burr-Brown and others that meet these requirements.

SELECTION OF TEST FREQUENCIES

The FFT (and any similar DSP operation) treats the total time-domain record length as one cycle of an infinitely long periodic signal. Therefore, if the end of the sampled record does not match up smoothly with the beginning, the output spectrum will contain serious errors known as leakage or truncation error⁽²⁾. This well-known problem is usually handled by applying a windowing function to the time-domain samples, suppressing the worst effects of the mismatch. However, the most often used windows such as Hanning, Hamming, raised cosine, etc., are completely inadequate for 16-bit ADC testing. More sophisticated functions such as the four-sample Blackman-Harris window⁽³⁾ will provide much better results, although there still will be obvious spreading of the spectral lines.

The most successful approach is to eliminate the need for windowing by properly selecting the test signal frequency (or frequencies) in relation to the ADC sampling frequency⁽⁴⁾. If the time sample contains exactly an integer number of cycles, then there is no mismatch or truncation error. Another point to consider is that the sampling frequency should not be an exact integer multiple of the signal frequency, which would tend to reduce the number of different ADC codes that are tested and also tend to artificially concentrate quantization error in the harmonics of the test signal.

Both of these criteria are met by choosing an FFT length which is a power of two (the most standard and fastest to compute) and choosing a test frequency which causes an exact **odd** integer number of cycles to appear in the time record. In software, this selection can be accomplished very easily:

1. Determine the desired sampling frequency f_S .
2. Determine the desired input signal frequency f_{APPROX} .
3. Determine the FFT length N , which should be a power of 2 (e.g., 4096 or 16384).
4. Divide f_{APPROX} by f_S , multiply the quotient by N , and round the result to the nearest odd integer. This is M , the number of cycles in the time record.
5. Multiply M by f_S and divide by N to obtain the exact input signal frequency f_{ACTUAL} .

SIGNAL GENERATOR CONSIDERATIONS

To suppress leakage effects, the calculated ratio of f_S to f_{ACTUAL} must be precisely maintained during the test. This requirement is met easily by the use of synthesized signal generators whose reference oscillators can be locked together. Other possible approaches include external phase locking of non-synthesized generators and direct digital synthesis techniques. If it is not possible to use phase-locked signals, then a Blackman-Harris window may be used as mentioned previously.

Another key issue is the purity of both the signal and sampling frequency generators. The sampling clock's phase noise (jitter) will act as another source of SNR degradation. This is not serious as long as the jitter is random and the noise sidebands contain no sharp peaks. The HP3325 synthesizer is suitable for this purpose. The input signal generator will require more attention because its distortion will usually be greater than that of the ADC701/SHC702. Presently, the lowest distortion synthesized generator is the Brüel & Kjær Model 1051 (or 1049). This is suitable for testing the system in the audio range. The upper frequency limit of the B&K synthesizer is 200kHz. Above 20kHz, the distortion becomes a limiting factor, and low-pass filters must be inserted into the signal path to reduce the harmonic and spurious content.

As noted previously, the combined noise contributions of the signal generator and sampling clock generator far exceed the SNR of the ADC701/SHC702 itself. The SNR has been measured separately by applying a highly filtered sinewave to the input, resulting in typical SNR performance of -93dB. However, the filters employed to achieve this low-noise test stimulus are found to cause reactive loading of the signal source which results in increased distortion. Therefore it is best to separate the tests for SNR from those for THD and IMD, unless a suitably pure **and** low-noise signal can be generated.

Figures 5 and 6 show block diagrams of FFT test setups for the ADC701 and SHC702, summarizing the placement of the major components discussed above. The Typical Dynamic Performance section shows typical results obtained from testing the ADC701/SHC702 at a 500kHz conversion rate, using 16K samples for the FFT analysis.

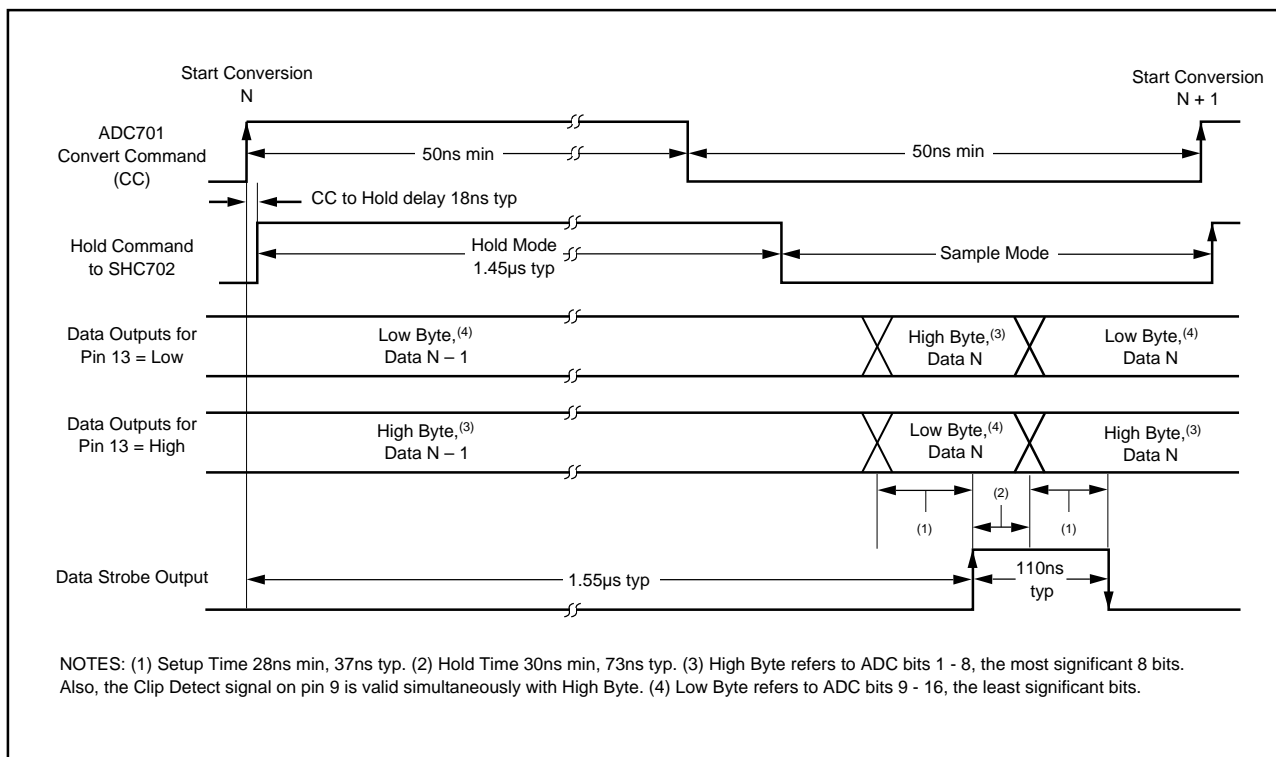


FIGURE 5. FFT Test Configuration for Single-Tone Testing.

HISTOGRAM TESTING

The FFT provides an excellent measure of harmonic and intermodulation distortion. Low-order spurious products are primarily caused by integral nonlinearity of the SHC and ADC. The influence of differential linearity errors is harder to distinguish in a spectral plot—it may show up as high-order harmonics or as very minor variations in the overall appearance of the noise floor.

A more direct method of examining the differential linearity (DL) performance is by using the popular histogram test method⁽⁵⁾. Application of the histogram test to the ADC701/SHC702 is relatively straightforward, though once again extra precision is required for a 16-bit system compared to 8- or 12-bit systems. Basically, this means that a very large number of samples are required to build an accurate statistical picture of each code width. If a histogram is taken using only one million points, then the average number of samples per code is less than fifteen. This is inadequate for good statistical confidence, and the resulting DL plot will look considerably worse than the actual performance of the con-

verter. In practice 10 to 20 million samples will demonstrate good results for a 16-bit system and expose any serious flaws in the DL performance. If the memory incrementing hardware can keep pace with the ADC701, then 20 million samples can be accumulated in well under one minute. The last figure on page six shows the results of a 19.6 million point histogram taken at an input frequency of 1kHz.

NOTES:

1. Available from Bergquist, 5300 Edina Industrial Blvd., Minneapolis, MN 55435 (612) 835-2322.
2. Brigham, E. Oran, *The Fast Fourier Transform*, Englewood Cliffs, N.J.: Prentice-Hall, 1974.
3. Harris, Fredric J., "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform", *Proceedings of the IEEE*, Vol. 66, No. 1, January 1978, pp 51-83.
4. Halbert, Joel M. and Belcher, R. Allan, "Selection of Test Signals for DSP-Based Testing of Digital Audio Systems", *Journal of the Audio Engineering Society*, Vol. 34, No. 7/8, July/August, 1986, pp 546-555.
5. "Dynamic Tests for A/D Converter Performance", Application Bulletin AB-133, Burr-Brown Corporation, Tucson, AZ, 1985.

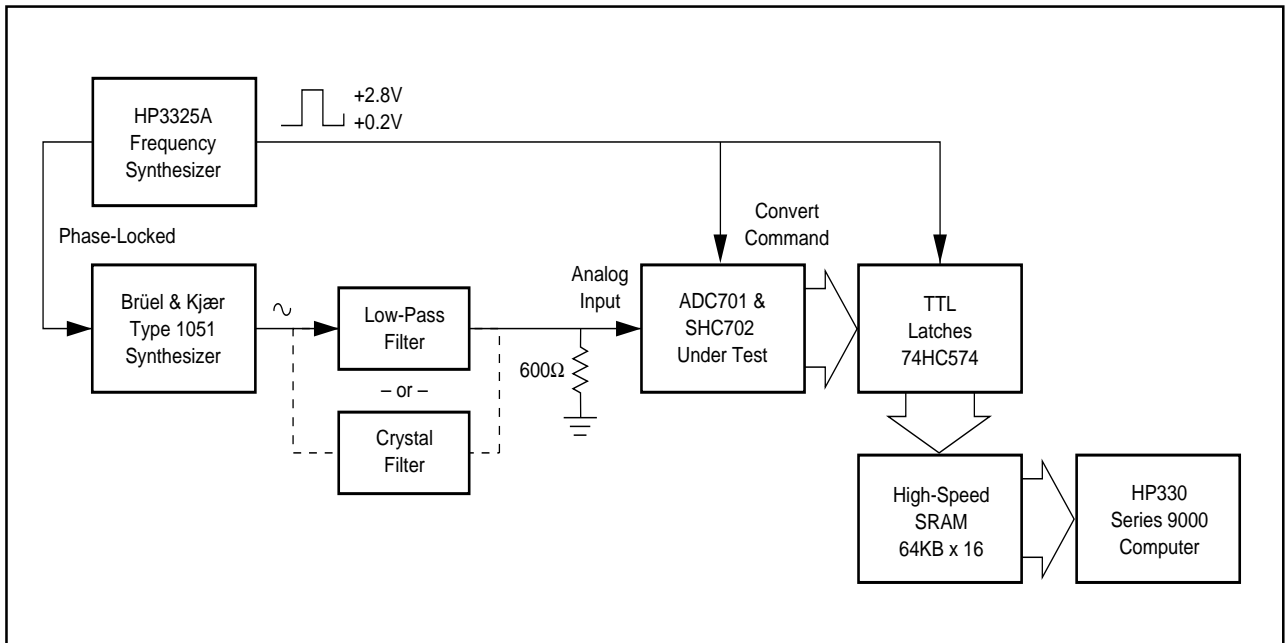


FIGURE 6. FFT Test Configuration for Two-Tone (Intermodulation) Testing.