High Speed SPI Functional Block for the FPSLIC

Introduction

The AT94K-AL FPSLIC family includes several hard-wired peripherals. These include UARTs, timers, and a two-wire synchronous serial interface. Another popular interface, not currently implemented in the AT94K-AL, is the SPI synchronous serial interface.

This application note shows how to implement a high-speed SPI with the following features:

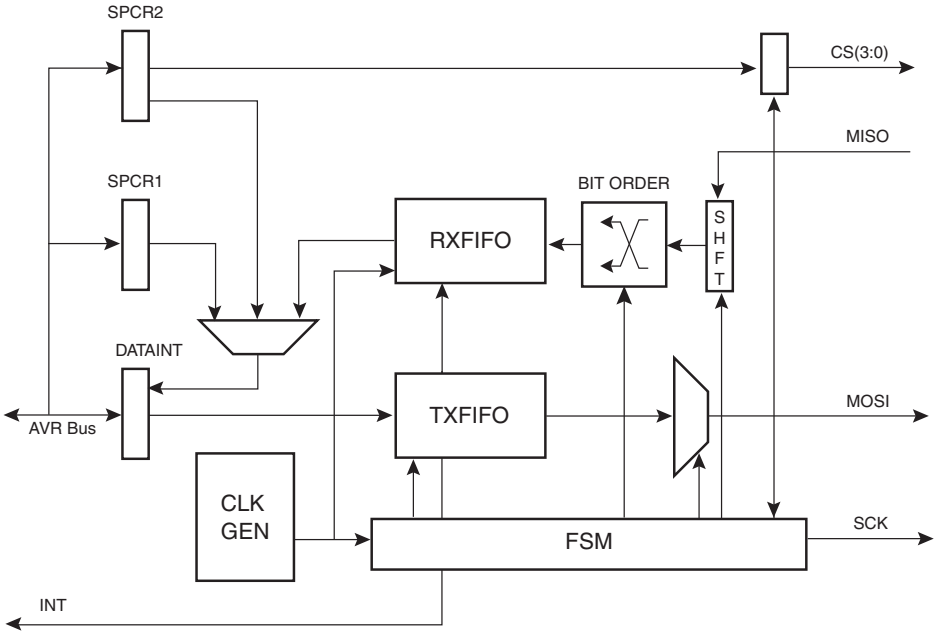
- Master only operation
- LSB first or MSB first data transfer
- Seven programmable bit rates
- End of transmission interrupt flag
- 32-byte FIFO on both the transceiver and the receiver

The design uses the internal Dual Port RAM (FreeRAM™) available in the FPGA portion of the AT94 to implement 32-byte FIFOs on both the receiver and the transmitter to maximize throughput.

Description

Figure 1 shows the block diagram of the SPI design.

Figure 1. SPI Interface Block Diagram



FPSLIC™

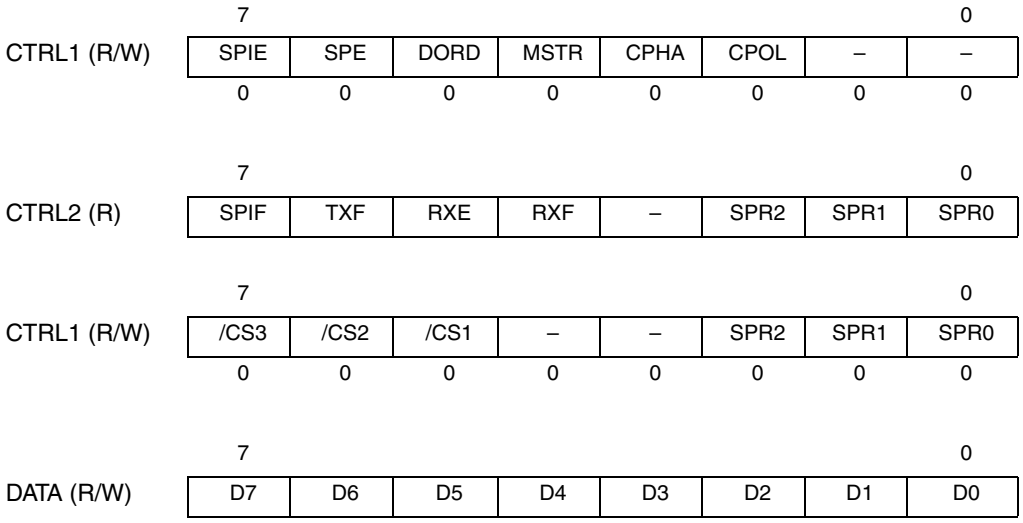
AT94K Series Field Programmable System Level Integrated Circuit

Application Note

3473A–FPSLI–7/04

The AVR® programming interface consists of two I/O locations for control purposes and a single data location that is used to transfer data to the transmit FIFO and from the receive FIFO. Both FIFOs provide “empty” and “full” flags which can be tested by the AVR. An interrupt is available and is active whenever the transmit FIFO is empty. The part will automatically generate chip selects for up to four different peripherals. The timing generator allows prescaling the clock to allow a frequency between 2 to 256 times slower than the system clock or between 100 kbps to 12.5 Mbps.

Figure 2. SPI Programming Interfacing



Control Register Bit Definitions

SPIE	**SPI Interrupt Enable**	When 1, the SPI Interrupt is enabled and will be asserted when the TX FIFO is empty
SPE	**SPI Enable**	When 0, the SPI block is disabled When 1, it shifts as long as the TX FIFO contains data.
DORD	**Data Order**	When 0, the SPI block shifts data MSB first When 1 it shifts data LSB first
MSTR	**Master/Slave**	When 0, the SPI block is in slave mode (not yet implemented) When 1, it is in master mode
CPHA	**Clock Phase**	See SPI specification or the AT90LS8515 datasheet
CPOL	**Clock Polarity**	See SPI specification or the AT90LS8515 datasheet
SPIF	**Transmit FIFO Empty**	Set to 1 when the transfer is completed
TXF	**Transmit FIFO Full**	Set to 1 when the TX FIFO is full
RXE	**Receive FIFO Empty**	Set to 1 when the RX FIFO is empty
RXF	**Receive FIFO Full**	Set to 1 when the RX FIFO is full
/CS(3:0)	**Chip Select Mask**	Set a bit to zero to enable the CS during the transfer Only 1 bit should be set at the same time
SPR(2:0)	**SPI Prescale**	

File Structure

The design consists of five files and they should be compiled in the following order:

1. SPI_config.vhd Definitions and auxiliary functions
2. Fifo2.vhd FIFO (same block used for TX and RX)
3. SPI_timing.vhd The Clock Prescaler
4. SPI_transmit.vhd The Finite State Machine controlling the design
   Also contains the shift mechanism and bit order handling
5. SPI.vhd Top level design, control section

Entity Port List

SPI Interface		
MISO	Master In, Slave Out	
MOSI	Master Out, Slave In	
SCK	SPI Clock	
SPI_CS_Z	SPI Chip Select (3 : 0)	Active Low
AVR Interface		
DOUT	Connect to AVR ADOUT	
DIN	Connect to AVR ADIN	
FIORE	Connect to AVR FIORE	
FIOWR	Connect to AVR FIOWR	
FIOSEL0	Connect to AVR FIOSEL0	
FIOSEL4	Connect to AVR FIOSEL4	
FIOSEL8	Connect to AVR FIOSEL8	
FIOSEL12	Connect to AVR FIOSEL12 (not used)	
SPI_IRQ	Connect to AVR INTA0	Active Low
System interface		
RESET_Z	Connect to external RESET signal	Active Low
CLOCK	Connect to FPGA GCLKn	

Control Section

The Control Section consists of two registers, CTRL1 and CTRL2. The signals for both CTRL registers reside in the SPCR record, which is passed to all internal blocks (except the FIFOs).

The design uses three chip selects that need to be connected to the AVR in System Designer:

- FIOSEL0 => CTRL1 register
- FIOSEL4 => CTRL2 register
- FIOSEL8 => DATA register

For simplicity, they have been named according to the AVR convention in the port list.

While FIOSEL12 is part of the port list, it is not used in the current design.

FIFO

The FIFO is 32 by 8 and contains two 6-bit address pointers for read and write purposes. They are one bit wider than necessary to simplify the settings of the “full” and “empty” flags. When the lower five bits of the address are equal and the upper bit is also equal, the FIFO is empty. When the lower part is equal and the upper bit is different, the FIFO is full.

Prescaler

The Prescaler runs at the system frequency, creating an enable signal for the flip-flops in the Finite State Machine controlling the SPI block. The FSM will only update its registers if the enable signal from the prescaler is asserted.

The enable signal is the carry out from a timer. After each clock cycle, the timer is updated with its previous value incremented by one, and OR’ed with a mask that was generated from the 3-bit SPR prescale configuration bits. The effect of the OR is to reduce the number of clock cycles needed to generate the carry out signal. This can be accomplished by a simple add, but the OR is faster and uses less logic.

Transmitter

The Transmitter State Machine will monitor the Transmit FIFO empty signal and whenever this is deasserted (the FIFO contains data), the transmitter will sample the control register and start shifting out data. The shift is implemented by an 8 to 1 multiplexer, where the 3-bit select signal is either first be incremented or de-incremented depending on if the current transmission should be MSB or LSB.

The transmitter also generates the SPI clock. The Phase and Polarity of the clock is programmable according to normal SPI conventions. The chip select and receive enable signals receive their enable signal from the transmitter FSM.

Receiver

The Receiver is a single shift register running from the system clock. The receive enable signal generated by the Transmit State Machine will control the shift rate.

When eight bits of data is shifted in, it gets written to the receive FIFO, possibly getting the bits reversed to handle the MSB/LSB configuration.

Example Driver

An Example Driver is included in the “driver” directory. This was compiled using the IAR AVR C compiler v1.51C.

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