



FPSLIC on-chip Partial Reconfiguration of the Embedded AT40K FPGA

Features

- Demonstrates Usage of Built-in FPGA Cache Logic[®] Interface
- Implementation Targeted for FPSLIC[™] Starter Kit
- Full FPGA and AVR[®] Source Code Included

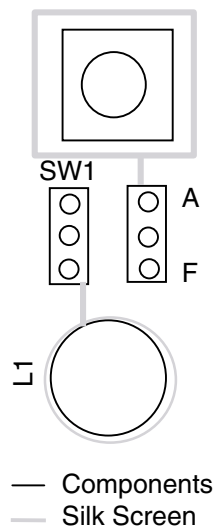
Description

This example demonstrates the reconfiguration process of the FPGA using the built-in Cache Logic Interface. This example takes a simple AND gate implemented in the FPGA and reconfigures the FPGA Core Cell Look-Up Table (LUT) into an OR gate.

The FPSLIC combined Bitstream file is included for convenience.

On the FPSLIC Starter Kit, set the jumpers for SW7, SW8 and L1 to the FPGA side, while SW1 is set to the AVR side, see Figure 1. After power-on-reset (POR) from the Configurator, SW7 and SW8 perform the AND function; the result is displayed on L1. Pressing SW1 initiates an External Interrupt 0 to the AVR, which reconfigures the FPGA from the AVR (internally) and writes an OR gate to the FPGA LUT, previously configured as an AND gate. SW7 and SW8 now perform the OR function; the result is displayed on L1.

Figure 1. ATSTK94 Switch/LED Jumper Settings



Programmable
SLI
AT94K
AT94S

Application
Note



Implementation

Assuming a default System Designer installation, the source files for this application note can be found at the `\SystemDesigner\Examples\AT94K\Designs\doc3013` folder. Alternatively, the source files may be found in the FPSLIC Software section of the Atmel web site (<http://www.atmel.com/atmel/products/prod320.htm>). The contents of `doc3013.zip` are shown in Table 1.

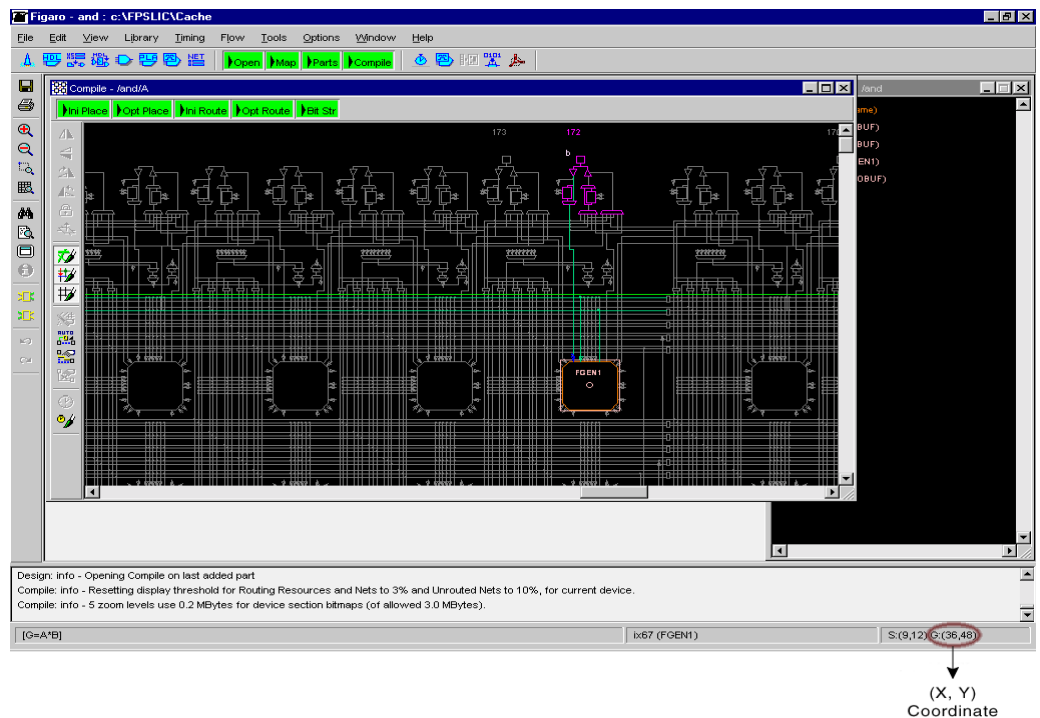
Table 1. Contents of `doc3013.zip`

File	Description
<code>AND.FGD</code>	Previously Compiled AND Gate Design File
<code>AND.PIN</code>	FPGA Pin Lock File for FPSLIC Starter Kit
<code>AND.VHD</code>	FPGA Design Source File
<code>AT94KDEF.INC</code>	Atmel AVR Assembler FPSLIC Include File
<code>CACHE.ASM</code>	AVR Design Source File
<code>FPSLIC_CACHE.BST</code>	FPSLIC Combined Bitstream File

In Figaro, the FPGA Place and Route tool, locate the core cell used to implement the AND gate:

- Go to the **Window** menu and choose **New Compile Window**. The **New Compile** window appears. Use **F7** to zoom in and **F8** to zoom out.
- Place the cursor over the AND gate (on the top edge of the array) to see the (X, Y) coordinates of the core cell location. The coordinates appear on the status bar in the lower right corner of the Figaro window, see Figure 2.

Figure 2. FPGA Place & Route Tool New Compile Window

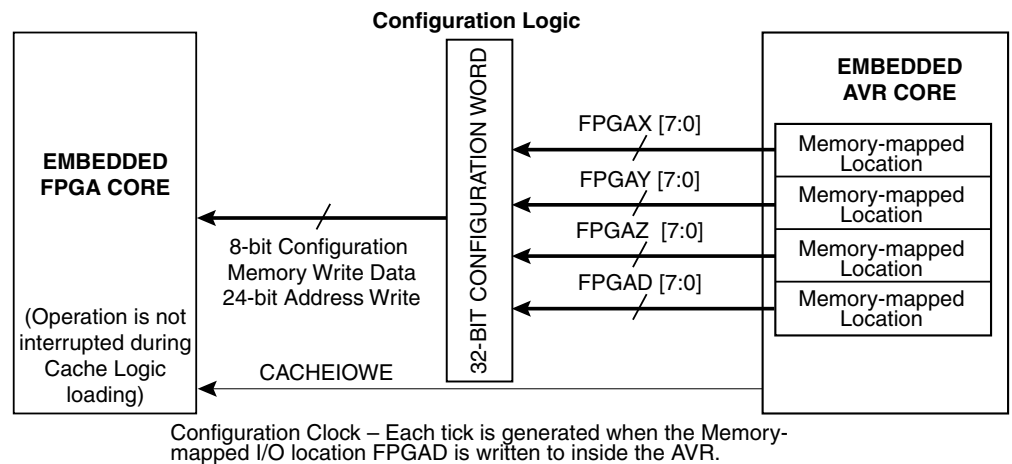


FPSLIC on-chip Partial Reconfiguration

It is then necessary to subtract one from each of these numbers as the actual Core Cells start at (0, 0) not (1, 1) as Figaro does. This yields, in this example, $X = 36 - 1$ and $Y = 48 - 1$.

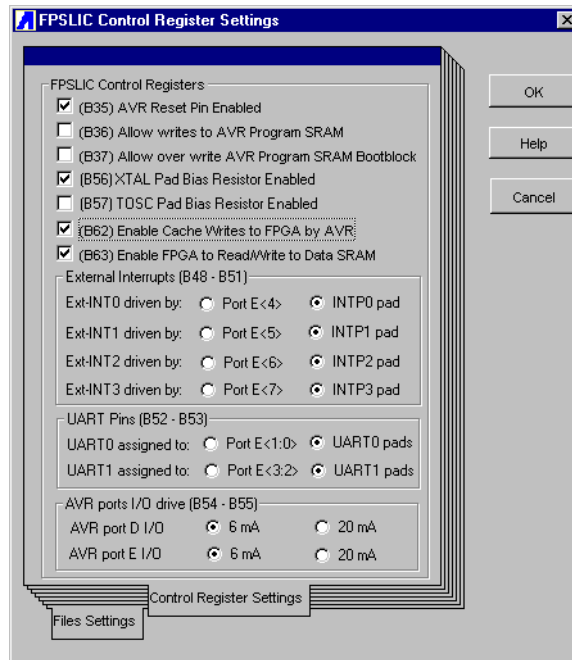
The AVR Assembly file takes the X and Y values and places them in the FPGAX and FPGAY registers, respectively. The FPGAZ and FPGAD values can be obtained from "FPGA Mode 4 Configuration", available under Non-Disclosure Agreement (NDA) from Atmel Corporation. This data is only made available under NDA to protect customers from the reverse engineering of their FPGA designs. The execution of the *out FPGAD, rTemp* instruction initiates the reconfiguration cycle; reconfiguration occurs automatically when the Interrupt Service Routine (ISR) for External Interrupt 0 is executed, see Figure 3.

Figure 3. AVR-FPGA Cache Logic Interface



When the combined Bitstream for the FPSLIC is created using System Designer™, make sure that System Control Register (SCR) Bit 62 is set. The enabling of this bit allows the FPGA to accept Cache Writes from the AVR via the Cache Logic interface, see Figure 4. An FPGA cell can be reconfigured in a very short time with few instructions.

Figure 4. System Designer Control Register Settings





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