PSLI Macro Library

Features

- **Functional Macros**
- **Dynamic Macros**

Description

The Programmable System Level Integrated (PSLI) library of components can be divided into 2 types of macros: functional and dynamic. Functional macros are components with fixed functionality, such as the 2-input AND gate. Dynamic macros are designed to allow user specification of any desired functionality attached as an attribute, via an equation string, on the symbol. This should be used only when a specific function for a core cell is required. Designs targeted to PSLI devices can use a mix of dynamic and functional macros.

The use of the PSLI Macros depends on the design entry method being used. For schematic entry, all of the components shown in this library could be used. For HDL entry (VHDL® or Verilog®), these components would be used by the Synthesis tool when synthesizing from VHDL or Verilog to the PSLI device.

Programmable SLI
AT40K
AT40KAL
AT94K

Application Note

Rev. 2448A–12/01

Functional Macros

Logical Function	Description	Area (x * y)
Gates – NAND		
ND2	2-input NAND	1 x 1
ND2I1	2-input NAND with 1 input inverted	1 x 1
ND2I2	2-input NAND with 2 inputs inverted	1 x 1
ND3	3-input NAND	1 x 1
ND3I1	3-input NAND with 1 input inverted	1 x 1
ND3I2	3-input NAND with 2inputs inverted	1 x 1
ND3I3	3-input NAND with 3 inputs inverted	1 x 1
ND4	4-input NAND	1 x 1
ND4I1	4-input NAND with 1 input inverted	1 x 1
ND4I2	4-input NAND with 2 inputs inverted	1 x 1
ND4I3	4-input NAND with 3 inputs inverted	1 x 1
ND4I4	4-input NAND with 4 inputs inverted	1 x 1
Gates – AND		
AN2	2-input AND	1 x 1
AN2I1	2-input AND with 1 input inverted	1 x 1
AN2I2	2-input AND with 2 inputs inverted	1 x 1
AN3	3-input AND	1 x 1
AN3I1	3-input AND with 1 input inverted	1 x 1
AN3I2	3-input AND with 2 inputs inverted	1 x 1
AN3I3	3-input AND with 3 inputs inverted	1 x 1
AN4	4-input AND	1 x 1
AN4I1	4-input AND with 1 input inverted	1 x 1
AN4I2	4-input AND with 2 inputs inverted	1 x 1
AN4I3	4-input AND with 3 inputs inverted	1 x 1
AN4I4	4-input AND with 4 inputs inverted	1 x 1
Gates – OR		
OR2	2-input OR	1 x 1
OR2I1	2-input OR with 1 input inverted	1 x 1
OR2I2	2-input OR with 2 inputs inverted	1 x 1
OR3	3-input OR	1 x 1
OR3I1	3-input OR with 1 input inverted	1 x 1
OR3I2	3-input OR with 2 inputs inverted	1 x 1
OR3I3	3-input OR with 3 inputs inverted	1 x 1

Functional Macros (Continued)

Logical Function	Description	Area (x * y)
OR4	4-input OR	1 x 1
OR4I1	4-input OR with 1 input inverted	1 x 1
OR4I2	4-input OR with 2 inputs inverted	1 x 1
OR4I3	4-input OR with 3 inputs inverted	1 x 1
OR4I4	4-input OR with 4 inputs inverted	1 x 1
Gates – NOR		
NR2	2-input OR	1 x 1
NR2I1	2-input OR with 1 input inverted	1 x 1
NR2I2	2-input OR with 2 inputs inverted	1 x 1
NR3	3-input OR	1 x 1
NR3I1	3-input OR with 1 input inverted	1 x 1
NR3I2	3-input OR with 2 inputs inverted	1 x 1
NR3I3	3-input OR with 3 inputs inverted	1 x 1
NR4	4-input OR	1 x 1
NR4I1	4-input OR with 1 input inverted	1 x 1
NR4I2	4-input OR with 2 inputs inverted	1 x 1
NR4I3	4-input OR with 3 inputs inverted	1 x 1
NR4I4	4-input OR with 4 inputs inverted	1 x 1
Gates – XOR		
XO2	2-input XOR	1 x 1
XO3	3-input XOR	1 x 1
XO4	4-input XOR	1 x 1
XN2	2-input XNOR	1 x 1
XN3	3-input XNOR	1 x 1
XN4	4-input XNOR	1 x 1
Inverters		
INV	Inverter	1 x 1
Constants		
ONE	Logic one	1 x 1
ZERO	Logic zero	1 x 1
Multiplexers		
MUX2	2 to 1 multiplexer	1 x 1
MUX3	3 to 1 multiplexer	1 x 2
Latches		
LD	D latch transparent High	1 x 1

Functional Macros (Continued)

Logical Function	Description	Area (x * y)
LDRA	D latch transparent High, reset Low	1 x 1
LDSA	D latch transparent High, set Low	1 x 1
LDE	D latch transparent High with enable	1 x 1
Flip-Flops		
FD	D flip-flop	1 x 1
FDRA	D flip-flop, asynchronous reset Low	1 x 1
FDSA	D flip-flop, asynchronous set Low	1 x 1
FDE	D flip-flop with enable	1 x 1
FDRAE	D flip-flop with enable, asynchronous reset Low	1 x 1
FDSAE	D flip-flop with enable, asynchronous set Low	1 x 1
FJK	JK flip-flop	1 x 1
FJKRA	JK flip-flop, asynchronous reset Low	1 x 1
FJKSA	JK flip-flop, asynchronous set Low	1 x 1
Arithmetic Functions		
FA	1-bit full adder	1 x 1
MULT	1-bit multiplier	1 x 1
Tri-State functions		
BUFZ	Tri-state buffer	1 x 1
HZ	Bus driver High or Z	1 x 1
LZ	Bus driver Low or Z	1 x 1
RAM Macros		
RAMS	32 x 4 asynchronous single-port RAM	1 x 1
RAMD	32 x 4 asynchronous dual-port RAM	1 x 1
RAMDSYNC	32 x 4 synchronous dual-port RAM	1 x 1
RAMSSYNC	32 x 4 synchronous single-port RAM	1 x 1

Dynamic Macros

This section describes the dynamic macros for the PSLI. The macros are provided to give the user better control over the implementation of specific functions in a single core cell. It can also be used to simplify the design entry process. Pre-defined attributes with user designated values are used to exploit the logic capabilities of the PSLI core cell. The different pre-defined attributes that can be specified for the dynamic macros[1] are listed below:

- FUNCTIONG
- FUNCTIONH
- CLOCKEDGE
- RSFUNCTION
- RSPOLARITY
- PRESERVE

Note: 1. When dynamic macros are used in a design, the circuit cannot be simulated directly. The circuit must be run through to *Initial Placement* before a functional netlist can be generated.

FUNCTIONG

Description Specifies the equation to be implemented as the G output of the macro.

Value An equation string of one to four variables. Details on the equation syntax are explained in “Equation Syntax” on page 6 of this document.

FUNCTIONH

Description Specifies the equation to be implemented as the H output of the macro.

Value An equation string of one to four variables. Details on the equation syntax are explained in “Equation Syntax” on page 6 of this document.

CLOCKEDGE

Description Specifies the rising edge or falling edge trigger on the clock to which the register responds, see Table 1.

Table 1. CLOCKEDGE Function

Value	Explanation
RISING	Positive edge trigger on the register CLK pin
FALLING	Negative edge trigger on the register CLK pin

RSFUNCTION

Description The register in the PSLI core cell can provide set or reset functions through the RS pin on the dynamic macros, see Table 2.

Table 2. RSFUNCTION

Value	Explanation
RESET	RS functions as reset pin
SET	RS functions as set pin

RSPOLARITY

Description

Specifies the polarity of the RS pin, see Table 3.

Table 3. RSPOLARITY Function

Value	Explanation
HIGH	Active High RS pin
LOW	Active Low RS pin

PRESERVE

Description

Specifies if the component should be preserved by the mapper during technology mapping, see Table 4.

Table 4. PRESERVE Function

Value	Explanation
YES	Do not touch the macro during mapping
NO	Macro can be flattened during mapping

Equation Syntax

The equation string attached to the FUNCTIONG and FUNCTIONH attributes describes the combinatorial behavior of the respective outputs of the core cell. To register and/or tri-state the output of the equation, the correct registered or tri-stated dynamic macros must be used from the library. The equation string is a multi-level sum-of-products equation built using the operators shown in Table 5.

Table 5. Equation Operators

Operators	Description
^, ~	Logical NOT
*, &	Logical AND
|, +	Logical OR
#, @	Logical XOR

The dynamic macro input port names, called A, B, C, and D, are the variables used in the equation. Unconnected input ports are allowed on dynamic macro instances. However, an error will be generated if a port name used in the equation string is not connected to a net. The CLK, RS and OE pins on the register and tri-state dynamic macros should not be used in the equation string.

Table 6 describes the dynamic macros available in the PSLI library.

Table 6. Logical Function

Logical Function	Description
FGEN1	*n* input function generator ($1 \le n \le 4$)
FGEN1F	*n* input function generator with combinatorial feedback ($1 \le n \le 3$)
FGEN1FT	*n* input function generator with combinatorial feedback followed by tri-state buffer ($1 \le n \le 3$)
FGEN1R	*n* input function generator followed by a register ($1 \le n \le 4$)
FGEN1RF	*n* input function generator with registered feedback ($1 \le n \le 3$)
FGEN1RFT	*n* input function generator with registered feedback followed by tri-state buffer($1 \le n \le 3$)
FGEN1RT	*n* input function generator followed by a register and tri-state buffer ($1 \le n \le 4$)
FGEN1T	*n* input function generator followed by a tri-state buffer ($1 \le n \le 4$)
FGEN2	Two *n* input function generators ($1 \le n \le 3$)
FGEN2F	Two *n* input function generators with combinatorial feedback on 1-output($1 \le n \le 2$)
FGEN2FT	Two *n* input function generators with combinatorial feedback followed by tri-state buffer on 1-output ($1 \le n \le 2$)
FGEN2R	Two *n* input function generators with 1-output registered and the other combinatorial ($1 \le n \le 3$)
FGEN2RF	Two *n* input function generators with 1-output registered and feedback ($1 \le n \le 2$)
FGEN2RFT	Two *n* input function generators with 1-output registered, tri-stated and feedback ($1 \le n \le 2$)
FGEN2RT	Two *n* input function generators with 1-output registered and tri-stated ($1 \le n \le 3$)
FGEN2T	Two *n* input function generator with 1-output tri-stated ($1 \le n \le 3$)
MGEN[1]	Two *3*-input function generators
MGENR	Two 3-input function generators with 1-output registered
MGENRT	Two 3-input function generators with 1-output registered and tri-stated
MGENT	Two 3-input function generator with 1-output tri-stated

Note: 1. The MGEN macros are special case macros (typically used in multipliers) with an upstream AND gate feeding the Look-Up Tables.

I/O Macros

This section covers the I/O macros available for the PSLI. In order to specify additional functionality on the I/O, various properties or attributes are used. Different pre-defined attributes can be set on the I/O pads in the PSLI library. Attributes are used on the I/O macros to select the threshold levels, different slew rates etc. The pre-defined attributes that can be specified on the I/O macros are listed below:

- THRESHOLD
- SCHMITT
- SLEWRATE
- EXTRADELAY

THRESHOLD

Description

Specifies the threshold level on the input buffers, see Table 7.

Table 7. THRESHOLD Macro

Value	Explanation
CMOS	CMOS on input
TTL	TTL on input

SCHMITT

Description

Specifies whether a Schmitt trigger circuit on the input pads should be enabled or disabled. The Schmitt trigger is a regenerative comparator circuit to improve the rise and fall times (leading and trailing edges) of the incoming signal, see Table 8.

Table 8. SCHMITT Trigger

Value	Explanation
ENABLE	Enable the schmitt trigger circuit
DISABLE	Disable the schmitt trigger circuit

SLEWRATE

Description

Specifies the output drive, see Table 9.

Table 9. SLEWRATE Macro

Value	Explanation
FAST	Full drive (20 mA buffer)
MEDIUM	Medium drive (14 mA buffer)
SLOW	Standard drive (6 mA buffer)

EXTRADELAY

Description

The input buffers in the PSLI library can have four different intrinsic delays. This attribute lets the user specify an extra delay on the input signal to meet any data hold requirements. A value of ‘0’ provides no extra delay above the intrinsic delay of the input buffer and a value of ‘1’ allows an extra delay of approximately 1 ns above the intrinsic delay, see Table 10 and Table 11.

Table 10. Intrinsic Delays

Value	Explanation
0	No extra intrinsic delay
1	Extra intrinsic delay of approximately 1 ns
3	Extra intrinsic delay of approximately 3 ns
5	Extra intrinsic delay of approximately 5 ns

Table 11. Logical Functions

Logical Function	Description
IBUF	Input buffer
OBUF	Output buffer
OBUFE	Output buffer with active High enable
OBUFOD	Output buffer open drain
OBUFOS	Output buffer open source
BIBUF	Bi-directional buffer
BIBUFOD	Bi-directional buffer open drain
BIBUFOS	Bi-directional buffer open source
GCLKBUF	Global clock buffer
RSBUF	Global reset buffer
FCLKBUF	Fast clock buffer

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