IP Core Generator: Subtractor

Features

- **Subtractor – Carry Select**
- **Subtractor – Ripple Carry**
- **Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices**
- **Carry-in Pin Option**
- **Carry-out Pin Option**
- **Variable Width of Input and Output Vectors**
- **Ripple-carry Subtractor Only**
  - **Register Inputs and Outputs Selection**
  - **Optional Signed Overflow Pin**
  - **Variable Pitch**
  - **Variable Aspect Ratio**

Subtractor – Carry Select

This generator can be used to create an *n* bit carry-select subtractor.

Parameters

Parameter	Value	Explanation
Width	Integer > 1	Width of input and output vectors
Carry In	Boolean	Provides a carry-in pin
Carry Out	Boolean	Provides a carry-out pin

Pins

Type	Name	Option	Explanation
In	CIN	Yes	Carry in
In	DATAA[Width - 1:0]	No	A input
In	DATAB[Width - 1:0]	No	B input
Out	SUM[Width - 1:0]	No	Subtractor output
Out	COUT	Yes	Carry out

Programmable SLI
AT40K
AT40KAL
AT94K

Application Note

Rev. 2447A–12/01

Truth Table

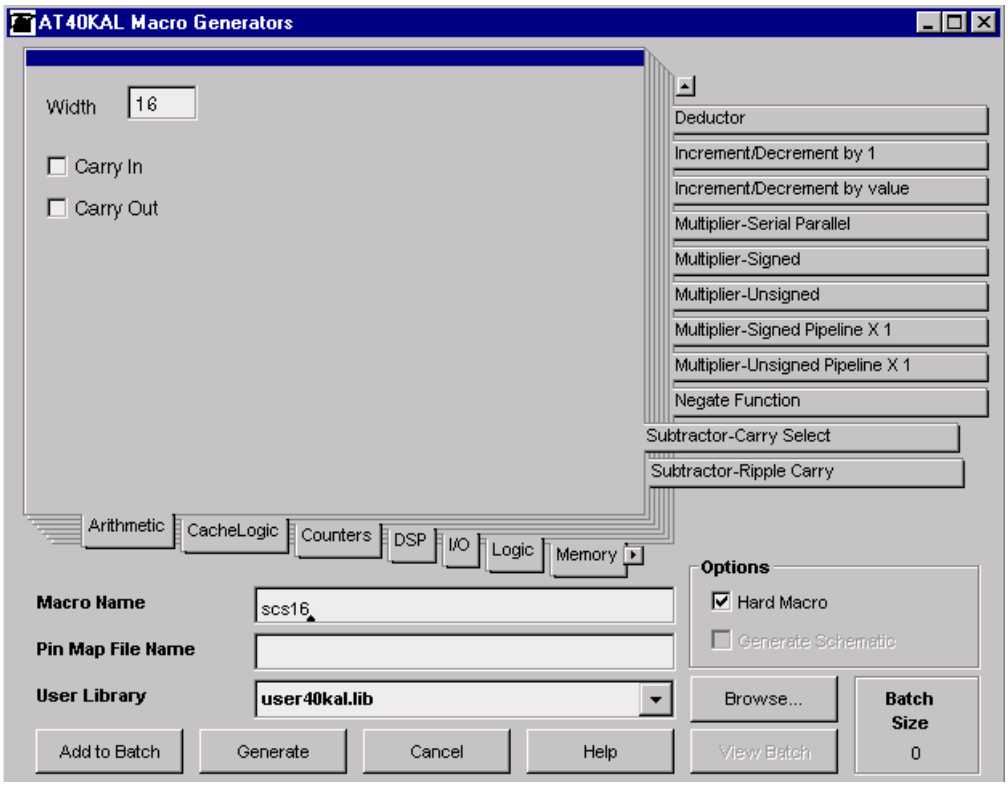
Input			Output	
CIN	DATAA[W - 1:0]	DATAB[W - 1:0]	SUM[W - 1:0]	COUT
C	A	B	A - B - C	1 if A - B - C < 0, 0 otherwise

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	scs16	40.0	25.0	48	3 x 19
AT94K/ AT40KAL	scs16	47.0	21.3	48	3 x 19

Figure 1 shows an example of the scs16 macro options.

Figure 1. Subtractor – Carry Select Generator



Subtractor – Ripple Carry

This generator can be used to create a Ripple-carry Subtractor.

Parameters

Parameter	Value	Explanation
CarryIn	NoRegister	Includes the carry-in pin on the generator, but does not register it
	Register	Registers carry-in of the subtractor
	Disabled	Does not include the carry-in pin on the subtractor
CarryOut	NoRegister	Includes the carry-out pin on the subtractor but does not register it
	Register	Registers carry-out of the subtractor
	Disabled	Does not include the carry-out pin on the subtractor
Register	None	Does not register the inputs and outputs
	Input	Registers inputs on the subtractor, and excludes carry-in pin
	Output	Registers outputs on the subtractor, and excludes carry-out pin
	Both	Registers both inputs and outputs including the carry-in and carry-out pins of the subtractor
Signed Overflow Pin	Boolean	Provides a signed overflow output (treating input vectors as signed values)
Pitch	Integer > 1	Spacing between input pins, pitch of 2 means one cell between input pins.
Width	Integer > 1	Width of input and output vectors
Aspect Ratio	Float ≥ 0.0	Aspect ratio of the subtractor layout. A ratio of 0:0 gives a thin, vertical layout; whereas a ratio of 1:0 gives a square layout.

If input, output, carry-in or carry-out registers are selected, three additional parameters are available.

Register Parameters

Parameter	Value	Explanation
Invert Clock	Boolean	Inverts the register clock
Initialization Polarity = Low	Boolean	Makes register initialization active low
Register Set/ Reset Function	Reset	Registers can be reset to zero
	Set	Registers can be set to one

Pins

Type	Name	Option	Explanation
In	CIN	Yes	Carry in
In	DATAA[Width - 1:0]	No	A input
In	DATAB[Width - 1:0]	No	B input
In	CLK/CLKN	Yes	Clock (noninverted/inverted)
In	R/RN/S/SN	Yes	Reset/set (active high/low)
Out	SUM[Width - 1:0]	No	Adder output
Out	COUT	Yes	Carry out (cannot be used with overflow in an unsigned adder)
Out	OVERFLOW	Yes	Overflow

Carry out = DATAA - DATAB - CIN > 2^n - 1 or

DATAA - DATAB - CIN < -2^n

Overflow for Unsigned

DATAA - DATAB - CIN > 2^n - 1 or

DATAA - DATAB - CIN < 0

Overflow for Signed

DATAA - DATAB - CIN > 2^n - 1 or

DATAA - DATAB - CIN < -2^n

Truth Table

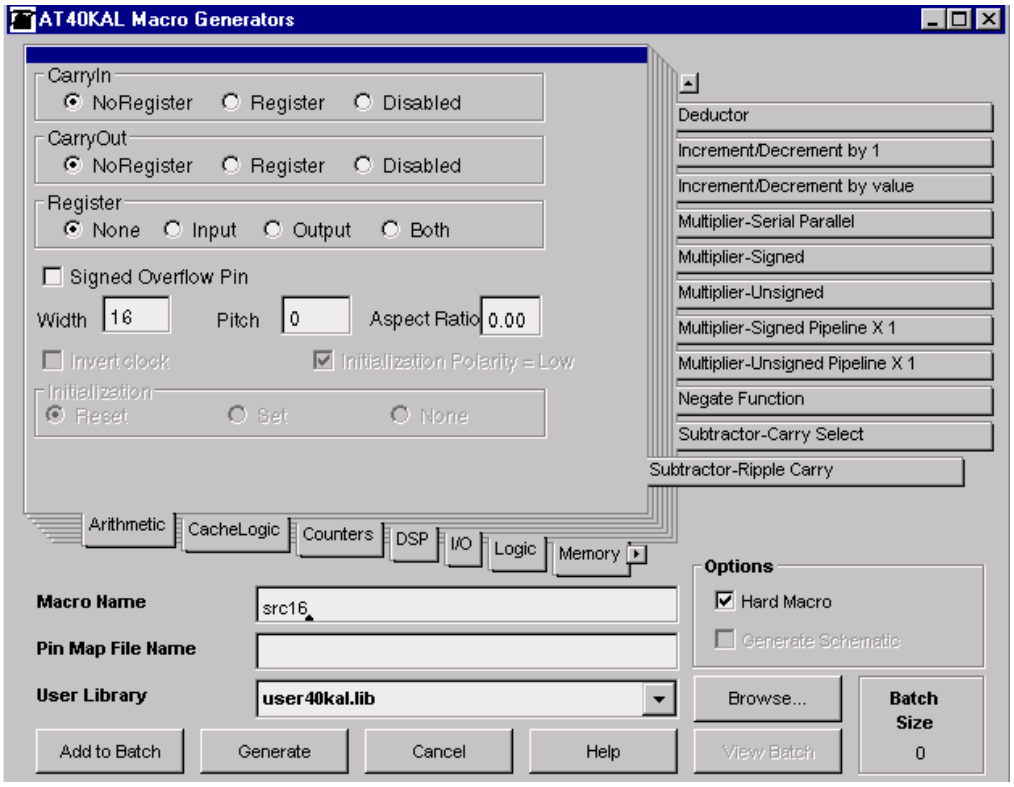
Input			Output	
CIN	DATAA[W - 1:0]	DATAB[W - 1:0]	SUM[W - 1:0]	COUT
C	A	B	A - B - C	1 if A - B - C < 0, 0 otherwise

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	src16	36.2	27.7	16	1 x 16
AT40K	src8	69.2	14.5	8	1 x 8
AT94K/ AT40KAL	src16	49.9	20.1	16	1 x 16
AT94K/ AT40KAL	src8	95.6	10.5	8	1 x 8

Figure 2 shows an example of the src16 macro options.

Figure 2. Subtractor – Ripple Carry Generator



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