IP Core Generator: Pulse Generator

Features

- **Pulse Generator – Fixed**
- **Pulse Generator – Loadable**
- **Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices**
- **Variable Pitch**
- **Clock Inversion Capability**
- **Initialization Polarity Selection**
- **Fixed Pulse Generator Only**
  - **Variable Output Clock Cycles**
  - **Initialization Radix of Above Value Selection**
- **Loadable Pulse Generator Only**
- **Variable Width of Pulse Generator**

Pulse Generator – Fixed

This can be used to create a pulse generator that asserts its output once every *n* clock cycles, where *n* is a fixed value specified by the user.

Parameters

Parameter	Value	Explanation
Generate a Pulse Every *n* Clock Cycles	Integer > 1	Output will be low for *n* - 1 clock cycle, then high for 1 clock cycle, in a repeating pattern
Radix of Above Value	Binary	*n* is specified in binary representation
	Octal	*n* is specified in octal representation
	Decimal	*n* is specified in decimal representation
	Hex	*n* is specified in hexadecimal representation
Pitch	Integer ≥ 1	Spacing between cells in the pulse generator. A pitch of 2 doubles the size of the generator by spreading out its layout.
Invert Clock	Boolean	Inverts the clock input
Initialization Polarity = Low	Boolean	Preset input is active low

Programmable SLI
AT40K
AT40KAL
AT94K

Application Note

Rev. 2443A–12/01

Pins

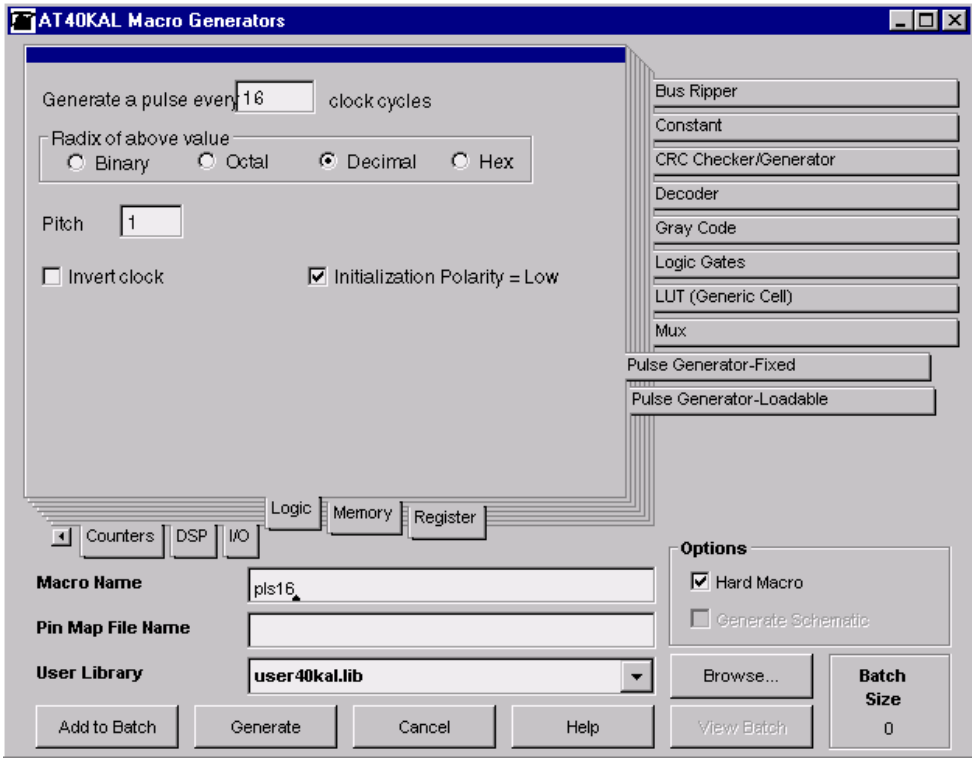
Type	Name	Option	Explanation
In	CLK/CLKN	No	Clock (noninverted/inverted)
In	P/PN	No	Preset to starting value (active high/low)
Out	TERMCNT	No	Terminal count (pulse output)

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	pls16	133.7	7.5	5	1 x 5
AT40K	pls8	171.5	5.8	4	1 x 4
AT94K/ AT40KAL	pls16	141.4	7.1	5	1 x 5
AT94K/ AT40KAL	pls8	171.5	5.8	4	1 x 4

Figure 1 shows an example of the pls16 macro options.

Figure 1. Pulse Generator – Fixed



Pulse Generator – Loadable

This can be used to create a pulse generator that asserts its output once every *n* clock cycles, where *n* is a value that is loaded into the macro at run-time. Performing a parallel load operation modifies the value of *n*, i.e., the pulse frequency.

Parameters

Parameter	Value	Explanation
Width	Integer > 1	Width of the pulse generator (i.e., the number of registers it contains). This parameter dictates the maximum size of *n* that can be loaded into the macro.
Pitch	Integer ≥ 1	Spacing between cells in the pulse generator. A pitch of 2 doubles the size of the generator by spreading out its layout.
Invert Clock	Boolean	Inverts the clock input
Initialization Polarity = Low	Boolean	Reset input is active low

Pins

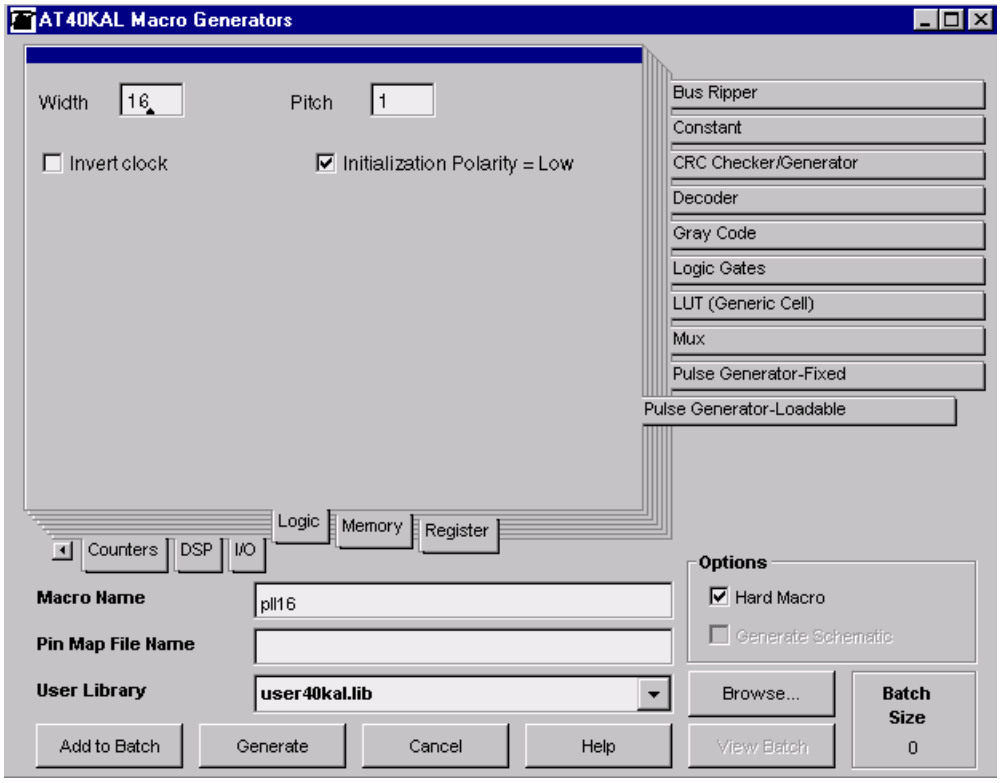
Type	Name	Option	Explanation
In	SLOAD	No	0 = Load pulse frequency value; 1 = Generate pulses
In	DATA[Width - 1:0]	No	Parallel load inputs for pulse frequency value
In	CLK/CLKN	No	Clock (noninverted/inverted)
In	R/RN	No	Reset (active high/low)
Out	TERMCNT	No	Terminal count (pulse output)

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	pll16	20.3	49.3	48	3 x 17
AT40K	pll8	38.6	25.9	24	3 x 9
AT94K/ AT40KAL	pll16	25.2	39.8	48	3 x 17
AT94K/ AT40KAL	pll8	47.9	20.9	24	3 x 9

Figure 2 shows an example of the pll16 macro options.

Figure 2. Pulse Generator – Loadable



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