

IP Core Generator: Negate Function

Features

- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Optional Overflow Output Pin
- Variable Width of Input and Output Data
- Variable Number of Inputs per Mux

Description

The Negate Function generator can be used to create a two's complement function implemented in a ripple carry manner.

if $DATA = 2^{(Width - 1)}$, then

OVERFLOW = 1, RESULT = -DATA

else

RESULT = -DATA

DATA must always represent a positive number and the RESULT is always a two's complement number.

Parameters

Parameter	Value	Explanation
Overflow	Boolean	Overflow output pin is present
Width	Integer > 1	Width of input and output data

Pins

Type	Name	Option	Explanation
In	DATA[Width - 1:0]	No	Data input
Out	RESULT	No	Data output = two's complement of data
Out	OVERFLOW	Yes	1 if data = $2^{(Width - 1)}$, 0 otherwise



Programmable
SLI
AT40K
AT40KAL
AT94K

Application
Note

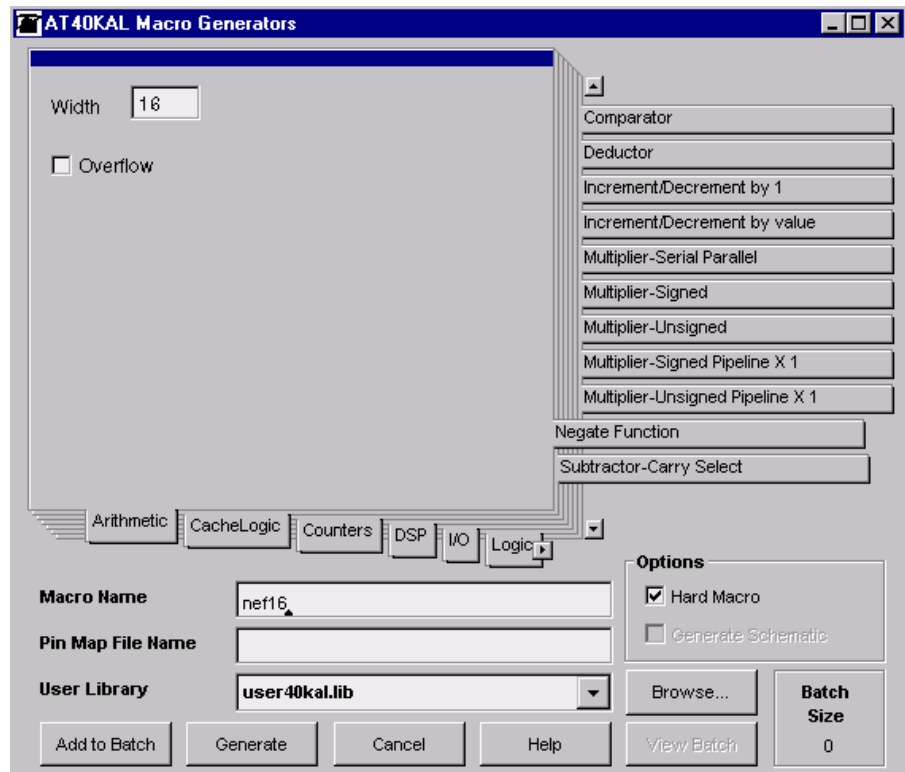


Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	nef16	36.4	27.4	16	1 x 16
AT40K	nef8	70.2	14.2	8	1 x 8
AT94K/ AT40KAL	nef16	51.4	19.4	16	1 x 16
AT94K/ AT40KAL	nef8	101.6	9.8	8	1 x 8

Figure 1 shows an example of the nef16 macro options.

Figure 1. Negate Function Generator





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