
IP Core Generator: Look-Up Table

Features

- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Look-Up Table Selection
- Tri-state Control Selection
- Variable Number of Look-Up Tables
- Variable Pitch of Generic Cells
- Internal Feedback Capability
- Function G Capability
- Function H Capability
- Optional Register
- Clock Inversion Capability
- Initialization Polarity Selection
- Initialization Selection
- Initialization Value Radix Selection

Description

The Look-Up Table (LUT), or Generic Cell generator can be used as a convenient interface for generating components using the FGENxx and MGENxx generic cell components in the AT40K macro library. The generator allows complete control over the function of an AT40K core cell, and it allows this function to be replicated n times.



**Programmable
SLI
AT40K
AT40KAL
AT94K**

**Application
Note**

Rev. 2439A-1/02



Parameters

Parameter	Value	Explanation
LUT Type	4-input LUT	Configure each cell in the macro as an FGEN1-type component, with a single 4-input LUT.
	2 x 3-input LUT	Configure each cell in the macro as an FGEN2-type component, with two 3-input LUT sharing common inputs.
	4-input LUT with AND gate	Configure each cell in the macro as an MGEN-type component, with a single 4-input LUT and an upstream AND gate.
Tri-state Control	None	Cells have no tri-state control
	Group OE pin	A single OE pin is used to tri-state the outputs of all cells
	Individual OE pins	Each cell has its own tri-state control
Number of LUTs	Integer > 0	Number of generic cells to be included in the macro, each cell is configured identically
Pitch	Integer > 0	Spacing between generic cells
Internal Feedback	Boolean	Program the cell to include internal feedback (FB input). This reduces the number of external inputs to the cell by one. Not available for 1 x 4-input LUT with AND gate.
Function G	String	Equation string used to specify the function of the G cell output, in terms of A, B, C, D and FB (if feedback option is selected).
Function H	String	Equation string used to specify the function of the H cell output, in terms of A, B, C, D and FB (if feedback option is selected).
Register	Boolean	Include a register in the cell

If the register option is selected, the following additional parameters are available:

Register Parameters

Parameter	Value	Explanation
Invert Clock	Boolean	Invert the clock input
Initialization Polarity = Low	Boolean	Reset/Set/Preset input is active low
Initialization	Reset	Registers can be reset to zero
	Set	Registers can be set to one
	None	Registers are automatically reset on power-up
	Preset	Registers can be asynchronously loaded with a constant value

Register Parameters (Continued)

Parameter	Value	Explanation
Initialization Value Radix	Binary	Initialization value is specified using binary representation
	Octal	Value is specified in octal
	Decimal	Value is specified in decimal
	Hex	Value is specified in hexadecimal

Pins

Type	Name ⁽¹⁾	Option	Explanation
In	A[N - 1:0]	No	Data input A (must always be used in equation)
In	B[N - 1:0]	Yes	Data input B
In	C[N - 1:0]	Yes	Data input C
In	D[N - 1:0]	Yes	Data input D
Out	G[N - 1:0]	No	Data output
Out	H[N - 1:0]	Yes	Data output
In	OE	Yes	Group output enable pin
In	OE[N - 1:0]	Yes	Individual output enable pins
In	CLK/CLKN	No	Clock pin (noninverted/inverted)
In	R/RN/S/SN/P/PN	No	Reset/Set/Preset (active high/low)

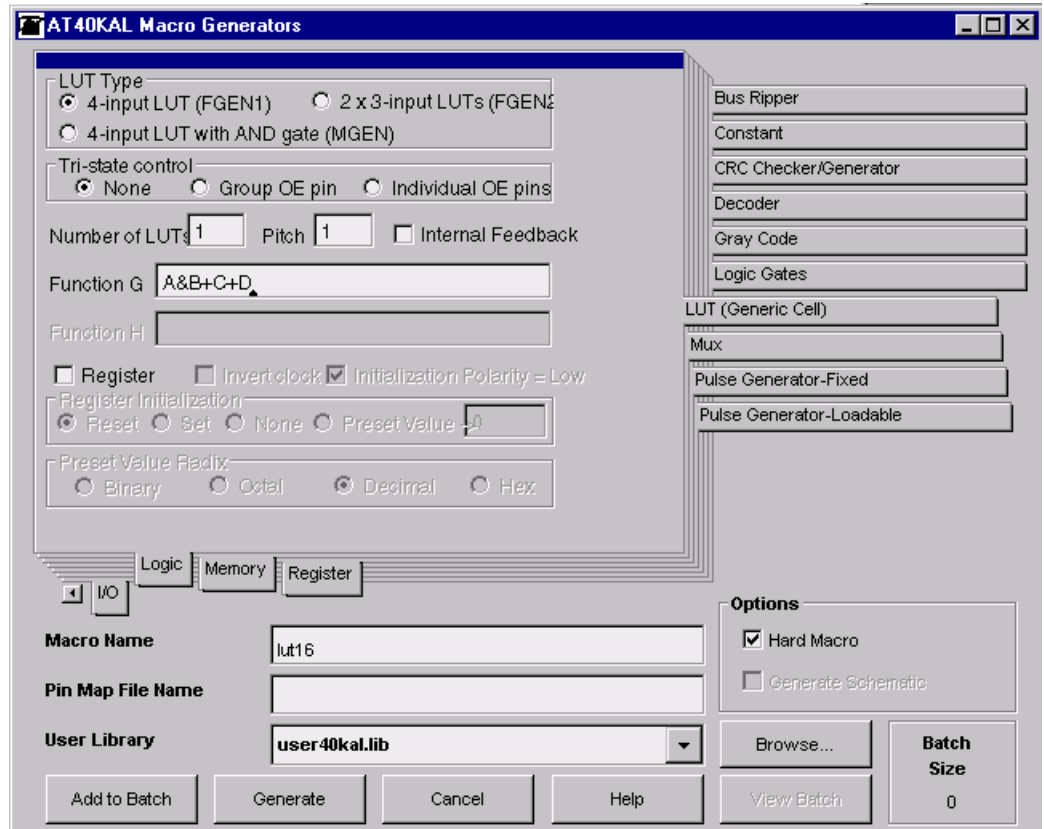
Note: 1. N stands for the number of generic cells in the macro.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	lut16	339.0	3.0	16	1 x 16
AT40K	lut8	339.0	3.0	8	1 x 8
AT40KAL/ AT94KAL	lut16	492.6	2.0	16	1 x 16
AT40KAL/ AT94KAL	lut8	492.6	2.0	8	1 x 8

Figure 1 shows an example of the lut16 macro options.

Figure 1. Look-Up Table Generator





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