IP Core Generator: Logic Gates

Features

- **Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices**
- **Variable Width of Input and Output Data**
- **Variable Pitch of Input Pins**
- **Latch Enable Selection**
- **Tri-state Control Selection**
- **Reset/Set/Preset Pin Selection**
- **Asynchronous Initialization Selection**
- **Initialization Value Radix Selection**

Description

A variety of Logic Gates can be generated, each with a programmable number of inverted inputs.

Parameters

Parameter	Value	Explanation
Gate Type	AND	AND gates
	NAND	NAND gates
	OR	OR gates
	NOR	NOR gates
	XOR	Exclusive OR gates
	XNOR	Exclusive NOR gates
	INV	Inverter gates
Number of Gates	Integer > 0	Number of gates in component
Number of Inputs per Gate	Integer > 0	Width of input vector for each gate
Number of Inverted Inputs per Gate	Integer > 0	Number of inputs that are inverted on each gate. The inverted inputs start from the first input to the gate and count up.
Common Input	Boolean	Select this option if a common input should be supplied to each of the gates

Programmable SLI
AT40K
AT40KAL
AT94K

Application Note

Rev. 2438A–1/02

Pins

Type	Name	Option	Explanation
In	DATA[S - 1:0]_[W - 1:0]	No	Gate input pin where S(1) goes from 0 to Size and W(2) goes from 0 to Width
Out	RESULT[S - 1:0]	No	Gate output
In	COMMON_DATA	Yes	Common input Enable pin for each of the gates

Notes: 1. S stands for Size (number of gates).
2. W stands for Width (number of inputs per gate).

Truth Table

Type	Name(1)	Explanation(2)
AND	DATA[S - 1:0]_[W - 1:0]	DATA0 * DATA1 ... * DATAW - 1
INV	DATA[S - 1:0]_[W - 1:0]	~DATA0, ~DATA1, ... ~DATAS - 1
NAND	DATA[S - 1:0]_[W - 1:0]	~(DATA0 * DATA1 ... * DATAW - 1)
NOR	DATA[S - 1:0]_[W - 1:0]	~(DATA0 + DATA1 ... + DATAW - 1)
OR	DATA[S - 1:0]_[W - 1:0]	DATA0 + DATA1 ... + DATAW - 1
XOR	DATA[S - 1:0]_[W - 1:0]	DATA0 ^ DATA1 ... ^ DATAW - 1
XNOR	DATA[S - 1:0]_[W - 1:0]	~(DATA0 ^ DATA1 ... ^ DATAW - 1)

Notes: 1. S stands for Size (number of gates).
2. W stands for Width (number of inputs per gate).

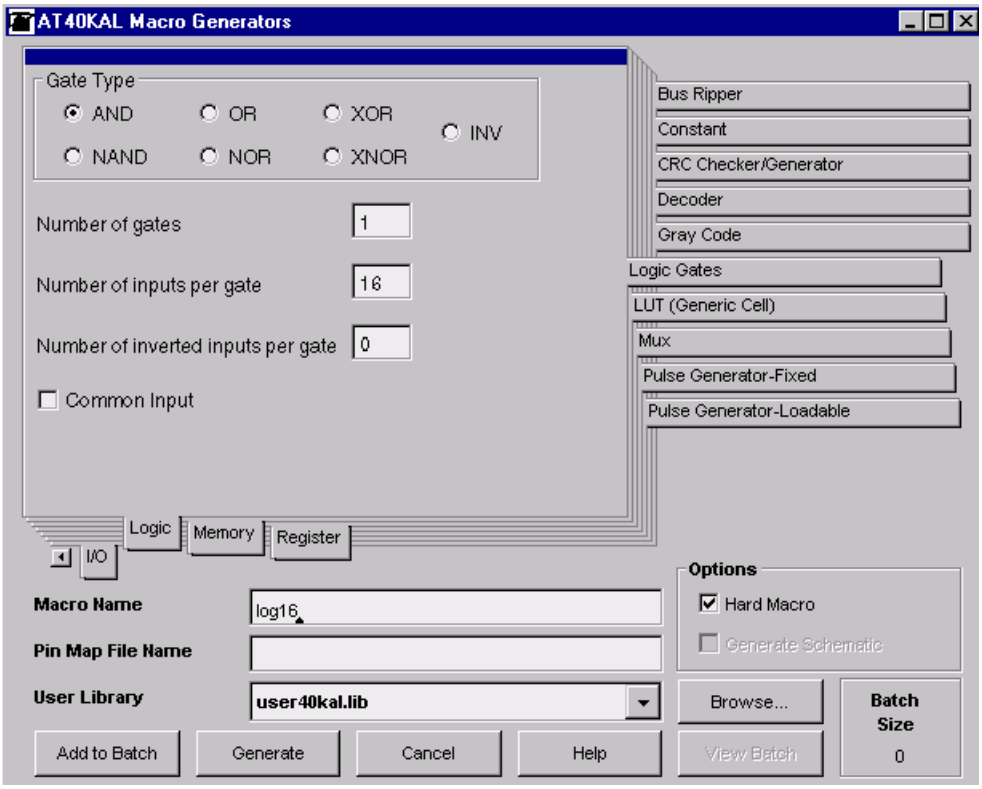
If the inverter function is selected, or the gate width is 2, the macro must be generated as a soft macro (i.e., with the Hard macro option deselected). This is to ensure the most efficient implementation of the logic as small gates are better handled by the Mapper in Figaro and cannot be effectively implemented as a hard macro.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	log16	96.9	10.4	6	4 x 2
AT40K	log8	189.9	5.3	3	3 x 2
AT40KAL/ AT94KAL	log16	138.9	7.2	6	4 x 2
AT40KAL/ AT94KAL	log8	304.9	3.3	3	3 x 2

Figure 1shows an example of the log16 macro options.

Figure 1. Logic Gates Generators



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