
IP Core Generator: Transparent Latch

Features

- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Variable Width of Input and Output Data
- Variable Pitch of Input Pins
- Latch Enable Selection
- Tri-state Control Selection
- Reset/Set/Preset Pin Selection
- Asynchronous Initialization Selection
- Initialization Value Radix Selection

Description

The Latch generator can be used to create a D-type transparent latch.



**Programmable
SLI
AT40K
AT40KAL
AT94K**

**Application
Note**

Rev. 2437B-1/02



Parameters

Parameter	Type	Explanation
Width	Integer > 0	Width of the input and output data
Pitch	Integer > 0	Spacing between input pins. Pitch of 2 means one cell between inputs
Latch Enable	Group Enable	One enable pin controls all latches
	Individual Enables	Each latch has its own enable input
Tri-state Control	None	Latch outputs are not tri-stated
	Group OE pin	Latch outputs are tri-stated and controlled from a single OE pin
	Individual OE pins	Each latch has its own OE pin to control the tri-stating of its outputs
Active Low Set/Reset	Boolean	Reset/Set/Preset input is active low
Asynchronous Initialization	Reset	Latches can be reset to zero
	Set	Latches can be set to one
	None	Latches are automatically reset on power-up
	Preset	Latches can be asynchronously loaded with a constant value
Initialization Value Radix	Binary	Initialization values are specified using binary representation
	Octal	Values are specified in octal
	Decimal	Values are specified in decimal
	Hex	Values are specified in hexadecimal

Pins

Type	Name	Option	Explanation
In	DATA[Width - 1:0]	No	Data input to the D-type latches
In	ENABLE	Yes	Common Latch Enable input (1 = flow-through, 0 = latch)
In	ENABLE[Width - 1:0]	Yes	Individual Latch Enable inputs (1 = flow-through, 0 = latch)
In	OE	Yes	Common Output Enable input (0 = tri-state)
In	OE[Width - 1:0]	Yes	Individual Output Enable inputs (0 = tri-state)
In	R/RN/S/SN/P/PN	Yes	Reset/Set/Preset (active high/low)
Out	Q[Width - 1:0]	No	Data output from D-type latches

Statistics

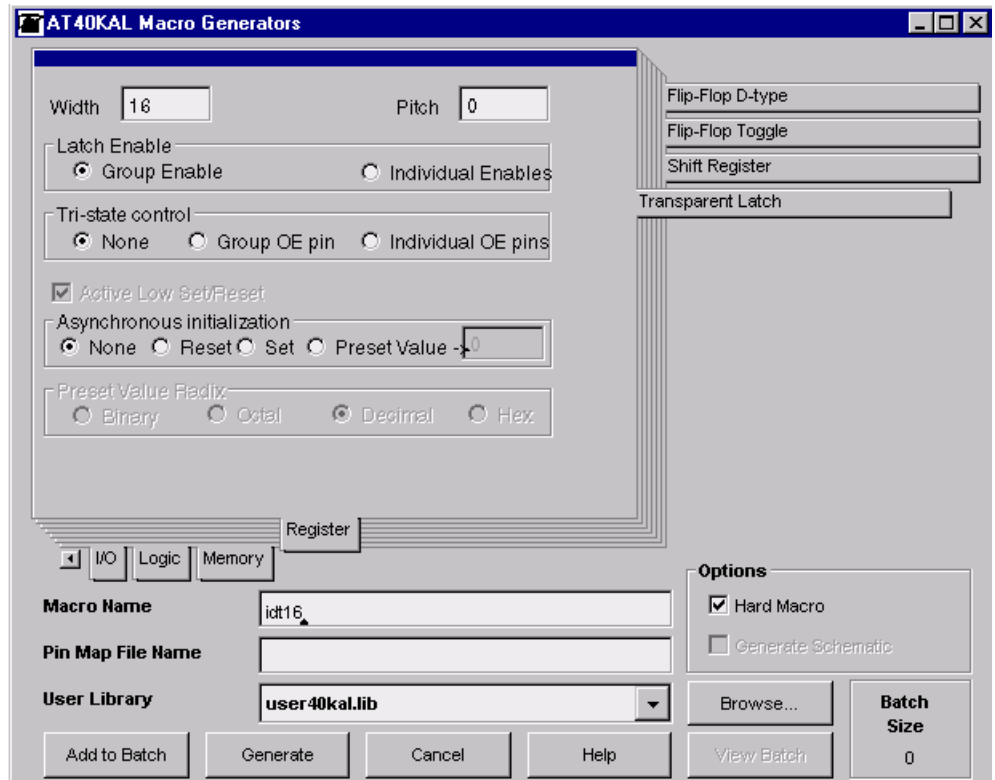
Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
ldt16	476.2	2.1	16	1 x 16
ldt8	476.2	2.1	8	1 x 8

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	ldt16	476.2	2.1	16	1 x 16
AT40K	ldt8	476.2	2.1	8	1 x 8
AT40KAL/ AT94KAL	ldt16	719.4	1.4	16	1 x 16
AT40KAL/ AT94KAL	ldt8	719.4	1.4	8	1 x 8

Figure 1 shows an example of the ldt16 macro options.

Figure 1. Latch – Transparent Generator





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