

IP Core Generator: Gray Code

Features

- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Function Code Selection
- Variable Width of Input and Output Data

Description

The Gray Code generator can be used to convert binary code to gray code or gray code to binary code respectively.

Parameters

Parameter	Value	Explanation
Function	ToGray	Converts the binary code input to gray code
	ToBinary	Converts the gray code input to binary code
Width	Integer > 1	Width of input and output data

Pins

Type	Name	Option	Explanation
In	DATA[Width - 1:0]	No	Input data to be converted
Out	OUT[Width - 1:0]	No	Output bits

Truth Table

Input		Output
Binary	DATA[W - 1:0]	DATAW, DATA[W - 1] xor DATAW, DATA[W - 2] xor DATA[W - 1],...
Gray	DATA[W - 1:0]	DATAW, DATA[W - 1] xor DATAW, DATA[W - 2] xor DATA[W - 1] xor DATAW, ...



**Programmable
SLI
AT40K
AT40KAL
AT94K**

**Application
Note**

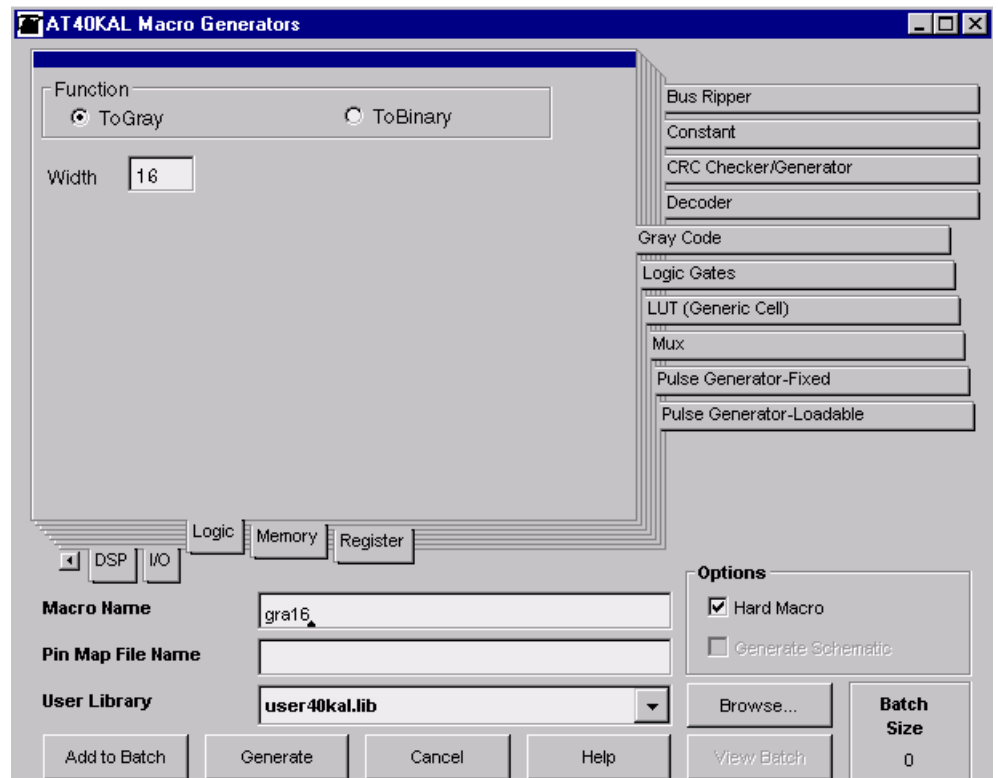


Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	gra16	423.7	2.4	8	1 x 8
AT40K	gra8	423.7	2.4	4	1 x 4
AT40KAL/ AT94KAL	gra16	543.5	1.8	8	1 x 8
AT40KAL/ AT94KAL	gra8	543.5	1.8	4	1 x 4

Figure 1 shows an example of the gra16 macro options.

Figure 1. Gray Code Generator





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