IP Core Generator: Flip-Flop

Features

- **Flip-Flop – D-Type**
- **Flip-Flop – Toggle**
- **Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices**
- **Register Bank Enable Selection**
- **Tri-state Control Selection**
- **Variable Width of Input and Output Data**
- **Variable Pitch of Input Pins**
- **Variable Clock Inversion Capability**
- **Initialization Polarity Selection**
- **Asynchronous Initialization Selection**
- **Synchronous Initialization Selection**
- **Initialization Value Radix Selection**

Flip-Flop – D-Type

The D Flip-Flop generator can be used to create a register bank consisting of D-type flip-flops.

Programmable SLI
AT40K
AT40KAL
AT94K

Application Note

Rev. 2434B–1/02

Parameters

Parameter	Value	Explanation
Register Bank Enable	None	No register enable control is provided
	Group Enable	A single enable input is used to control all flip-flops
	Individual Enables	Each flip-flop in the register bank has its own enable control
Tri-state Control	None	Register bank has no tri-state control
	Group OE pin	A single OE pin is used to tri-state the outputs of all flip-flops
	Individual OE pins	Each flip-flop has its own tri-state control
Width	Integer > 0	Width of the input and output data
Pitch	Integer > 0	Spacing between input pins. Pitch of 2 means one cell between inputs
Invert Clock	Boolean	Inverts the clock input
Initialization Polarity = Low	Boolean	Reset/Set/Preset input is active low
Asynchronous Initialization	Reset	Registers can be reset to zero
	Set	Registers can be set to one
	None	Registers are automatically reset on power-up
	Preset	Registers can be asynchronously loaded with a constant value
Synchronous Initialization	None	Registers have synchronous initialization capability
	Auxiliary Input	Registers have a second data input that can be used to synchronously preset them to any value
	Constant Value	Registers can be synchronously preset with a user-supplied constant value
Initialization Value Radix	Binary	Initialization values are specified using binary representation
	Octal	Values are specified in octal
	Decimal	Values are specified in decimal
	Hex	Values are specified in hexadecimal

Pins

Type	Name	Option	Explanation
In	DATA[Width - 1:0]	No	Data input
In	CLK/CLKN	No	Clock pin (noninverted/inverted)
Out	Q[Width - 1:0]	No	Data output
In	ENABLE	Yes	Group enable input
In	ENABLE[Width - 1:0]	Yes	Individual enable inputs
In	LOAD	Yes	Perform synchronous initialization
In	LOADDATA[Width - 1: 0]	Yes	Data input for synchronous initialization
In	OE	Yes	Group tri-state control input
In	OE[Width - 1:0]	Yes	Individual tri-state control inputs
In	R/RN/S/SN/P/PN	No	Reset/Set/Preset (active high/low)

Truth Table(1)

Input				Output(2)
RN	DATA[W - 1:0]	CLK	ENABLE	Q[W - 1:0]
0	X	X	X	0
1	X	0>1	X	No Change
1	0	0>1	1	0
1	1	0>1	1	1
1	X	0>1	1	Q(I) = Q - (I - 1) Q(0) = SI

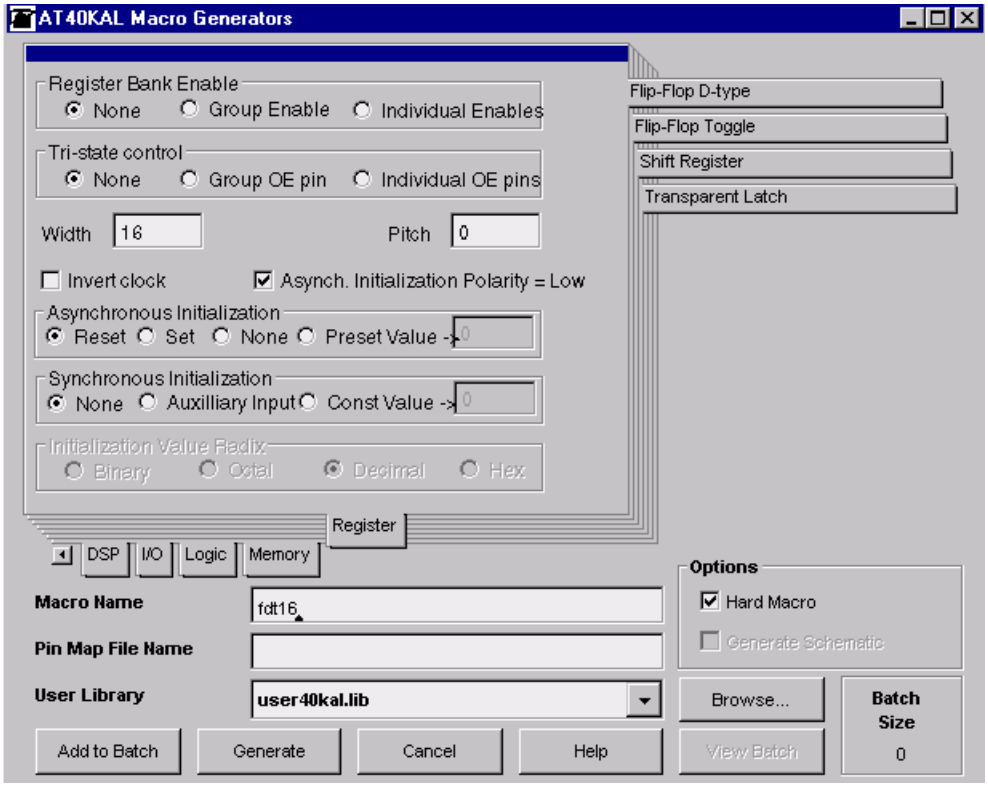
Notes: 1. This Truth Table assumes that an active-low reset and noninverted clock have been selected.
2. Q - is the value of Q preceding the clock transition.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	fdt16	565.0	1.8	16	1 x 16
AT40K	fdt8	565.0	1.8	8	1 x 8
AT40KAL/ AT94KAL	fdt16	598.8	1.7	16	1 x 16
AT40KAL/ AT94KAL	fdt8	598.8	1.7	8	1 x 8

Figure 1 shows an example of the fdt16 macro options.

Figure 1. Flip-Flop – D-Type Generator



Flip-Flop – Toggle

The Toggle Flip-Flop generator can be used to create a register bank consisting of T-type (toggle) flip-flops.

Parameters

Parameter	Value	Explanation
Register Bank Enable	None	No register enable control is provided
	Group Enable	A single enable input is used to control all flip-flops
	Individual Enables	Each flip-flop in the register bank has its own enable control
Tri-state Control	None	Register bank has no tri-state control
	Group OE pin	A single OE pin is used to tri-state the outputs of all flip-flops
	Individual OE pins	Each flip-flop has its own tri-state control
Width	Integer > 0	Width of the input and output data
Pitch	Integer > 0	Spacing between input pins. Pitch of 2 means one cell between inputs.
Invert Clock	Boolean	Inverts the clock input
Initialization Polarity = Low	Boolean	Reset/Set/Preset input is active low
Asynchronous Initialization	Reset	Registers can be reset to zero
	Set	Registers can be set to one
	None	Registers are automatically reset on power-up
	Preset	Registers can be asynchronously loaded with a constant value
Synchronous Initialization	None	Registers have synchronous initialization capability
	Auxiliary Input	Registers have a second data input that can be used to synchronously preset them to any value
	Constant Value	Registers can be synchronously preset with a user-supplied constant value
Initialization Value Radix	Binary	Initialization values are specified using binary representation
	Octal	Values are specified in octal
	Decimal	Values are specified in decimal
	Hex	Values are specified in hexadecimal

Pins

Type	Name	Option	Explanation
In	DATA[Width - 1:0]	No	Data input
In	CLK/CLKN	No	Clock pin (noninverted/inverted)
Out	Q[Width - 1:0]	No	Data output
In	ENABLE	Yes	Group enable input
In	ENABLE[Width - 1:0]	Yes	Individual enable inputs
In	LOAD	Yes	Performs synchronous initialization
In	LOADDATA[Width - 1: 0]	Yes	Data input for synchronous initialization
In	OE	Yes	Group tri-state control input
In	OE[Width - 1:0]	Yes	Individual tri-state control inputs
In	R/RN/S/SN/P/PN	No	Reset/Set/Preset (active high/low)

Truth Table(1)

Input				Output(2)
RN	DATA[W - 1:0]	CLK	ENABLE	Q[W - 1:0]
0	X	X	X	0
1	X	0>1	0	No Change
1	0	0>1	1	Q
1	1	0>1	1	~Q

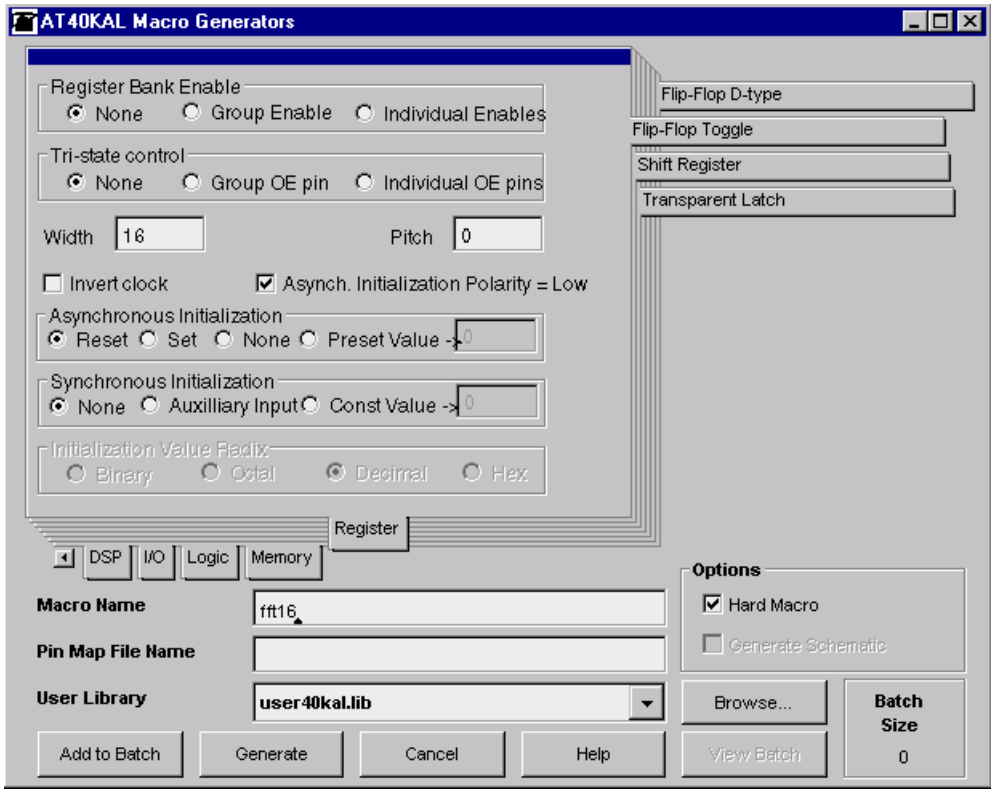
Notes: 1. This Truth Table assumes that an active-low reset and non inverted clock have been selected.
2. Q - is the value of Q preceding the clock transition.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	fft16	565.0	1.8	16	1 x 16
AT40K	fft8	565.0	1.8	8	1 x 8
AT40KAL/ AT94KAL	fft16	598.8	1.7	16	1 x 16
AT40KAL/ AT94KAL	fft8	598.8	1.7	8	1 x 8

Figure 2 shows an example of the fft16 macro options.

Figure 2. Flip-Flop – Toggle Generator



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