IP Core Generator: FIFO

Features

- **Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices**
- **Variable Width of Parallel Input and Output Data**
- **Variable Depth of FIFO**
- **Variable Clock Inversion Capability**

Description

This generator creates a First-In First-Out (FIFO) buffer that makes use of the RAM cells in the AT40K Series architecture to produce a compact implementation with no read or write latency. In order to make efficient use of the RAM cells, some restrictions are placed on the data width and FIFO depth parameters: the data width must be a multiple of 4, and the FIFO depth is rounded up to the nearest power of 2.

The Read Enable (REN) and Write Enable (WEN) pins control the FIFO operation. When the WEN pin is asserted (i.e. pulled low), the buffer is in the write mode. Data presented at the D bus will be written into the FIFO until the FULL pin goes low, indicating that the FIFO cannot accept any more data. When the REN pin is asserted, the FIFO is in the read mode. Data can be read from the Q bus until the EMPTY pin goes low, indicating that no more data is present in the buffer. When REN and WEN are both high, operation of the FIFO is effectively suspended.

Parameters

Parameter	Value	Explanation
Data Width	Integer ≥ 4	Width of parallel input and output data (must be a multiple of 4)
Depth	Integer > 2	FIFO depth (rounded up to the nearest power of 2)
Invert Clock	Boolean	Invert the polarity of the clock input

Programmable SLI
AT40K
AT40KAL
AT94K

Application Note

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Pins

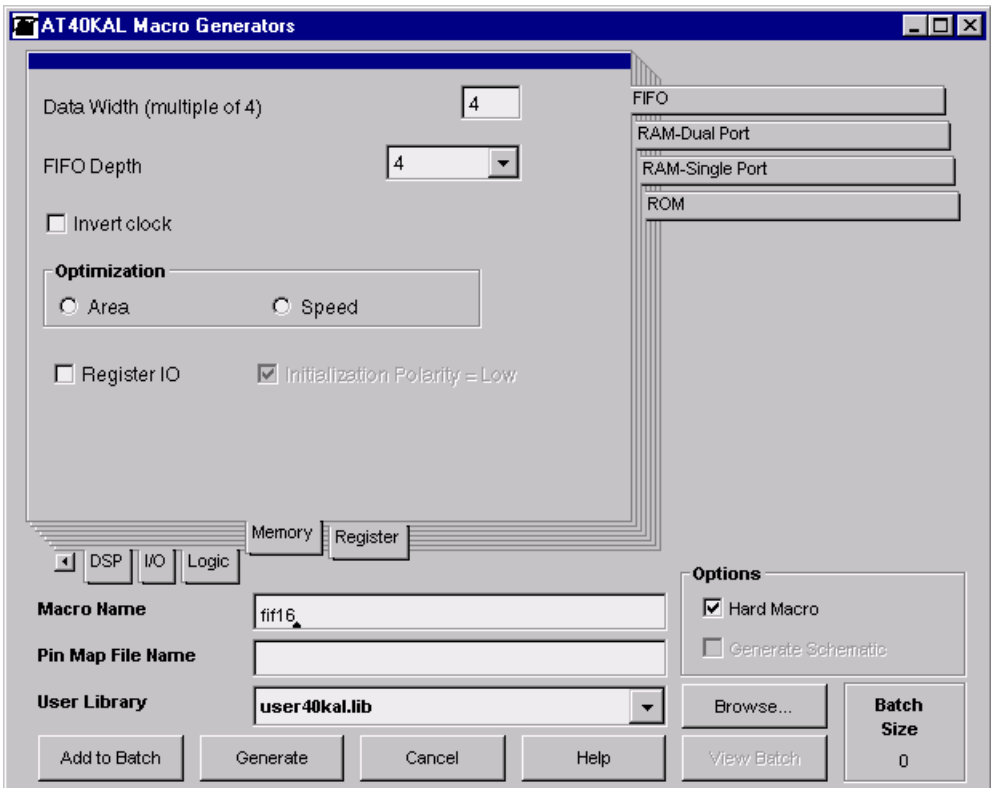
Type	Name	Option	Explanation
In	D [Width - 1:0]	No	Data input bus
Out	Q [Width - 1:0]	No	Data output bus
In	CLK/CLKN	No	Clock (noninverted/inverted)
In	REN	No	Read enable pin (active low)
In	WEN	No	Write enable pin (active low)
In	RESET	Yes	Reset (active low)
Out	FULL	No	FIFO full flag (active low)
Out	EMPTY	No	FIFO empty flag (active low)
Out	SH	Yes	Indicator of bang band register output
Out	MQ	Yes	Bang band register output
Out	SQ	Yes	Shift register output

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	fif16	38.3	26.3	19	7 x 6
AT40K	fif8	38.0	26.1	16	7 x 5
AT40KAL/ AT94KAL	fif16	46.0	21.7	19	7 x 6
AT40KAL/ AT94KAL	fif8	45.8	21.8	16	7 x 5

Figure 1 shows an example of the fif16 macro options.

Figure 1. FIFO Generator



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