IP Core Generator: Deductor

Features

- **Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices**
- **Variable Pitch of Input Pins**
- **Variable Width of Output Vectors**
- **Registers Initialization Selection**
- **Variable Clock Inversion Capability**
- **Initialization Polarity Selection**
- **Preset Value Radix Selection**

Description

The Deductor subtracts a given number from the register initial value. The functional description of the deductor is as follows(1):

```
always @ (posedge CLK or negedge R)
begin
  if(R == 'b0)
    SUM = 0;
  else if (ACC)
    {COUT, SUM} = SUM - DATA - CIN;
end
```

Note: 1. This code assumes that positive-edge clock and active-low reset have been specified.

Programmable SLI
AT40K
AT40KAL
AT94K

Application Note

Rev. 2432B–1/02

Parameters

Parameter	Value	Explanation
Pitch	Integer ≥ 1	Spacing between input pins, a pitch of 2 means will result in 1 cell between input pins.
Width	Integer > 1	Width of input and output vectors
Initialization	Reset	Registers can be reset to zero
	Set	Registers can be set to one
	None	Registers are set automatically on power-up
	Preset Value	Registers can be asynchronously loaded with a constant value
Invert Clock	Boolean	Inverts the clock input
Initialization Polarity = Low	Boolean	Set/Reset/Preset input is active low
Preset Value Radix	Binary	Constants for preset are specified in binary representation
	Octal	Constants for preset are specified in octal representation
	Decimal	Constants for preset are specified in decimal representation
	Hex	Constants for preset are specified in hexadecimal representation

Pins

Type	Name	Option	Explanation
In	CIN	No	Carry-in pin
In	ACCUMULATE	No	Enables the deductor, active high
In	DATA [Width - 1:0]	No	Data input
In	CLK/CLKN	Yes	Clock (noninverted/inverted)
In	R/RN/S/SN/P/PN	Yes	Reset/Set/Preset (active high/low)
Out	SUM[Width - 1:0]	No	Deductor output
Out	COUT	No	Carry-out pin(1)

Note: 1. Carry out = SUM[Width - 1:0] - DATA[Width - 1:0] - CIN < -2^n

Truth Table

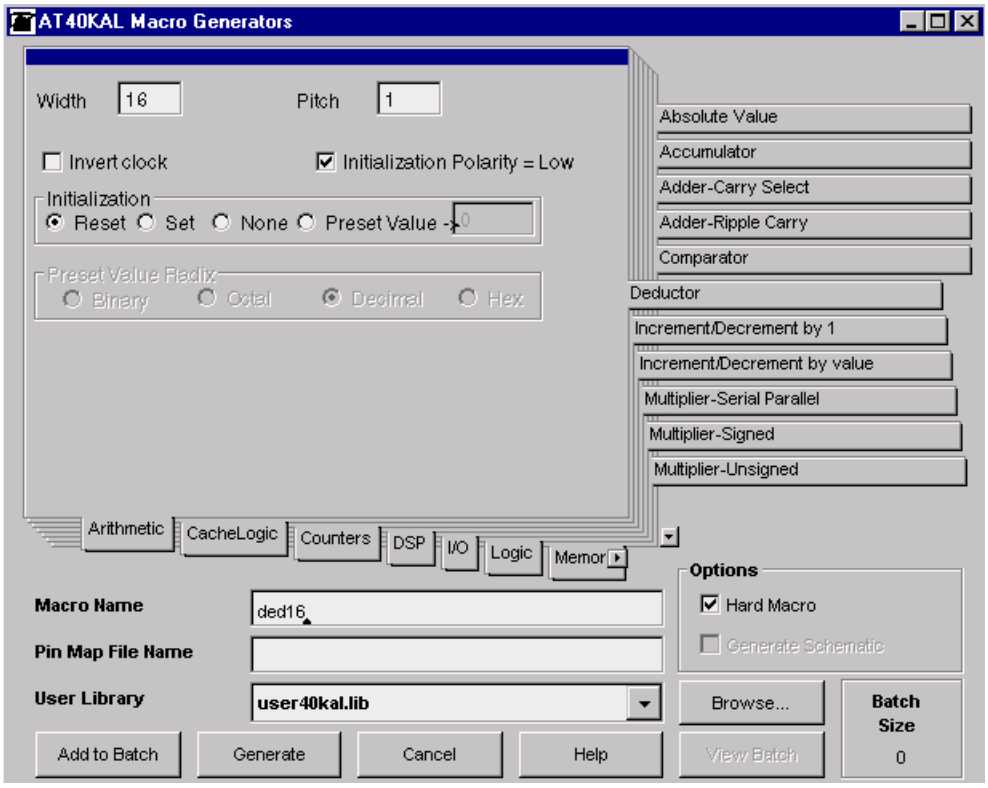
Input		Output	
CIN	DATA [W - 1:0]	SUM[W - 1:0]	COUT
A	B	SUM[W - 1:0] - A - B	1 if SUM[W - 1:0] - A - B < $-(2^W)$, 0 otherwise

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	ded16	29.7	33.6	34	2 x 18
AT40K	ded8	48.9	20.4	18	2 x 10
AT40KAL/ AT94KAL	ded16	38.7	25.9	34	2 x 18
AT40KAL/ AT94KAL	ded8	61.5	16.3	18	2 x 10

Figure 1 shows an example of the ded16 macro options.

Figure 1. Deductor Generator



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