IP Core Generator: Counter

Features

- Counter – Johnson
- Counter – LFSR
- Counter – PreScaled
- Counter – Ripple Carry
- Counter – Terminal
- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Clock Inversion Capability
- Initialization Polarity Selection
- Counter Johnson Only
  - Variable Width of Output Vectors
  - Optional Enable
  - Optional Fold Layout
  - Registers Initialization Selection
- Counter LFSR Only
  - Generator Output Selection
  - Variable Width of Input and Output Data
  - Variable Pitch of Output Pins
  - Optional Fold Layout
  - Count Sequence Report File
  - Count Sequence Formatting File
  - Registers Initialization Selection
- Counter PreScaled Only
  - Counter Direction Selection
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  - Parallel Load Capability
  - Registers Initialization Selection
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  - Optional Enable
  - Optional Fold Layout
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  - Radix of Terminal Selection
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Programmable SLI
AT40K
AT40KAL
AT94K

Application Note

Rev. 2430B–FPSLI–01/02

Counter – Johnson

The Johnson Counter generator can be used to generate counters in which only one output changes on each clock cycle. The following parameters are available:

Parameters

Parameter	Value	Explanation
Width	Integer > 1	Width of output vector
Enable	Boolean	Add an Enable pin to component
Fold	Boolean	Fold layout in half
Invert Clock	Boolean	Invert the clock input
Initialization Polarity = Low	Boolean	Set/Reset/Preset input is active low
Initialization	Reset	Registers can be reset to zero
	Set	Registers can be set to one
	None	Registers are initialized automatically on power-up

Pins

Type	Name	Option	Explanation
In	R/RN/S/SN	No	Reset/Set (active high/low)
In	CLK/CLKN	No	Clock (noninverted/inverted)
In	ENABLE	Yes	Enable counter
Out	Q[Width - 1:0]	No	Counter output

Truth Table(1)

Input			Output
RN	CLK	ENABLE	Q[W - 1:0]
0	X	X	0
1	X	0	Q[W - 1:0]
1	R	1	Q[W - 2:0]Q[W -1]

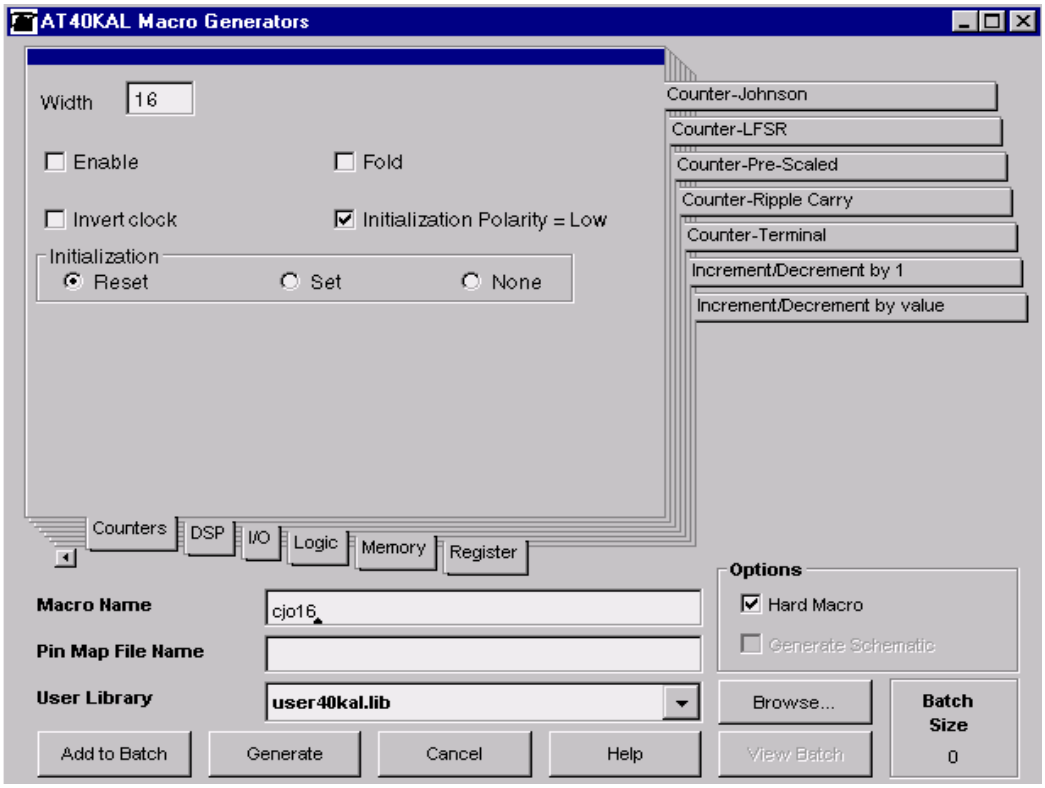
Note: 1. This truth table assumes that a noninverted clock and active low reset have been selected.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	cjo16	95.4	10.5	16	1 x 16
AT40K	cjo8	124.1	8.1	8	1 x 8
AT94K/ AT40KAL	cjo16	98.0	10.2	16	1 x 16
AT94K/ AT40KAL	cjo8	120.2	8.3	8	1 x 8

Figure 1 shows an example of the cjo16 macro options.

Figure 1. Counter – Johnson Generator



Counter – LFSR

The LFSR generator can be used to create a high-speed divide by [2**(n - 1) -1] counter, where *n* is the number of bits. The count sequence can be output in a format specified by a user-supplied data file (described below).

Parameters

Parameter	Value	Explanation
Generator Output	Component	Generate component only – do not output count sequence
	Count File	Output count sequence only – do not generate component
	Both	Output count sequence and generate component
Width	Integer ≥ 3	Width of input and output data
Pitch	Integer ≥ 1	Pitch of output pins. A pitch of 2 results in a one cell gap between outputs
Fold Layout	Boolean	Fold layout in half
Count Sequence Report File	Filename	Name of count sequence output file. This file is written out to the current project directory when “Count file” or “Both” are selected as the generator output option.
Count Sequence Formatting File	Filename	Name of the file (found in the current project directory) that is to be used to format the count sequence output.
Invert Clock	Boolean	Invert the clock input
Initialization Polarity = Low	Boolean	Set/Reset/Preset input is active low
Initialization	Reset	Registers can be reset to zero
	Set	Registers can be set to one
	None	Registers are initialized automatically on power-up
	Preset	Registers can be asynchronously loaded with a constant value
Preset Value Radix	Binary	Preset value is specified in binary representation
	Octal	Preset value is specified in octal representation
	Decimal	Preset value is specified in decimal representation
	Hex	Preset value is specified in hexadecimal representation

Pins

Type	Name	Option	Explanation
In	R/RN/S/SN/P/PN	No	Reset/Set/Preset (active high/low)
In	CLK/CLKN	No	Clock (noninverted/inverted)
Out	Q[Width - 1:0]	No	Counter output

Truth Table[1]

Input		Output
RN	CLK	Q[W - 1:0]
0	X	0
1	X	Present State
1	R	LFSR Next State

Note: 1. This truth table assumes a noninverted clock and active low reset have been selected.

Count Sequence Output – When the Generator Output option is set to Count or Both, an output file called the Count sequence report file is generated on completion of the program run. This file lists the count sequence for the generated LFSR.

The user can also create an input file, called the Count sequence formatting file, to specify which parts of the count sequence should be listed. The Count sequence formatting file should be placed in the design directory. The format of the file is basically a header line with “hex”, “dec” or “bin” to indicate that the numbers in the file are in hexadecimal, decimal or binary format. Each subsequent line should be in the form of Start_Count End_Count. For example:

lfsr.dat

dec

0 2

4 20

88 127

300 844

1088 1090

The output will have the format Count *count_number* Decode *decode_value*, where *decode_value* is the counter Q[W-1:0] output for *count_number*.

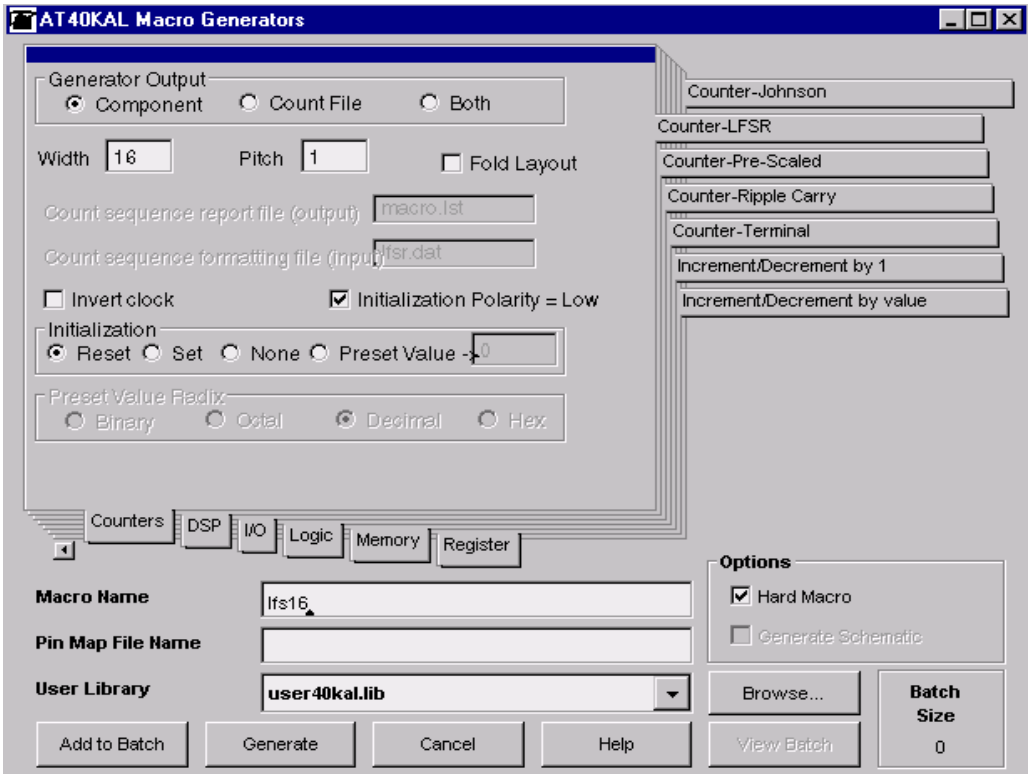
Decoding Terminal Count – The count sequence always ends with the same sequence: all bits are 1’s after which 0’s shift in on each clock from the LSB until all bits are 0’s. For example, a 3 bit counter would end with the sequence 7, 6, 4, 0. A simple comparator circuit can therefore be used to quickly decode the Terminal Count.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	lfs16	93.5	10.7	16	1 x 16
AT40K	lfs8	115.7	8.6	8	1 x 8
AT94K/ AT40KAL	lfs16	94.7	10.6	16	1 x 16
AT94K/ AT40KAL	lfs8	110.6	9.0	8	1 x 8

Figure 2 shows an example of the lfs16 macro options.

Figure 2. Counter – LFSR Generator



Counter – PreScaled

The PreScaled Counter generator can be used to implement a faster Ripple Carry binary counter.

Parameters

Parameter	Value	Explanation
Direction	Up	Create an up counter
	Down	Create a down counter
	Up/Down	Create a programmable up/down counter
Width	Integer > 2	Width of input and output vectors
Pitch	Integer ≥ 1	Spacing between output pins. A pitch of 2 means one cell between pins
Parallel Load	Boolean	Provide a parallel load capability
Enable	Boolean	Provide an enable input
Invert Clock	Boolean	Invert the clock input
Initialization Polarity = Low	Boolean	Set/Reset/Preset input is active low
Initialization	Reset	Registers can be reset to zero
	Set	Registers can be set to one
	None	Registers are reset automatically on power-up
	Preset	Registers can be asynchronously loaded with a constant value
Preset Value Radix	Binary	Preset value is specified in binary representation
	Octal	Preset value is specified in decimal representation
	Decimal	Preset value is specified in octal representation
	Hex	Preset value is specified in hexadecimal representation

Pins

Type	Name	Option	Explanation
In	SLOAD	Yes	Performs a parallel load when low
In	ENABLE	Yes	Enables the counter, active high
In	CARRYIN	No	Carry in to counter
In	UP_DOWN	No	Up = 1, down = 0
In	DATA[Width - 1:0]	Yes	Parallel load data input
In	CLK/CLKN	Yes	Clock (noninverted/inverted)
In	R/RN/S/SN/P/PN	Yes	Reset/Set/Preset (active high/low)
Out	Q[Width - 1:0]	No	Counter output
Out	RCO	No	Carry out(1)

Note: 1. If Up, then Carry out = 1 when counter overflows. Carry out = 1 when counter underflows.

Truth Table[1]

Input					Output	
SLOAD	ENABLE	UP_DOWN	CARRYIN	DATA [W - 1:0]	Q[W - 1:0]	RCO
0	X	1	X	A	A	1 if A > (2^W) - 1, 0 otherwise
0	X	0	X	A	A	1 if A < -(2^W), 0 otherwise
1	0	X	X	X	Present State	Present State
1	X	X	0	X	Q[W - 1:0]	RCO
1	1	1	1	X	Q[W - 1:0] + 1	1 if Q[W - 1:0] + 1 > (2^W) - 1, 0 otherwise
1	1	0	1	X	Q[W - 1:0] - 1	1 if Q[W - 1:0] - 1 < -(2^W), 0 otherwise

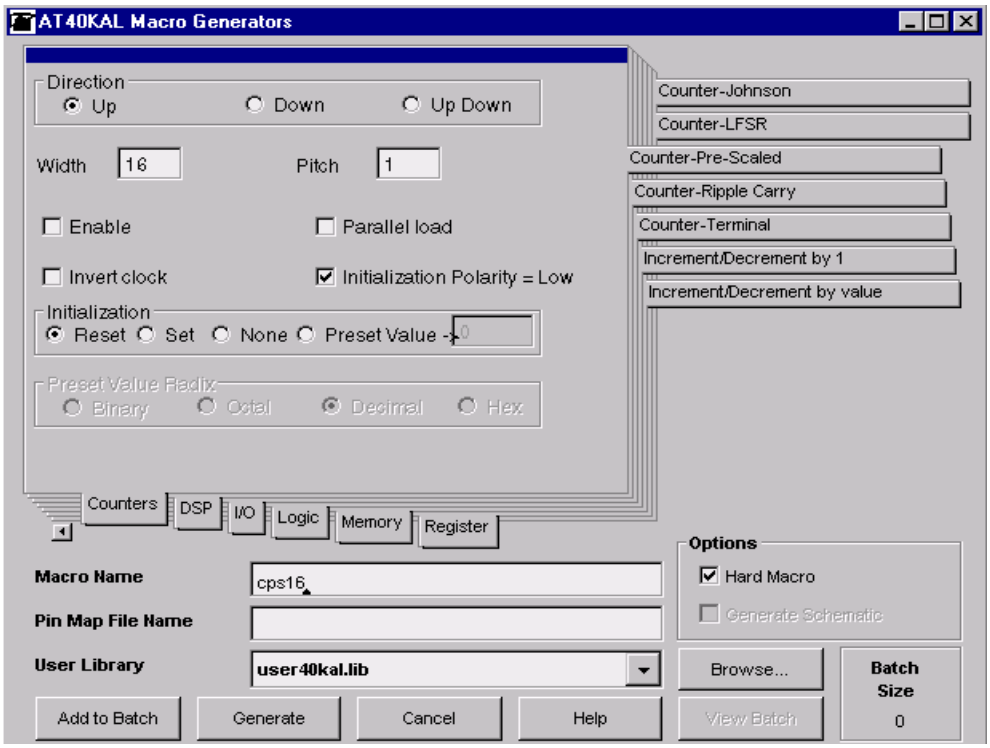
Note: 1. The ENABLE signal must be negated during load, and must remain negated for at least 1 clock cycle after SLOAD negates.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	cps16	36.1	27.7	17	1 x 17
AT40K	cps8	68.8	14.5	9	1 x 9
AT94K/ AT40KAL	cps16	45.2	22.1	17	1 x 17
AT94K/ AT40KAL	cps8	82.1	12.2	9	1 x 9

Figure 3 shows an example of the cps16 macro options.

Figure 3. Counter – PreScaled Generator



Counter – Ripple Carry

The Counter generator can be used to generate Ripple Carry Counters. The following parameters are available for the counters.

Parameters

Parameter	Value	Explanation
Direction	Up	Create an Up counter
	Down	Create a Down counter
	Up/Down	Create an Up/Down counter
Width	Integer > 1	Width of input and output vectors
Enable	Boolean	Add an enable pin to component
Fold	Boolean	Fold layout in half
Parallel load	Disabled	No parallel load capability
	Var. Value	Parallel load capability
	Const. Value	Fixed value can be synchronously loaded
Initialization	Reset	Registers can be reset to zero
	Set	Registers can be set to one
	None	Registers are initialized automatically on power-up
	Preset	Registers can be asynchronously loaded with a constant value
Invert Clock	Boolean	Invert the clock input
Initialization Polarity = Low	Boolean	Set/Reset/Preset input is active low
Preset & Load Value Radix	Binary	Constants for parallel load and preset are specified in binary representation
	Octal	Constants are specified in octal
	Decimal	Constants are specified in decimal
	Hex	Constants are specified in hexadecimal

Pins

Type	Name	Option	Explanation
In	R/RN/S/SN/P/PN	No	Reset/Set/Preset (active high/low)
In	CLK/CLKN	No	Clock (Noninverted/Inverted)
In	ENABLE	Yes	Enable counter
In	DATA[Width - 1:0]	Yes	Parallel load input
In	LOAD	Yes	Load signal (active low)
In	UP_DOWN	Yes	Up/Down control up = 1
Out	Q[Width - 1:0]	No	Counter output
Out	RCO	No	Ripple carry out

Truth Table[1]

Input						Output	
RN	ENABLE	CLK	LOAD	DATA[W - 1:0]	UP/DOWN	Q[W - 1:0]	RCO
0	X	X	X	X...X	X	0...0	0
1	0	X	1	X...X	X	QW...Q0	0
1	1	R	0	DW...D0	X	DW...D0	0
1	1	X	1	X...X	X	Present State	QW*...*Q1*Q0
1	1	R	1	DW...D0	1	DW...D0 + 1	QW*...*Q1*Q0
1	1	R	1	DW...D0	0	DW...D0 - 1	QW*...*Q1*Q0

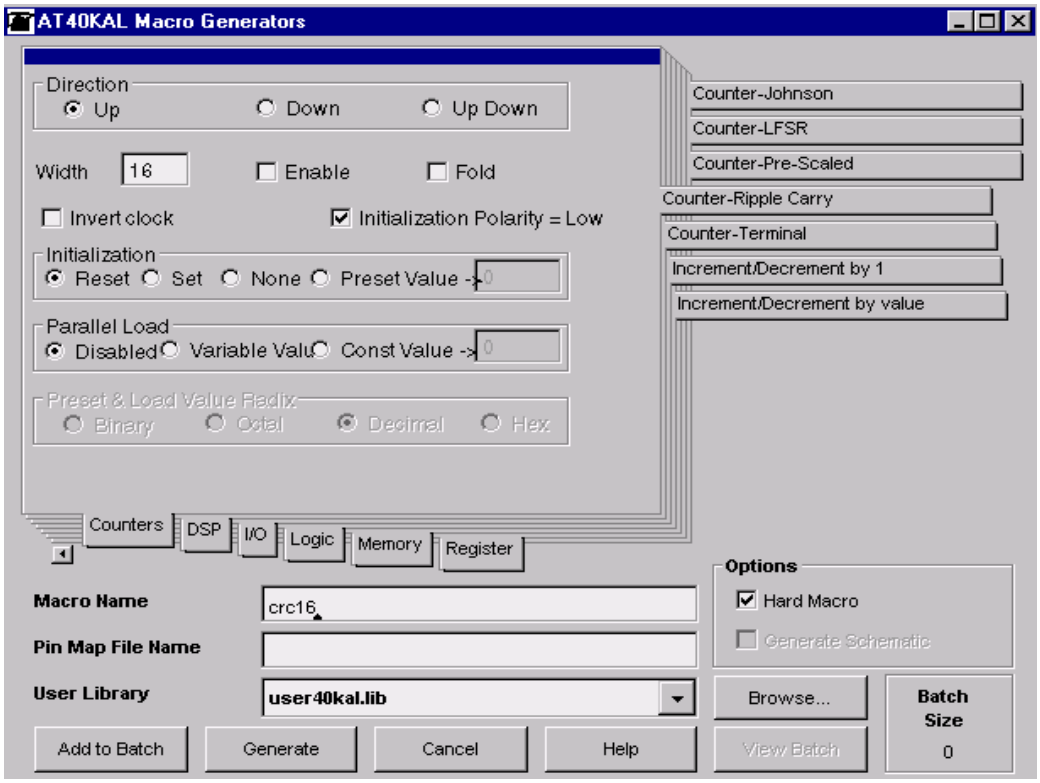
Note: 1. This truth table assumes that an active-low reset and non-inverted clock have been selected. For an up counter, the RCO pin goes high whenever the current state equals the maximum count. For a down counter, it goes high when the minimum count state is reached (i.e. all zeros). Counters can be chained together by connecting the RCO pin of one counter to the enable input of the next.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	crc16	36.8	27.2	16	1 x 16
AT40K	crc8	71.5	14.0	8	1 x 8
AT40KAL/ AT94KAL	crc16	45.7	21.9	16	1 x 16
AT40KAL/ AT94KAL	crc8	83.6	12.0	8	1 x 8

Figure 4 shows an example of the crc16 macro options.

Figure 4. Counter – Ripple Carry Generator



Counter – Terminal

The Terminal Counter generator allows the user to create a counter that stops after *n* clock cycles. The following options are available:

Parameters

Parameter	Value	Explanation
Terminal Count	Integer ≥ 1	The number of states the counter should step through before stopping and asserting the TERMCNT pin.
Radix of Terminal Count	Binary	Terminal count value is specified in binary representation
	Octal	Value is specified in octal
	Decimal	Constants are specified in decimal
	Hex	Constants are specified in hexadecimal
Pitch	Integer >= 1	Pitch between output pins. A pitch of 2 results in a one cell gap between pins.
Invert Clock	Boolean	Invert the clock input
Initialization Polarity = Low	Boolean	Preset input is active low

Pins

Type	Name	Option	Explanation
In	CLK/CLKN	No	Clock (noninverted/inverted)
In	P/PN	No	Preset input (active high/low)
Out	TERMCNT	No	Terminal count(1)

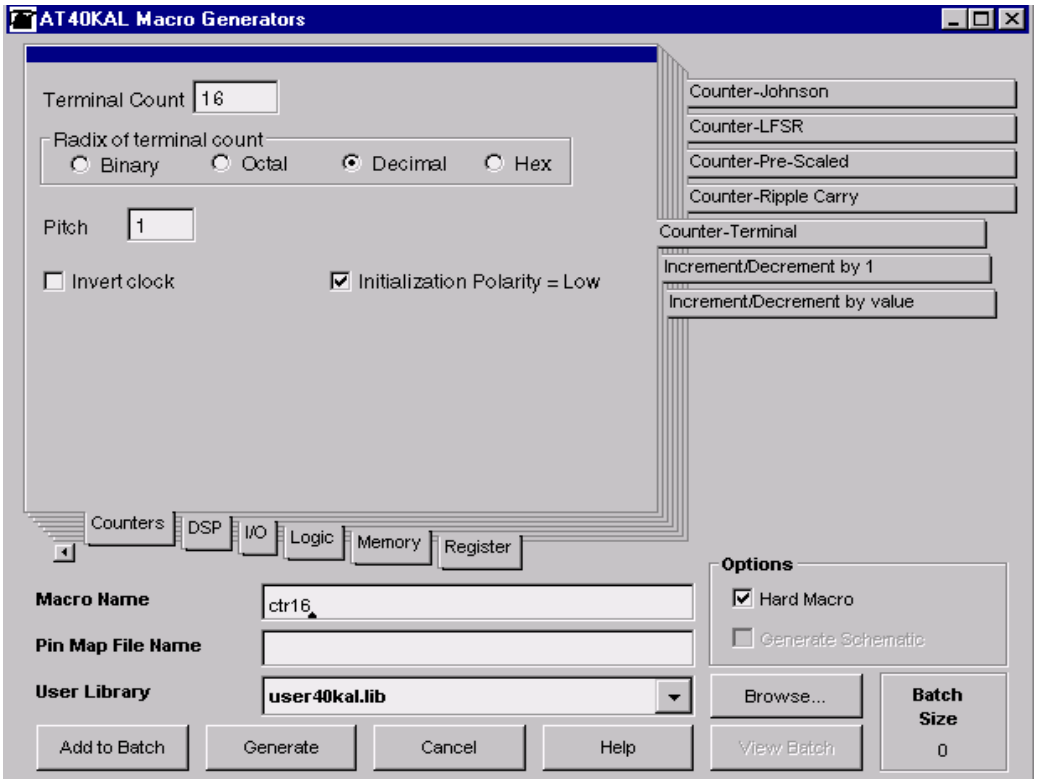
Note: 1. Terminal Count = 1 when *n* clock cycles have been applied. The count can be reset by asserting the preset pin. This loads the counter with the appropriate value to produce a count sequence of length *n*.

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	ctr16	85.0	11.8	6	1 x 6
AT40K	ctr8	98.9	10.1	5	1 x 5
AT94K/ AT40KAL	ctr16	85.0	11.8	6	1 x 6
AT94K/ AT40KAL	ctr8	95.0	10.5	5	1 x 5

Figure 5 shows an example of the ctr16 macro options.

Figure 5. Counter – Terminal Generator



Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
Atmel Corporate
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 436-4270
FAX 1(408) 436-4314

Microcontrollers
Atmel Corporate
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 436-4270
FAX 1(408) 436-4314

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

Atmel Colorado Springs
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Atmel Smart Card ICs
Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Atmel Heilbronn
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

Atmel Colorado Springs
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

Atmel Programmable SLI Hotline
(408) 436-4119

Atmel Programmable SLI e-mail
fpga@atmel.com – fpslic@atmel.com

FAQ
Available on web site

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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