

# IP Core Generator: Comparator

## Features

- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Optional Signed or Unsigned Inputs
- Variable Width of Inputs A and B
- Variable Outputs

## Comparator

The function of the Comparator generator can be explained as follows:

Equals	=	(DATAA == DATAB)
NotEquals	=	(DATAA != DATAB)
LessThan	=	(DATAA < DATAB)
LessThanOrEqualTo	=	(DATAA ≤ DATAB)
GreaterThan	=	(DATAA > DATAB)
GreaterThanOrEqualTo	=	(DATAA ≥ DATAB)

## Parameters

Parameter	Value	Explanation
Representation	Unsigned	Treat inputs as unsigned
	Signed	Treat inputs as signed
Width	Integer > 1	Width of inputs A and B
A = B <sup>(1)</sup>	Boolean	Add Equal pin (AEB) to comparator
A != B	Boolean	Add NotEqual pin (ANEB) to comparator
A < B	Boolean	Add LessThan pin (ALB) to comparator
A ≤ B	Boolean	Add LessThanOrEqualTo pin (ALEB) to comparator
A > B	Boolean	Add GreaterThan pin (AGB) to comparator
A ≥ B	Boolean	Add GreaterThanOrEqualTo pin (AGEB) to comparator

Note: 1. If A = B is the only output selected, an optimized Equality-Only comparator will be produced, resulting in a much smaller layout.



Programmable  
SLI  
AT40K  
AT40KAL  
AT94K

Application  
Note



## Pins

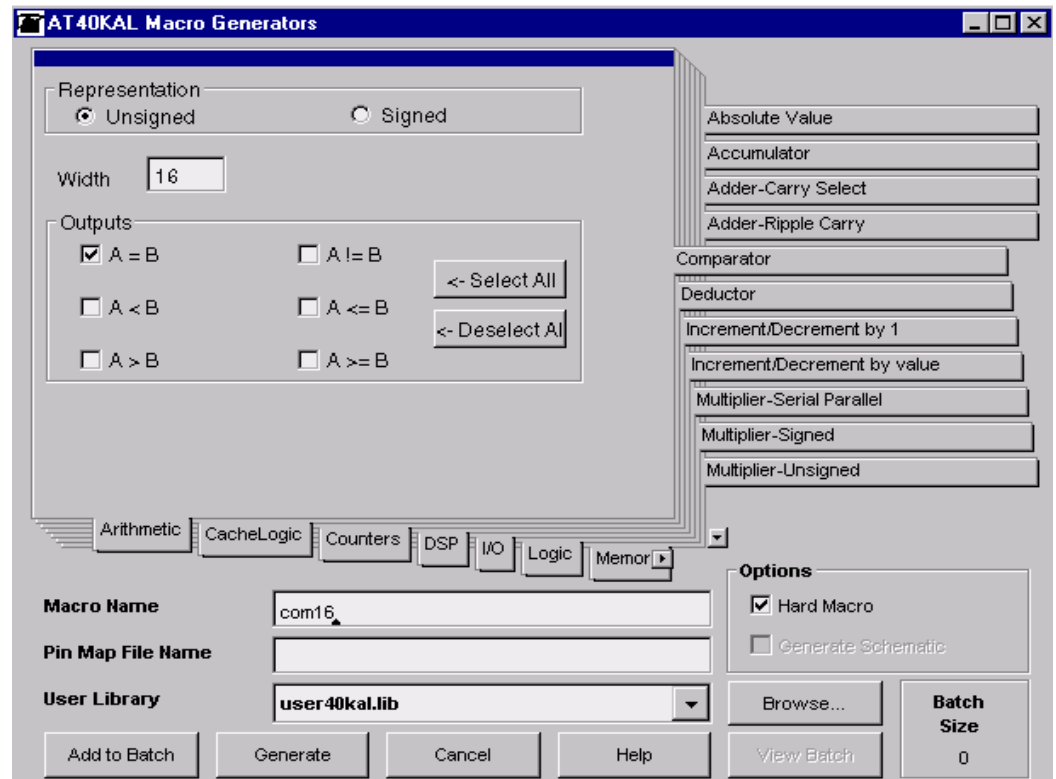
Type	Name	Option	Explanation
In	DATAA[Width - 1:0]	No	Input data A
In	DATAB[Width - 1:0]	No	Input data B
Out	AEB	Yes	1 if A = B, 0 otherwise
Out	ANEB	Yes	1 if A != B, 0 otherwise
Out	ALB	Yes	1 if A < B, 0 otherwise
Out	ALEB	Yes	1 if A ≤ B, 0 otherwise
Out	AGB	Yes	1 if A > B, 0 otherwise
Out	AGEB	Yes	1 if A ≥ B, 0 otherwise

## Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	com16	45.4	22	16	8 x 2
AT40K	com8	97.4	10.3	8	4 x 2
AT40KAL/ AT94KAL	com16	56.1	17.8	16	8 x 2
AT40KAL/ AT94KAL	com8	128.0	7.8	8	4 x 2

Figure 1 shows an example of the com16 macro options.

Figure 1. Comparator Generator





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