IP Core Generator: Adders

Features

- **Adder – Carry Select**
- **Adder – Ripple Carry**
- **Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices**
- **Variable Width for Input and Output Vectors**
- **Optional Carry In**
- **Optional Carry Out**
- **Ripple Carry Adder Only**
  - **Optional Registered Inputs and Outputs**
  - **Optional Signed Overflow Pin**
  - **Variable Pitch**
  - **Variable Width**
  - **Variable Aspect Ratio**

Adder – Carry Select

This generator can be used to generate an *n* bit Carry Select Adder.

Parameters

Parameter	Value	Explanation
Width	Integer > 1	Width of input and output vectors
Carry In	Boolean	Provide a carry-in pin
Carry Out	Boolean	Provide a carry-out pin

Pins

Type	Name	Option	Explanation
In	CIN	Yes	Carry in
In	DATAA[Width - 1:0]	No	A input
In	DATAB[Width - 1:0]	No	B input
Out	SUM[Width - 1:0]	No	Adder output
Out	COUT	Yes	Carry out

Programmable SLI
AT40K
AT40KAL
AT94K

Application Note

Rev. 2425B–FPSLI–01/02

Truth Table

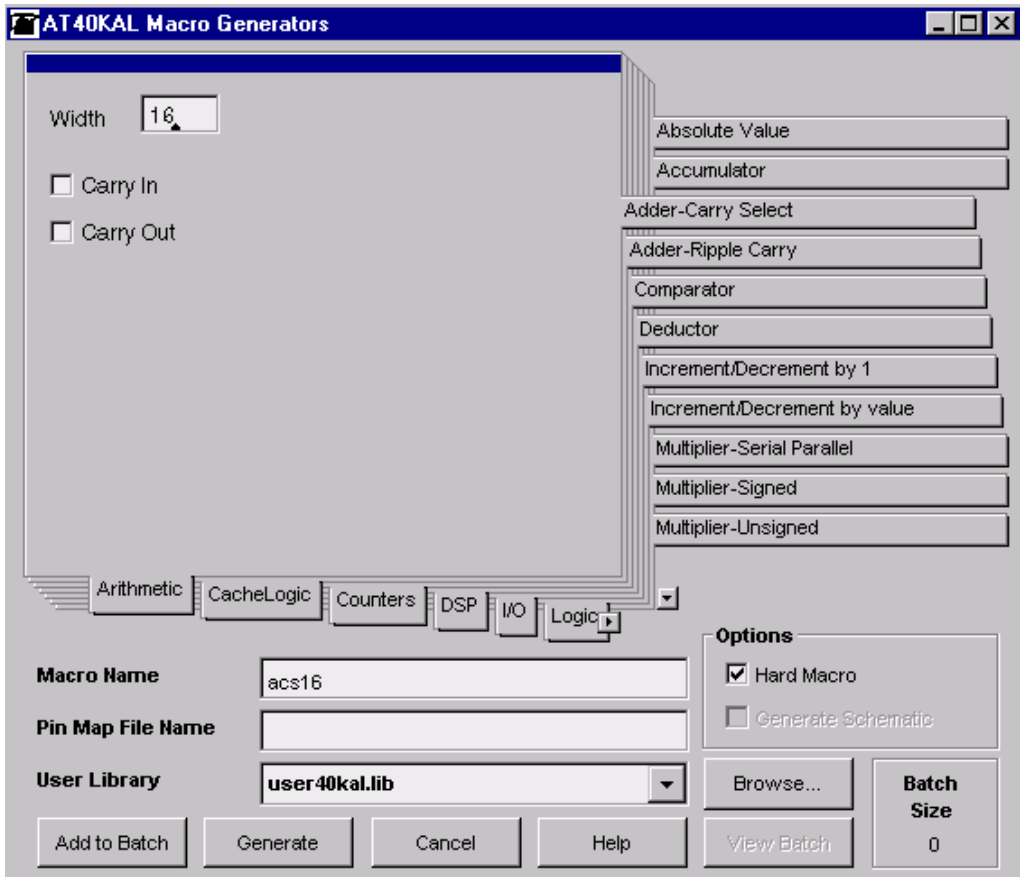
Input			Output	
CIN	DATAA[W - 1:0]	DATAB[W - 1:0]	SUM[W - 1:0]	COUT
C	A	B	A + B + C	1 if A + B + C > 2^W, 0 otherwise

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	acs16	40.0	25.0	48	3 x 19
AT94K/ AT40KAL	acs16	47.0	21.3	48	3 x 19

Figure 1 shows an example of the acs16 macro options.

Figure 1. Adder – Carry Select Generator



Adder – Ripple Carry

The Adder generator can be used to generate a ripple carry adder.

Parameters

Parameter	Value	Explanation
Carry In	NoRegister	Include the carry in pin on the generator but do not register it
	Register	Register carry in of the adder
	Disabled	Do not include the carry-in pin on the adder
Carry Out	NoRegister	Include the carry-out pin on the adder but do not register it
	Register	Register carry out of the adder
	Disabled	Do not include the carry-out pin on the adder
Register	None	Do not register the inputs and outputs
	Input	Register inputs on the adder, exclude carry-in pin
	Output	Register outputs on the adder, exclude carry-out pin
	Both	Register both inputs and outputs including the carry-in and carry-out pins of the adder
Signed Over-flow Pin	Boolean	Provide a signed overflow output (treating input vectors as signed values)
Pitch	Integer > 1	Spacing between input pins, pitch of 2 means one cell between input pins
Width	Integer > 1	Width of input and output vectors
Aspect Ratio	Float ≥ 0.0	Aspect ratio of the adder layout. A ratio of 0.0 gives a thin, vertical layout, whereas a ratio of 1.0 gives a square layout

If input, output, carry-in or carry-out registers are selected, three additional parameters are available.

Register Parameters

Parameter	Value	Explanation
Invert Clock	Boolean	Invert the register clock
Initialization Polarity = Low	Boolean	Make register initialization active low
Register Set/Reset Function	Reset	Registers can be reset to zero
	Set	Registers can be set to one

Pins

Type	Name	Option	Explanation
In	CIN	Yes	Carry in
In	DATAA[Width - 1:0]	No	A input
In	DATAB[Width - 1:0]	No	B input
In	CLK/CLKN	Yes	Clock (noninverted/inverted)
In	R/RN/S/SN	Yes	Reset/Set (active high/low)
Out	SUM[Width - 1:0]	No	Adder output
Out	COUT	Yes	Carry out (cannot be used with overflow in an unsigned adder)
Out	OVERFLOW	Yes	Overflow

Carry out = DATAA + DATAB + CIN > 2^n - 1 or

DATAA + DATAB + CIN < -2^n

Signed overflow = DATAA + DATAB + CIN > 2^n - 1 or

DATAA + DATAB + CIN < -2^n

Truth Table

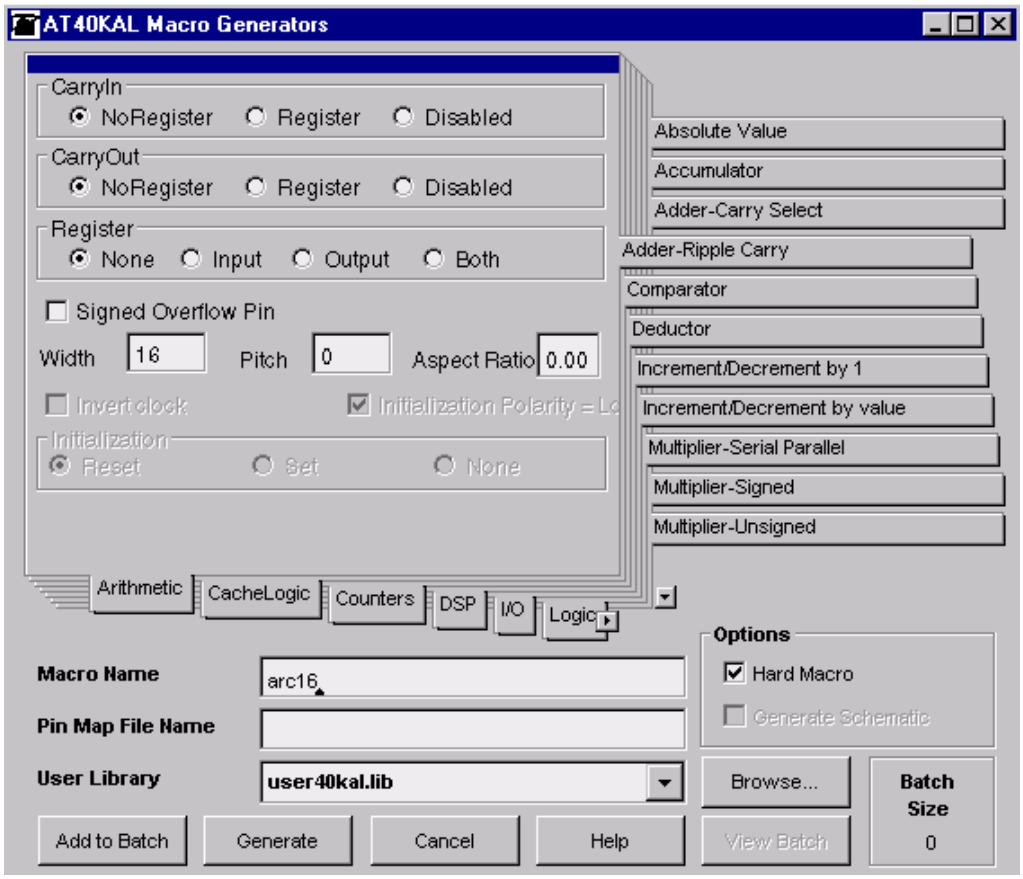
Input			Output	
CIN	DATAA[W - 1:0]	DATAB[W - 1:0]	SUM[W - 1:0]	COUT
C	A	B	A + B + C	1 if A + B + C > 2^W, 0 otherwise

Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	arc16	36.2	27.7	16	1 x 16
AT40K	arc8	69.2	14.5	8	1 x 8
AT94K/ AT40KAL	arc16	49.9	20.1	16	1 x 16
AT94K/ AT40KAL	arc8	95.6	10.5	8	1 x 8

Figure 2 shows an example of the arc16 macro options.

Figure 2. Adder – Ripple Carry Generator



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