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## IP Core Generator: Accumulator

### Features

- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Variable Pitch Option
- Variable Width for Input and Output Devices
- Optional Set or Reset
- Optional Preset
- Clock Inversion Capability
- Initialization Polarity Selection

### Description

The Accumulator adds a given number to the register initial value. The functional description of the accumulator is as follows<sup>(1)</sup>:

```
always(@posedge CLK or negedge RST)
begin
    if(RST == 'b0)
        SUM = 0;
    else if (ACC)
        {COUT, SUM} = SUM + DATA + CIN;
end
```

Note: 1. The above assumes that positive-edge clock and active-low reset have been specified.



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**Programmable  
SLI  
AT40K  
AT40KAL  
AT94K**

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**Application  
Note**

Rev. 2424B-FPSLI-01/02



## Parameters

Parameter	Value	Explanation
Pitch	Integer $\geq 1$	Spacing between input pins. A pitch of 2 means will result in 1 cell between input pins
Width	Integer $> 1$	Width of input and output vectors
Initialization	Reset	Registers can be reset to zero
	Set	Registers can be set to one
	None	Registers are reset automatically on power-up
Preset	Value	Registers can be asynchronously loaded with a constant value
Invert Clock	Boolean	Invert the clock input
Initialization Polarity = Low	Boolean	Set/Reset/Preset input is active low
Preset Value Radix	Binary	Constants for preset are specified in binary representation
	Octal	Constants are specified in octal
	Decimal	Constants are specified in decimal
	Hex	Constants are specified in hexadecimal

## Pins

Type	Name	Option	Explanation
In	CIN	No	Carry in
In	ACCUMULATE	No	Enables the accumulator, active high
In	DATA[Width - 1:0]	No	Data input
In	CL/CLKN	Yes	Clock (noninverted/inverted)
In	R/RN/S/SN	Yes	Reset/Set (active high/low)
Out	SUM[Width - 1:0]	No	Accumulator output
Out	COUT	No	Carry out <sup>(1)</sup>

Note: 1. Carry Out = SUM[Width - 1:0] + DATA[Width - 1:0] + CIN  $> 2^n - 1$

## Truth Table

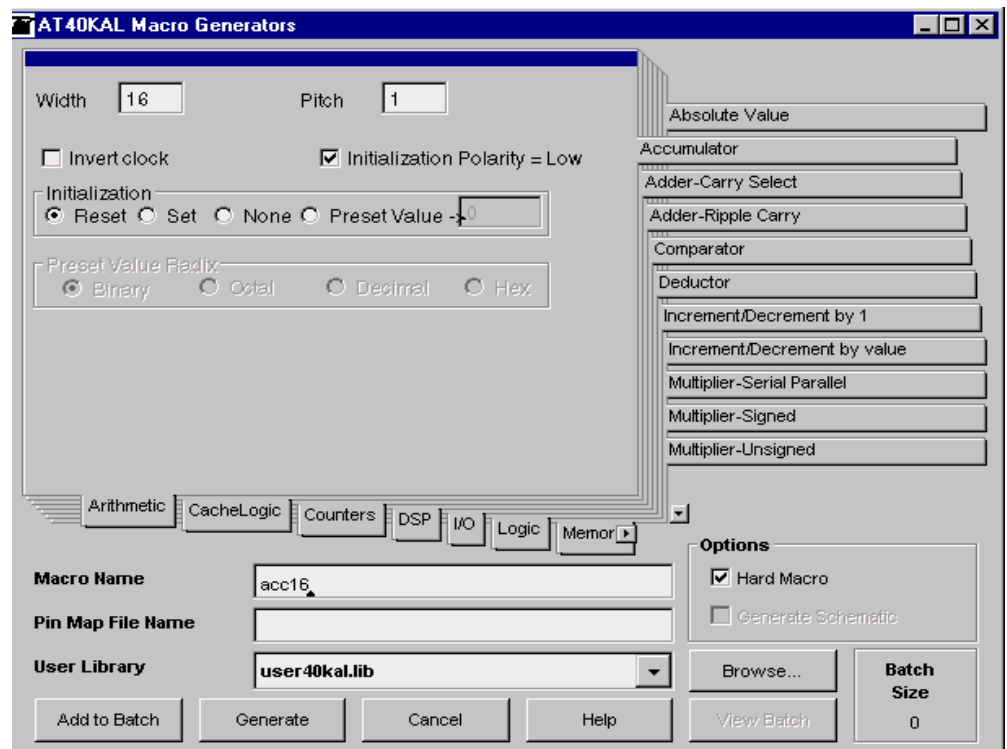
Input		Output	
CIN	DATA [W - 1:0]	SUM[W - 1:0]	COUT
A	B	A + B + SUM[W - 1:0]	1 if A + B + SUM[W - 1:0] $> (2^W) - 1$ , 0 otherwise

## Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	acc16	29.7	33.7	36	2 x 18
AT40K	acc8	48.8	20.5	20	2 x 10
AT94K/ AT40KAL	acc16	38.7	25.8	36	2 x 18
AT94K/ AT40KAL	acc8	61.6	16.2	20	2 x 10

Figure 1 shows an example of the acc16 macro options.

**Figure 1.** Accumulator Generator





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