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## IP Core Generator: Absolute Value

### Features

- Accessible from the Macro Generator Dialog and HDLPlanner™ – Included in IDS for FPGA Devices and System Designer™ for AT94K FPSLIC™ Devices
- Optional Overflow Pin
- Variable Width for Input and Output Vectors

### Description

The function of the Absolute Value generator can be explained as follows:

if  $DATA = -2^{(Width - 1)}$ , then

    OVERFLOW = 1, RESULT = 0

else if  $DATA < 0$ , then

    RESULT = - DATA

else

    RESULT = DATA

DATA must always represent a two's complement and the RESULT is always a positive number.

### Parameters

Parameter	Value	Explanation
Overflow	Boolean	Create with overflow pin
Width	Integer > 1	Width of input and output vectors

### Pins

Type	Name	Option	Explanation
In	DATA[Width - 1:0]	No	Input data
Out	RESULT[Width - 1:0]	No	Absolute value of data (number of outputs will be width - 1 if overflow is used)
Out	OVERFLOW	Yes	True if $Data = -2^{(Width - 1)}$



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Programmable

SLI

AT40K

AT40KAL

AT94K

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Application  
Note

Rev. 2423B-FPSLI-01/02

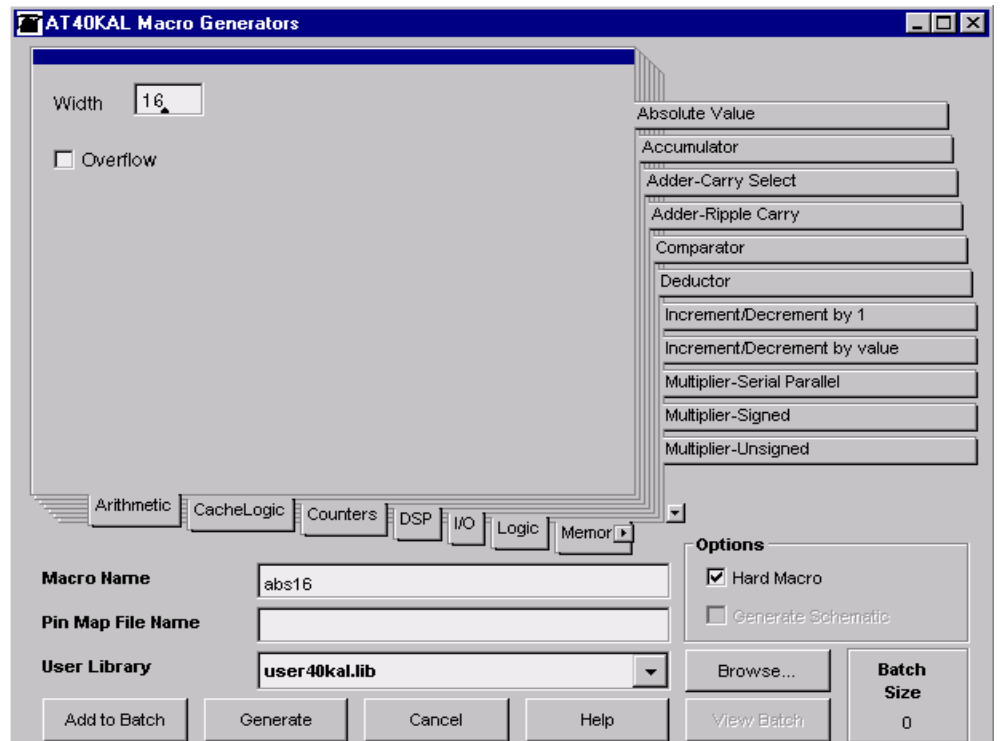


## Statistics

Device	Name	Speed (MHz)	Delay (ns)	Cells	Size (x * y)
AT40K	abs16	38.88	25.8	15	1 x 15
AT40K	abs8	79.4	12.6	7	1 x 7
AT94K/ AT40KAL	abs16	54.8	18.2	15	1 x 15
AT94K/ AT40KAL	abs8	115.7	8.6	7	1 x 7

Figure 1 shows an example of the abs16 macro options.

**Figure 1.** Absolute Value Generator





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