AVR-FPGA Interface Design 3

Features

- **Initialization and Use of AVR-FPGA Interface and Interrupts**
- **Initialization and Use of the Shared Dual-port SRAM**
- **Full Source Code for AVR® Microcontroller and FPGA Included**

Description

Atmel's AT94K sample designs are provided to familiarize the user with the AT94K FPSLIC™ device. This design is an enhancement of Design 2 (doc2326.pdf). The only difference between the two designs is that this design implements a second counter, which is loaded from the shared dual-port SRAM.

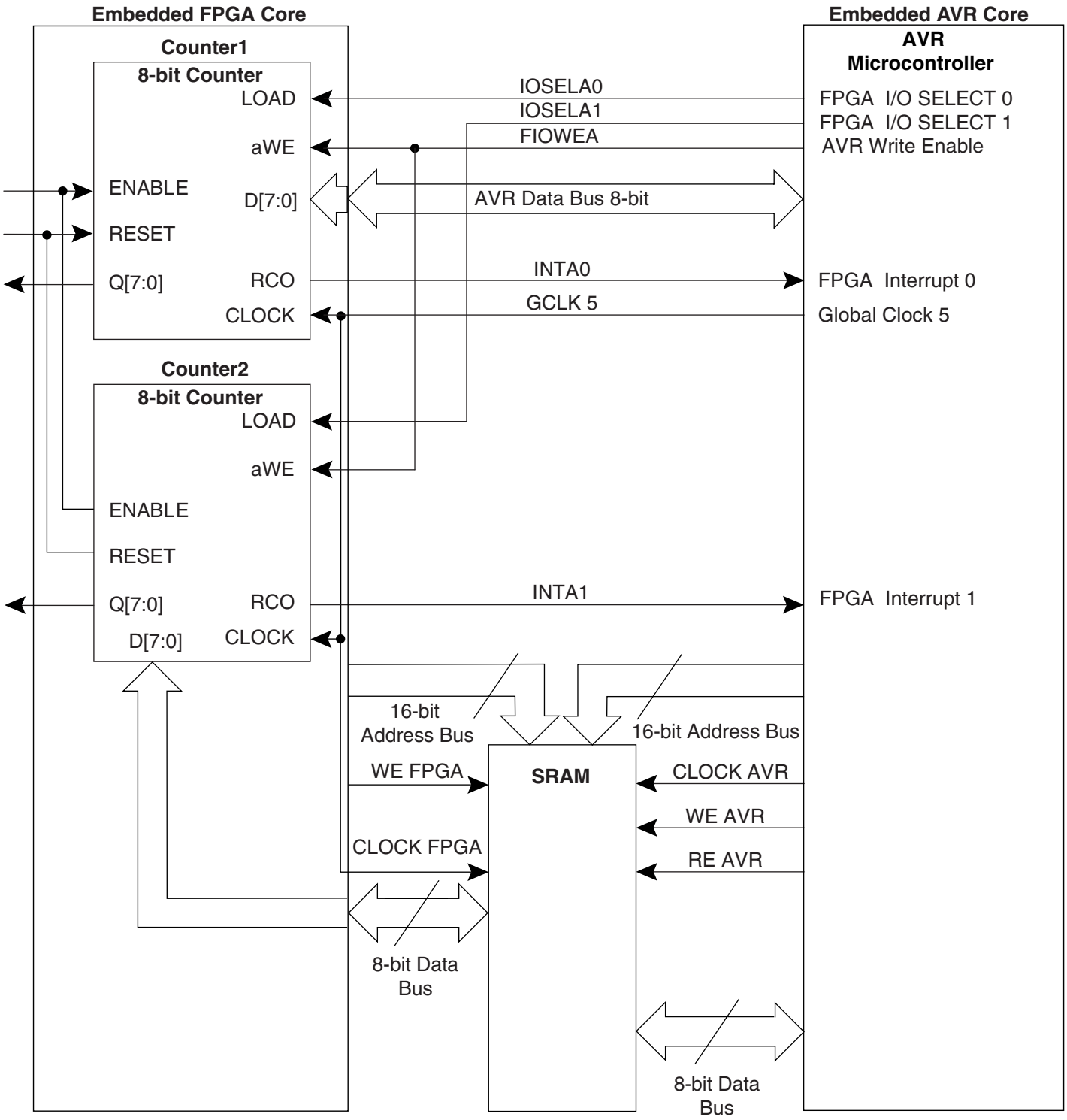
This design is composed of a simple AVR program and two loadable ripple-carry counters implemented in the FPGA. The counters begin counting at zero upon power-up and will generate an interrupt to the AVR using the ripple-carry out signal. The active low interrupt must be held for three clock cycles prior to being acknowledged by the AVR.

Programmable SLI
AT94K

Application Note

Rev. 2327B–FPSLI–03/03

Functional Block Diagram



The block diagram shows the connections used in this example, all interface connections are implemented using dedicated resources. This example makes use of the AVR-FPGA Data Bus, two FPGA Interrupts, two I/O Select signals and two SRAM locations.

Implementation

The AVR source of this design has been implemented in C for the CodeVision AVR, IAR Systems and ImageCraft compilers, and in assembly for the Atmel Assembler. The FPGA design has been implemented in Verilog and VHDL. Each file is commented.

Assuming a default System Designer™ installation, the source files for this application note can be found within the `\SystemDesigner\Examples\AT94K\Cover-ify\doc2327.zip` archive. Alternatively, the source files may be downloaded from the FPSLIC Application Notes section of the Atmel web site (http://www.atmel.com). The source files for the Design 3 are shown in Table 1.

Table 1. Source Files for Design 3

File	Description
AT94KDEF.INC	Atmel AVR Assembler FPSLIC Include File
D3-ATML.ASM	Atmel AVR Assembler Design 3 Source File
D3-CVAVR.C	CodeVision AVR Design 3 Source File
D3-IAR.C	IAR Systems Design 3 Source File
D3-ICC.C	ImageCraft Design 3 Source File
v150-at94k-32.xcl	IAR Systems v1.50 Design XLINK File
v200-at94k-32.xcl	IAR Systems v2.00 Design XLINK File
COUNTER.V	Counter One Implementation Verilog Source File
COUNTER2.V	Counter Two Implementation Verilog Source File
COUNTER3.V	Top-level Verilog Source File
COUNTER.VHD	Counter One Implementation VHDL Source File
COUNTER2.VHD	Counter Two Implementation VHDL Source File
COUNTER3.VHD	Top-level VHDL Source File

The top-level HDL source code is `COUNTER3.V` or `COUNTER3.VHD`. This code instantiates two 8-bit loadable ripple-carry counters, which count from $00 to $3F and $00 to $1F. The counters' ENABLE and RESET lines are active high. The ripple-carry out signals are connected to AVR Interrupt Signals INTA0 and INTA1, respectively.

The file containing the AVR microcontroller source code depends on the programming language and the compiler being targeted, consult the archive contents above to determine the corresponding file to your tool flow. When the AVR senses an interrupt resulting from the first counter's ripple-carry out signal, the Interrupt Service Routine (ISR) for INTA0 is executed. During the ISR for INTA0, the AVR increments the count of INTA0 occurrences and stores the count in the shared dual-port SRAM at location $0F9B. Finally, the ISR places the incremented count on the 8-bit AVR-FPGA Data Bus, which triggers the AVR Write Enable (FPGA signal aWE) and FPGA I/O Select 0 (FPGA signal LOAD), and loads the counter with the value from the AVR-FPGA Data Bus. When the AVR senses an interrupt resulting from the second counter's ripple-carry out signal, the Interrupt Service Routine (ISR) for INTA1 is executed. During the ISR for INTA1, the AVR increments the count of INTA1 occurrences and stores the count in the shared dual-port SRAM at location $0F9C. Finally, the ISR triggers the AVR Write Enable (FPGA signal aWE) and FPGA I/O Select 1 (FPGA signal LOAD), and loads the counter with the value from the shared dual-port SRAM at location $0F9C.

Once the aWE and LOAD signals from either counter are released, the corresponding counter will start counting from the loaded value. When either counter has reached its terminal count, its RCO signal will be driven low and will generate an interrupt to the AVR, causing the corresponding ISR to be executed. This operation will then be repeated.

Simulation

When performing co-verification simulation using Atmel's System Designer software, it is necessary to provide stimulus for the counter's RESET and ENABLE signals. Listed below is the suggested HDL stimulus that should be added to the testbench:

- For VHDL Design Flows:

```
stimulus: process
begin
sig_reset  <= '0';
    sig_enable <= '0';
    wait for 100 ns;

    sig_reset  <= '1';
    wait for 100 ns;

    sig_reset  <= '0';
    sig_enable <= '1';
    wait for 200 us;

  end process stimulus;
```

- For Verilog Design Flows:

```
  initial
  begin
        sig_reset  = 1'b0;
        sig_enable = 1'b0;

    #100 sig_reset  = 1'b1;

    #100 sig_reset  = 1'b0;
         sig_enable = 1'b1;

    #200000;
  end
```

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2327B–FPSLI–03/03/xM