AVR-FPGA Interface Design 1

Features

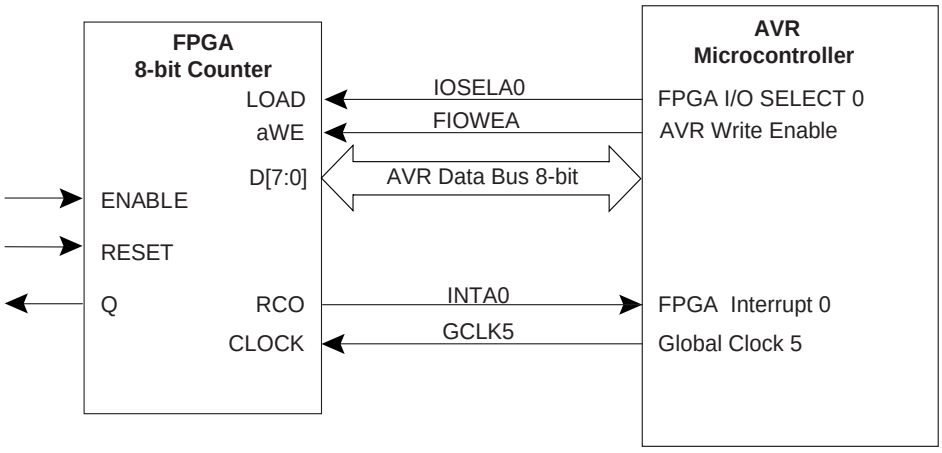
- **Initialization and Use of AVR-FPGA Interface and Interrupts**
- **Full Source Code for AVR® Microcontroller and FPGA Included**

Description

Atmel's AT94K sample designs are provided to familiarize the user with the AT94K FPSLIC™ device. This design is intended to demonstrate the communication between the AVR and FPGA, utilizing the Data Bus, Interrupts and I/O Select signals.

This design is composed of a simple AVR program and a loadable ripple-carry counter implemented in the FPGA. The counter begins counting at zero upon power-up and will generate an interrupt to the AVR using the ripple-carry out signal. The active low interrupt must be held for three clock cycles prior to being acknowledged by the AVR.

Functional Block Diagram



The block diagram shows the connections used in this example, all interface connections are implemented using dedicated resources. This example makes use of the AVR-FPGA Data Bus, one FPGA Interrupt and one I/O Select signal.

Programmable SLI

AT94K

Application Note

Rev. 2325B–FPSLI–09/27/02

Implementation

The AVR source of this design has been implemented in C for the CodeVision AVR, IAR Systems and ImageCraft compilers, and in assembly for the Atmel Assembler. The FPGA design has been implemented in Verilog and VHDL. Each file is commented.

Assuming a default System Designer™ installation, the source files for this application note can be found within the `\SystemDesigner\Examples\AT94K\Coverify\doc2325.zip` archive. Alternatively, the source files may be found in the FPSLIC Software section of the Atmel web site (http://www.atmel.com), under the `doc2325.zip` archive. The source files for the Design 1 are shown in Table 1

Table 1. Source Files for Design 1

File	Description
AT94KDEF.INC	Atmel AVR Assembler FPSLIC Include File
D1-ATML.ASM	Atmel AVR Assembler Design 1 Source File
D1-CVAVR.C	CodeVision AVR Design 1 Source File
D1-IAR.C	IAR Systems Design 1 Source File
D1-ICC.C	ImageCraft Design 1 Source File
COUNTER.V	Top-level Verilog Source File
COUNTER.VHD	Top-level VHDL Source File

The top-level HDL source code is `COUNTER.V` or `COUNTER.VHD`. The code implements an 8-bit loadable ripple-carry counter, which counts from $00 to $3F. The counter's ENABLE and RESET lines are active high. The ripple-carry out signal is connected to the AVR Interrupt Signal INTA0.

The file containing the AVR microcontroller source code depends on the programming language and the compiler being targeted, consult the archive contents above to determine the corresponding file to your tool flow. When the AVR senses an interrupt resulting from the counter's ripple-carry out signal, the Interrupt Service Routine (ISR) for INTA0 is executed. During the ISR for INTA0, the AVR increments the count of INTA0 occurrences and places it on the 8-bit AVR-FPGA Data Bus, which triggers the AVR Write Enable (FPGA signal aWE) and FPGA I/O Select 0 (FPGA signal LOAD), and loads the counter with the value from the AVR-FPGA Data Bus.

Once the LOAD and aWE signals are released, the counter will start counting from the loaded value. When it has reached its terminal count value ($3F), it will drive RCO low and will generate an interrupt to the AVR, causing the ISR to be executed. This operation will then be repeated.

Simulation

When performing co-verification simulation using Atmel's System Designer software, it is necessary to provide stimulus for the counter's RESET and ENABLE signals. Listed below is the suggested HDL stimulus that should be added to the test bench:

- For VHDL Design Flows:

```
stimulus: process
begin
sig_reset  <= '0';
    sig_enable <= '0';
    wait for 100 ns;

    sig_reset  <= '1';
    wait for 100 ns;

    sig_reset  <= '0';
    sig_enable <= '1';
    wait for 200 us;

  end process stimulus;
```

- For Verilog Design Flows:

```
  initial
  begin
        sig_reset  = 1'b0;
        sig_enable = 1'b0;

    #100 sig_reset  = 1'b1;

    #100 sig_reset  = 1'b0;
        sig_enable = 1'b1;

    #200000;
  end
```

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