AT94K Series Configuration

Configuration is the process by which a design is loaded into an AT94K Field Programmable System Level Integrated Circuit (FPSLIC™) device. AT94K Series devices are SRAM based and can be configured any number of times. The entire device or select portions can be configured. Sections can be configured while others continue to operate undisturbed. Full configuration takes only milliseconds. Partial configuration takes even less time and is a function of design density.

Configuration Modes

The FPSLIC configuration process involves configuring the FPGA, the FPSLIC (AVR®) program code and the FPSLIC data memory. This configuration requires a single bitstream that configures the FPGA, the FPSLIC (AVR) Program SRAM and the FPSLIC Data SRAM. The combined bitstream is automatically generated by the Bitstream Generator, a System Designer™ software utility.

The Bitstream Generator takes the output from the FPGA place and route software and the AVR compiler, and generates a single programming file that will program the FPSLIC device by loading the programming code and the configuration memory. The FPSLIC will automatically read out of a configuration memory on power-up. The programming code can also be serially loaded into the FPSLIC device from another microprocessor or downloaded from a PC.

The configuration programming code is transferred to the device in one of three modes (see Table 1). Two dedicated input pins, M_0 and M_2, determine the configuration mode. There is one auto-configuring Master mode, one Slave mode and a Synchronous RAM mode for accessing the SRAM-based configuration memory directly from a parallel microprocessor port.

Table 1. AT94K Series Configuration Modes

Mode	Description	M2	M0	Clock	Data	Notes
0	Master Serial	0	0	Output	Serial	Auto Configuration, Serial EEPROM
1	Slave Serial Cascade	0	1	Input	Serial	Microprocessor or Serial EEPROM
4	Synchronous RAM	1	0	Input	8-bit Word	24-bit Address In, Parallel Port of Microprocessor

FPSLIC™

AT94K Series Field Programmable System Level Integrated Circuit

Application Note

Rev. 2313A–08/01

Master Mode

The Master mode is auto-configuring: after reset and the internal clearing of configuration memory, the FPSLIC device self-initiates configuration. The Master mode uses an internal oscillator to provide CCLK for clocking the external EEPROMs (configurators) which contain a configuration data. CCLK will also drive a downstream device (Slave) in The Master Serial mode clocks and receives data from a EEPROM Serial Configuration Memory (AT17C/LV512, AT17C/LV010). After auto-configuration is complete, reconfiguration can be initiated manually by the user, if needed.

Slave Mode

In Slave mode, configuration is always initiated by an external source. Data is applied to the device on the rising edge of CCLK. In Slave mode, the device receives serial configuration data. CCLK is not generated in Slave mode.

Synchronous RAM Mode

In Synchronous RAM mode, the device receives a 32-bit wide bitstream composed of a 24-bit address and 8-bit wide data. Address, data and write enable are applied simultaneously at the rising edge of CCLK. In this mode the FPSLIC configuration SRAM is seen as a simple memory mapped address space. The user has full write and limited read access to the entire FPSLIC configuration SRAM. The overhead normally associated with bitstreams is eliminated, resulting in faster (re)configuration.

Configuration Pins

There are four basic configuration states of operation. Power-on-reset, occurs when power is first applied to the part. The FPSLIC initiates a complete clearing of all internal configuration SRAM (configuration clear cycle).

The second state, manual reset, occurs when the RESET pin is driven low by the user. Again, the FPSLIC initiates a configuration clear cycle.

The third state is configuration download. In this state the configuration mode is active. The FPSLIC accepts serial or parallel data from an outside source and loads the configuration SRAM appropriately.

The fourth state is idle, when there is no configuration activity.

During configuration, the flow of the programming code to and from the device is controlled by the dedicated mode pins and a number of dual-function pins that double as user I/O (FPGA) under normal programmed operation. The number of dual-function pins required for each mode varies (see Table 2).

The mode pins are dedicated TTL threshold inputs that determine the configuration mode to be used. Table 2 lists the states for each configuration mode. The mode pins should not be changed during power-on-reset, manual reset or configuration download. The user may change the mode pins during configuration idle. These pins have no pull-up resistors to VDD, so they need to be driven by the user, tied off or pulled up/down automatically.

Table 2. Configuration Pins Interface Definition

Pins	State					
			Download			
	Manual Reset	Power-on-Reset	Download Mode 0	Download Mode 1	Download Mode 4	Idle
M_0, M_2	TTL Input	TTL Input	TTL Input	TTL Input	TTL Input	TTL Input
RESET	TTL Input, 50 kΩ Pull-up	TTL Input, 50 kΩ Pull-up	TTL Input, 50 kΩ Pull-up	TTL Input, 50 kΩ Pull-up	TTL Input, 50 kΩ Pull-up	TTL Input, 50 kΩ Pull-up
INIT	Open Drain Bi-directional, 20 kΩ Pull-up	Open Drain Bi-directional, 20 kΩ Pull-down	Open Drain Bi-directional, 20 kΩ Pull-up	Open Drain Bi-directional, 20 kΩ Pull-up	Open Drain Bi-directional, 20 kΩ Pull-up	User I/O
CON	Open Drain Bi-directional, 10 kΩ Pull-up	Open Drain Bi-directional, 10 kΩ Pull-up	Open Drain Bi-directional, 10 kΩ Pull-up	Open Drain Bi-directional, 10 kΩ Pull-up	Open Drain Bi-directional, 10 kΩ Pull-up	Open Drain Bi-directional, 10 kΩ Pull-up
CCLK	Schmitt Trigger Input, 50 kΩ Pull-up	Schmitt Trigger Input, 50 kΩ Pull-down	Output	Schmitt Trigger Input, 50 kΩ Pull-up	Schmitt Trigger Input, 50 kΩ Pull-up	Schmitt Trigger Input, 50 kΩ Pull-up
HDC	Output	Input Pull-down	Output	Output	User I/O	User I/O
LDC	Output	Input Pull-down	Output	Output	User I/O	User I/O
D_0	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-up
$TD_{(7:0)}$	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-down	User I/O	User I/O	Bi-directional	User I/O
$A_{(29:0)}$	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-down	User I/O	User I/O	Input	User I/O
CS0	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-down	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-up
CSOUT	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-down	Optional Output	Optional Output	AVR WTP3 Input, 20 kΩ Pull-up	AVR WTP3 Input, 20 kΩ Pull-up
CHECK	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-down	Check Input	Check Input	Check Input	User I/O
OTS	CMOS Input, 20 kΩ Pull-up	CMOS Input, 20 kΩ Pull-down	OTS Input or User I/O	OTS Input or User I/O	OTS Input or User I/O	OTS Input or User I/O

CCLK

CCLK is the configuration clock pin. It is an input or an output depending on the mode of operation. During power-on-reset or manual reset, it is a tri-stated output. During configuration download in Mode 0, it is an output with a nominal frequency of 1 MHz. During configuration download in all other modes, it is a Schmitt trigger input. It is an input during configuration idle, but is ignored. It is pulled to VDD with a nominal 50 kΩ internal resistor.

RESET

RESET is the FPSLIC manual reset pin. It is available during all configuration states. It initiates a configuration clear cycle and, if operating in Mode 0, an auto-configuration. It is a dedicated Schmitt trigger. It is pulled to VDD with a nominal 50 kΩ internal resistor.

INIT

INIT is a multi-function pin. During power-on-reset and manual reset, the pin functions as an open drain bi-directional I/O which releases high when the configuration clear cycle is complete, but can be held low during reset to hold the device in a reset state. Once released, the FPSLIC will proceed to either configuration download or idle, as appropriate. During configuration download, the INIT pin is again an open drain bi-directional pin which signals if an error (driven low) is encountered during the download of a configuration bitstream. In addition, during the Check Function, the INIT pin drives low for any configuration SRAM mismatch (see the description of the Check Function on page 21 for more details). While in open drain mode, the pin is pulled to VDD with a nominal 20 kΩ internal resistor. When not configuring, the INIT pin becomes a fully functional user I/O.

CON

CON is the FPSLIC configuration start and status pin. It is a dedicated open drain bi-directional pin. During power-on-reset or manual reset, CON is driven low by the FPSLIC. In Slave Modes 1 or 4, when the FPSLIC has finished the configuration clear cycle, CON is released to indicate the device is ready for a configuration download. The user may then drive CON low to initiate a configuration download. After three clock cycles when the preamble has been recognized, CON is then driven low by the FPSLIC until it finishes the download, and it is then released. In Mode 0, CON is not released by the FPSLIC at the end of power-on-reset or manual reset. Instead, CON is controlled by the FPSLIC until the end of the auto-configuration process. CON is released at the end of configuration download in Mode 0, and the user may then leave the device in Mode 0 or change the mode and initiate a configuration download by driving CON low. While in open drain mode, the pin is pulled to VDD with a nominal 10 kΩ internal resistor.

HDC

HDC is the FPSLIC high during configuration pin. It is an output driven high by the FPSLIC during manual reset and configuration download. During configuration idle, the pin is a fully functional user I/O. During power-on-reset, HDC is an input with a normal 20 kΩ internal pull-down resistor.

Note: All user I/O default to inputs with pull-ups “on”. The HDC pin transitions from driving a strong “1” to a pull-up “1” after manual reset. The HDC pin will transition from driving a strong “1” to the user programmed state at the end of configuration download. If it is not programmed, the default state is input with pull-up.

LDC

LDC is the FPSLIC low during configuration pin. It is an output, driven low by the FPSLIC during manual reset and configuration download. During configuration idle, the pin is a fully functional user I/O. During power-on-reset, LDC is an input pull-down with a nominal 20 kΩ internal pull-down resistor.

Note: All user I/O pull-ups and pull-downs are programmed by the user. The LDC pin transitions from driving a strong "0" to a weak "1" after reset. The LDC pin will transition from driving a strong "0" to the user programmed state at the end of configuration download. If it is not programmed, the default state is input with pull-up.

D_0

D_0 is the FPSLIC configuration data line used to download configuration data to the device. The D_0 is a dedicated CMOS input with a nominal 20 kΩ internal pull-up resistor.

TD_0:TD_7

TD_0:TD_7 are the 8 bits of the parallel data bus used in Synchronous RAM mode to download configuration data to the device. During manual reset, TD_0:TD_7 are controlled by the configuration SRAM. The TD_0:TD_7 pins will transition from the user programmed state to CMOS inputs with nominal 20 kΩ internal pull-up resistors as the SRAM at those locations is cleared by the configuration clear cycle. During power-on-reset, TD_0:TD_7 are inputs with nominal 20 kΩ internal pull-down resistors switching to nominal 20 kΩ internal pull-up resistors at the end of the configuration clear cycle. TD_0:TD_7 are not used in the serial Modes 0 and 1.

A_0:A_{29}

A_0:A_{29} are used to control the FPSLIC configuration SRAM, the Data SRAM, and the AVR Program SRAM addressing in Mode 4 configuration downloads. During manual reset, A_0:A_{29} are controlled by the configuration SRAM. The A_0:A_{29} pins will transition from the user programmed state to CMOS inputs with nominal 20 kΩ internal pull-up resistors as the SRAM at those locations is cleared by the configuration clear cycle. A_0:A_{29} are used only in Mode 4 Synchronous RAM mode. During power-on-reset, A_0:A_{29} are inputs with nominal 20 kΩ internal pull-down resistors switching to nominal 20 kΩ internal pull-up resistors at the end of the configuration clear cycle. Bits A_{24}:A_{29} are for future memory expansion and are consistently ignored.

CS_0

CS_0 is an FPSLIC configuration chip select. It is active low. The CS_0 pin is dedicated to a CMOS input with a nominal 20 kΩ internal pull-up resistor. In Mode 1, it is used as a chip select to enable configuration to begin. It is most often used as the chip select of the downstream device in a cascade chain, and is usually driven by CSOUT of the upstream device. Releasing CS_0 during configuration causes the Mode 1 FPSLIC to abort the download and release CON. CS_0 is used only in Mode 1.

CSOUT

CSOUT is the configuration pin used to enable the downstream device in a cascade chain. During configuration download, CSOUT becomes an optional output. It is enabled by default after reset, and may be enabled or disabled via the configuration control register. If the user has disabled the cascade function, control of CSOUT is turned over to the AVR (INTP3.) If the cascade function is enabled, the CSOUT pin is driven high at the start of configuration download. At the end of the device's portion of the cascade bitstream, the CSOUT pin is driven low (and into the CS_0 of the downstream device) to enable the downstream device. CSOUT is released by the device at the end of the cascade bitstream and becomes a fully functional user I/O.

Note: AVR I/O default to inputs with nominal 20 kΩ internal pull-up resistors following manual reset or power-on-reset.

CHECK

CHECK is a configuration control pin used to control the Check Function. The Check Function takes a bitstream and compares it to the contents of a previously loaded bitstream and notifies the user of any differences. Any differences causes the INIT pin to go low. During configuration download, CHECK becomes an optional input. It is enabled by default after reset, and may be enabled or disabled via the configuration control register. If the user has disabled the Check Function, is turned over to the AVR (PE7 - PortE, bit 7).

Note: AVR I/O default to inputs with nominal 20 kΩ internal pull-up resistors following manual reset or power-on-reset.

OTS

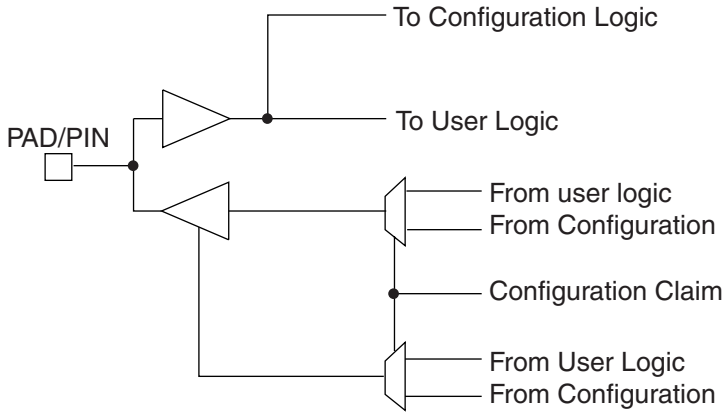
OTS is an input pin used to immediately tri-state all user I/O. It is enabled by a bit in the configuration control register. Once activated in the configuration control register, it is always an input. The OTS tri-state control of Dual Use pins is superseded by the configuration logic's claim on those pins. If the user has disabled the OTS function, the pin remains as User I/O.

Dual Use I/O

Any pin which functions as user I/O and configuration I/O is a Dual Use I/O pin. INIT, HDC, LDC, TD_0:TD_7, A_0:A_{29}, CSOUT, CHECK, and OTS are all Dual Use I/O pins. It must be noted that while the configuration logic controls Dual Use I/O pins during a particular mode of operation, the configuration logic does not control the pull-up, pull-down, CMOS/TTL threshold select or Schmitt trigger selects. The user must be cautioned to avoid possible system problems with the use of Dual Use I/O pins. For example, turning off the internal pull-up resistor for the open drain INIT pin would not apply the weak high required of an open drain driver. Conversely, disabling the pull-up and enabling the pull-down of the HDC pin might be a good idea, since the user may then actually see the pin go low at the end of configuration.

Dual Use pins share input buffers. It should be noted that even when the configuration has claimed a pin for its own purposes, the user input buffer is still fully functional. This implies that any internal user logic tied to the input buffers of the pins in question will remain operational (see Figure 1).

Figure 1. Dual Use IO



Configuration States

When power is first applied to an AT94K Series FPSLIC device, an internal power-on-reset circuit senses VDD and activates at approximately 1.9V. The FPSLIC then enters the power-on-reset state. During this state, INIT is pulled low, CON is driven low, LDC is pulled low (input), HDC is pulled low (input), and all user I/O are tri-stated pulled low. I/O thresholds are at an indeterminate state. The FPSLIC configuration clear cycle begins and the configuration SRAM is reset. The configuration clear cycle is repeated a nominal 150 ms to allow VDD to rise to the minimum operational level for the device.

This additional delay is only applied at power-on-reset, (not required for manual reset.)

Once the configuration clear cycle is complete, INIT is driven low, CON remains driven low, LDC is driven low (output), HDC is driven high (output) and all user I/O are tri-stated (input) and pulled high; then RESET is sampled. If high, INIT is released. This open drain pin is sampled to make sure all other devices (if any) in a cascade chain are also done with the configuration clear cycle. Once INIT goes high the mode pins are sampled.

If Mode 0 is detected, the part proceeds to the configuration download state. CON is held low by the FPSLIC, HDC remains high, LDC remains low and CCLK is now driven by the FPSLIC at a nominal frequency of approximately 1 MHz. The appropriate configuration interface pins for Mode 0 become active.

If a Slave mode is detected (i.e., Mode 1), then CON is released and pulled high with the internal pull-up resistor. Once CON goes high, the part proceeds to the idle state and LDC and HDC are released. The internal oscillator stops running. The part is now available for configuration download.

When RESET is lowered, the manual reset state is entered. An internal oscillator begins running, INIT is driven low, CON is driven low, LDC is driven low and HDC is driven high. During this state, the FPSLIC configuration clear cycle begins and the configuration SRAM is reset. All user I/O, will transition from their user programmed state to a CMOS input with nominal 20 kΩ internal pull-up resistor as the SRAM at that location is cleared. Once this cycle is complete, RESET is sampled and the reset state machine proceeds as above. The configuration reset state diagram is shown in Figure 2.

After a configuration clear cycle, the user logic in the FPGA array of the FPSLIC is set to a benign state. The following chart shows the various types of user circuitry and their default states.

There is no activity in either the user logic or the configuration logic and the device is in a low power state.

Table 3. Configuration Clear Cycle Times

Device	FPGA Array Size	FPGA SRAM Size	Clear Cycle Time			Units
			Min	Typ	Max	
AT94K05	16 x 16	2048	137	228	365	µs
AT94K10	24 x 24	4096	197	328	525	µs
AT94K40	48 x 48	18432	377	628	1005	µs

Table 4. User Circuitry and Default States

User Circuitry	Default State
Core	Inputs Tied Off Local Drivers Off DFF Set
Repeater	All Drivers Off Passgates Off
I/O	Output Drivers Off CMOS Threshold Pull-up Enabled Pull-down Disabled
Clocks	Tied High
Resets	Tied Low (Active)
FreeRAM™	Disabled Contents Cleared

The AT94K FPSLIC allows complete reconfigurability down to the byte level. The Cache Logic® architecture lets users reconfigure part of the FPSLIC while the rest of the FPSLIC continues to operate unaffected.

Control of the FPSLIC system level interface is possible on an AT94K Series FPSLIC. User I/O, internal Global Set/Reset, and Global and Fast Clocks can be enabled or disabled during configuration downloads by setting bits in the system control register (SCR.)

User I/O become active as soon as the relevant I/O configuration SRAM is loaded. To aid system level integration, a bit in the system control register (SCR_{31}) may be set to command all I/O pins that are not part of the configuration interface to tri-state. This bit is set at the start of configuration so the very first download can be affected.

Another bit in the system control register (SCR_{30}) may be set to enable (drive low) the global reset net during configuration download, allowing the user to post all configured logic into a known state.

Another set of bits in the system control register (SCR_{25}:SCR_{16}) may be set to disable (drive high) each of the Global and Fast Clock input buffers which drive the FPGA clock nets. The user I/O portion of these buffers is not affected.

Holding off Auto-configuration

There are two methods by which the user may delay a master Mode 0 auto-configuration. The first is to drive RESET low during power-on-reset or manual reset and hold the signal low until the user is ready to proceed with auto-configuration. The second is to drive INIT low with an open drain driver during power-on-reset or manual reset and release when the user is ready to proceed with auto-configuration. Both are valid in a AT94K Series device. Assuming the device has completed its configuration clear cycle and that INIT and RESET are inactive (high), a Mode 0 FPSLIC starts CCLK and configuration download.

System Control Register

The first 4 bytes of the 8-byte System Control Register (bits SCR[31:0]) are set in the header portion of the bitstream. The remaining 4 bytes (bits SCR[63:32]) must be set in a bitstream window. Each 4-byte block is treated separately by the configuration logic so the System Control Register has been broken down into two tables, see Table 5 and Table 6. The System Designer software allows to set the system control register in the bitstream utilities.

Figure 2. Configuration Reset State Diagram

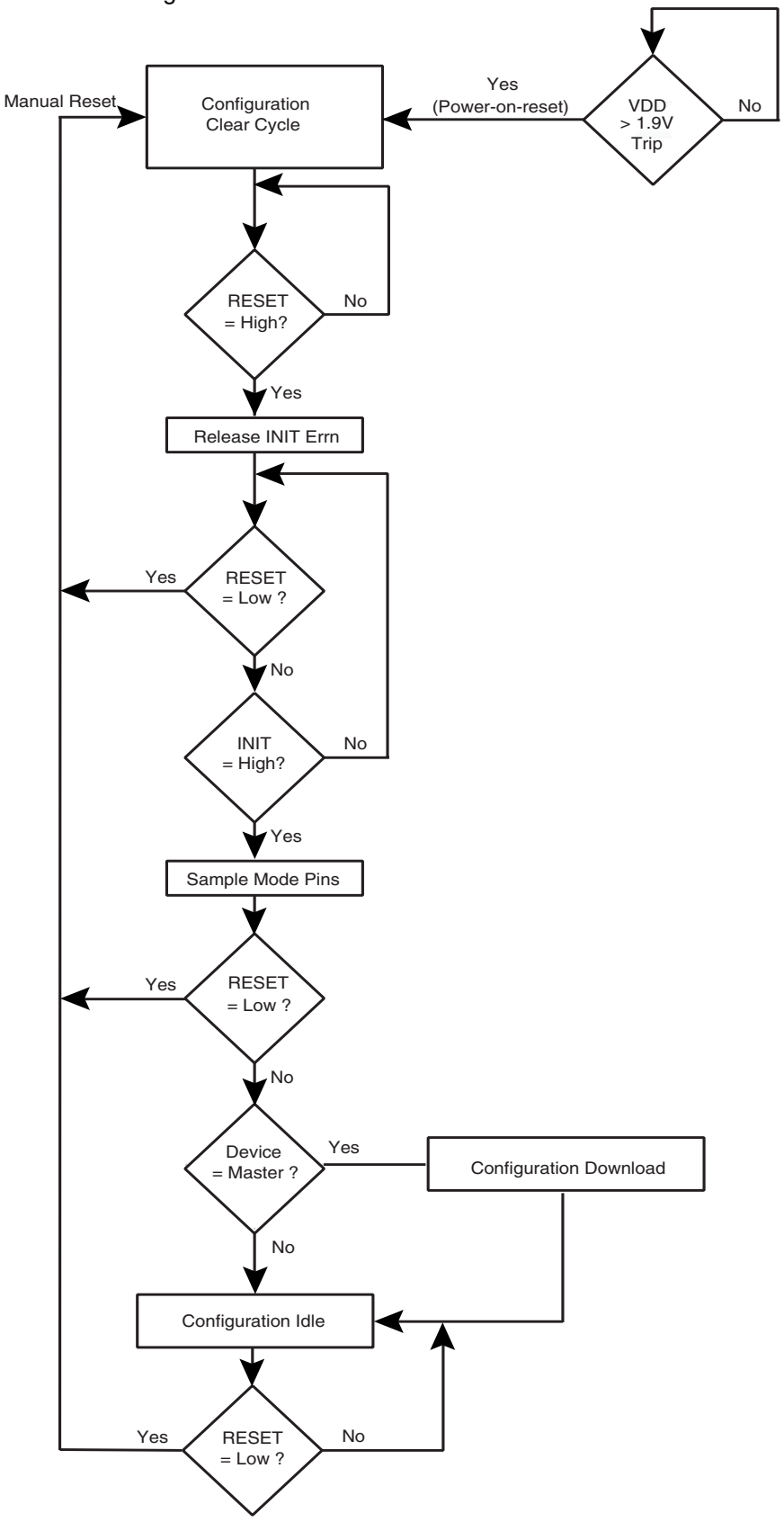


Table 5. System Control Register Bytes [3:0]

SCR Bit	Scope	Comment
31	I/O Tri-state	1 = I/O Tri-state Active During Configuration
30	Global Set/Reset	1 = Global Set/Reset (active low) During Configuration
29	AVR Real Time Monitor	1 = Enable AVR Real Time Monitor
28	Reserved	
27	Reserved	
26	Reserved	
25	Fast Clock 1	1 = Fast Clock 1 Disabled During Configuration
24	Fast Clock 0	1 = Fast Clock 0 Disabled During Configuration
23	Global Clock 8	1 = Disabled During Configuration
22	Global Clock 7	1 = Disabled During Configuration
21	Global Clock 6	1 = Disabled During Configuration
20	Global Clock 5	1 = Disabled During Configuration
19	Global Clock 4	1 = Disabled During Configuration
18	Global Clock 3	1 = Disabled During Configuration
17	Global Clock 2	1 = Disabled During Configuration
16	Global Clock 1	1 = Disabled During Configuration
15	Reserved	
14	Reserved	
13	Reserved	
12	Reserved	
11	Reserved	
10	Reserved	
9	Reserved	
8	Reserved	
7	Reserved	
6	OTSn Pin Enable	1 = Enable OTSn Pin Special Function
5	Reserved	
4	Configuration Memory Lockout	1 = Configuration Memory Lockout Enabled
3	Check Function	1 = Check Function Disabled (Checkn Inactive)
2	Cascade Control	1 = Cascade Disabled (Csoutn Inactive)
1	Reserved	
0	Reserved	

Table 6. System Control Register Bytes [7:4]

SCR	Scope	Comment
63	Frame Interface	1 = Enable Frame Interface
62	AVR Cache Interface	1 = Enable AVR Cache Interface
61	Global Clock 6 Mux Select Bit 1	
60	Global Clock 6 Mux Select Bit 0	
59	Reserved	
58	Reserved	
57	TOSC Internal Bias Resistor	1 = Enable Internal Bias Resistor
56	XTAL Internal Bias Resistor	1 = Enable Internal Bias Resistor
55	AVR Port E Drive	1 = Full 20 mA Drive
54	AVR Port D Drive	1 = Full 20 mA Drive
53	UART1 Tx/Rx Pins	1 = TX1/RX1; 0 = UART1 Tx/Rx Shared with PE2/PE3
52	UART0 Tx/Rx Pins	1 = TX0/RX0; 0 = UART0 Tx/Rx Shared with PE0/PE1
51	External Interrupt 3 Pin	1 = INTP3; 0 = External Interrupt 3 Shared with PE7
50	External Interrupt 2 Pin	1 = INTP2; 0 = External Interrupt 2 Shared with PE6
49	External Interrupt 1 Pin	1 = INTP1; 0 = External Interrupt 1 Shared with PE5
48	External Interrupt 0 Pin	1 = INTP0; 0 = External Interrupt 0 Shared with PE4
47	Reserved	
46	Reserved	
45	Reserved	
44	Reserved	
43	Reserved	
42	Reserved	
41	AVR Shared Program/Data Bit 1	(See AVR Program/Data SRAM Partitioning)
40	AVR Shared Program/Data Bit 0	(See AVR Program/Data SRAM Partitioning)
39	Reserved	
38	Frame Clock Phase Select	1 = Non-inverted Frame Clock
37	Program Boot Sector Write Protect	1 = Disable Write Protect During Frame Writes
36	Program SRAM Write Protect	1 = Disable Write Protect During Frame Writes
35	AVRResetn Pin	1 = Enable AVRResetn Pin (Active Low)
34	Reserved	
33	Reserved	
32	Reserved	

Quick Facts

- Configuration download overrides the AVR Program memory write protect bits in SCR (refer to the “System Control Register” on page 9). Write protect bits only limit access from the AVR or FPGA interface and not the configuration interface. Write protect bits are ignored by the configuration control logic.
- The configuration control logic has no access to the AVR core registers or the AVR IO registers.

System Control Register Bits [63:0]

Byte 7

SCR[63]: Frame Interface

0 = Disable FPGA Read/Write FPSLIC (AVR) SRAM

1 = Enable FPGA Read/Write FPSLIC (AVR) SRAM

SCR[62]: AVR Cache Interface

0 = Disable AVR Write FPGA Configuration SRAM

1 = Enable AVR Write FPGA Configuration SRAM

SCR[61:60]: Global Clock 6 Mux Select Bits

Table 7. Global Clock 6 Mux Select

SCR61	SCR60	Global Clock 6
0	0	“1”
0	1	AVR System Clock (osc)
1	0	Timer Counter Clock (tosc)
1	1	Watchdog Timer Clock (iosc)

SCR[59]: *Reserved*

SCR[58]: *Reserved*

SCR[57]: TOSC Internal Bias Resistor

0 = Disable Internal Bias Resistor

1 = Enable Internal Bias Resistor

SCR[56]: XTAL Internal Bias Resistor

0 = Disable Internal Bias Resistor

1 = Enable Internal Bias Resistor

Byte 6

SCR[55]: AVR Port E Drive

0 =6 mA Drive

1 =20 mA Drive

SCR[54]: AVR Port D Drive

0 =6 mA Drive

1 =20 mA Drive

SCR[53]: UART1 Tx/Rx Pins

0 = UART1 Tx Pin Shared with PE2; UART1 Rx Pin Shared with PE3

1 = UART1 Tx Pin is TX1; UART1 Rx Pin is RX1

SCR[52]: UART0 Tx/Rx Pins

0 = UART0 Tx Pin Shared with PE0; UART0 Rx Pin Shared with PE1

1 = UART0 Tx Pin is TX0; UART0 Rx Pin is RX0

SCR[51]: External Interrupt 3 Pin

0 = External Interrupt 3 Pin is Shared with PE7

1 = External Interrupt 3 Pin is INTP3

SCR[50]: External Interrupt 2 Pin

0 = External Interrupt 2 Pin is Shared with PE6

1 = External Interrupt 2 Pin is INTP2

SCR[49]: External Interrupt 1 Pin

0 = External Interrupt 1 Pin is Shared with PE5

1 = External Interrupt 1 Pin is INTP1

SCR[48]: External Interrupt 0 Pin

0 = External Interrupt 0 Pin is Shared with PE4

1 = External Interrupt 0 Pin is INTP0

Byte 5

SCR[47:42]: *Reserved*

SCR[41:40]: AVR Program/Data SRAM Partitioning Bits

Table 8. AVR Program / Data SRAM Partitioning

SCR41	SCR40	Program/Data Partitioning
0	0	16K x 16/4K x 8
0	1	14K x 16/8K x 8
1	0	12K x 16/12K x 8
1	1	10K x 16/6K x 8

Byte 4

SCR[39]: *Reserved*

SCR[38]: Frame Clock Phase Select

0 = Inverted Frame Clock

1 = Non-inverted Frame Clock

By default, the user-selected Frame Clock is inverted at the FPSLIC (AVR) SRAM. By setting this bit (one) the inversion stage is bypassed.

SCR[37]: AVR Program Boot Sector Write Protect Disable

0 = AVR SRAM Boot Sector is Protected from FPGA Writes

1 = AVR SRAM Boot Sector is NOT Protected from FPGA Writes

This Bit is Overridden During Configuration Download

SCR[36]: AVR Program SRAM Write Protect Disable

0 = AVR SRAM is Protected from FPGA Writes (Excludes Boot Sector)

1 = AVR SRAM is NOT Protected from FPGA Writes (excludes Boot Sector)

This Bit is Overridden During Configuration Download

SCR[35]: AVRResetn Pin Enable

0 = Disable AVRResetn Pin Function

1 = Enable AVRResetn Pin Function

SCR[34]: *Reserved*

SCR[33]: *Reserved*

SCR[32]: *Reserved*

Byte 3

SCR[31]: I/O Tri-state

0 = Disable I/O Tri-state During Configuration

1 = Enable I/O Tri-state – forces all user defined I/O pins to tri-state during configuration download. Tri-state is released at the end of configuration download on the rising edge of CON.

SCR[30]: Global Set/Reset

0 = Global Set/Reset NOT Controlled by User During Configuration

1 = Global Set/Reset Controllable by User(Active Low) – allows the Global Set/Reset to hold the core DFFs in reset during configuration download. The Global Set/Reset is released at the end of configuration download on the rising edge of CON.

SCR[29]: AVR Real Time Monitor

0 = Disable AVR Real Time Monitor

1 = Enable AVR Real Time Monitor

Real Time Monitor allows the user to externally visualize the AVR instruction bus and program counter in real time. The AVR must be placed into Debug Mode by setting the DBG bit in the Software Control Register (SFTCR).

SCR[28]: *Reserved*

SCR[27]: *Reserved*

SCR[26]: *Reserved*

SCR[25:24]: Fast Clock [1:0] Configuration Disable

0 = Enable Fast Clock [1:0]

1 = Disable Fast Clock [1:0] During Configuration – allows the user to disable the input buffers driving the Fast Clocks. The clock buffers are enabled and disabled synchronously with the rising edge of the respective FCLK [1:0] signal, and stop in a high (“1”) state. Setting the bit disables the appropriate FCLK [1:0] input buffer only and has no effect on the connection from the input buffer to the FPGA array.

Byte 2

SCR[23:16]: Global Clocks [8:1] Configuration Disable

0 = Enable Global Clock [8:1]

1 = Disable Global Clock [8:1] During Configuration – allows the user to disable the input buffers driving the Global Clocks. The clock buffers are enabled and disabled synchronously with the rising edge of the respective GCLK [8:1] signal, and stop in a high (“1”) state. Setting the bit disables the appropriate GCLK [8:1] input buffer only and has no effect on the connection from the input buffer to the FPGA array.

Byte 1

SCR[15:14]: *Reserved*

SCR[13]: *Reserved*

SCR[12]: *Reserved*

SCR[11]: *Reserved*

SCR[10]: *Reserved*

SCR[9]: *Reserved*

SCR[8]: *Reserved*

Byte 0

SCR[7]: *Reserved*

SCR[6]: OTS Pin Enable

0 = Disable OTS Pin Special Function

1 = Enable OTS Pin Special Function – makes the OTS pin an active low input which controls global tri-state for all user I/O.

SCR[5]: *Reserved*

SCR[4]: Configuration Memory Lockout (FPSLIC Security Bit)

0 = Disable Memory Lockout

1 = Enable Memory Lockout – any *subsequent* configuration download initiated by the user, whether a normal download or a Check function download, causes the InitnErrn pin to immediately activate. CON is released, and no further configuration actively takes place. The download sequence during which SCR[4] is set is NOT affected. Further *subsequent* writes to the System Control Register are also prohibited, so bit SCR[4] may only be cleared by a power on reset or manual reset.

SCR[3]: Check Function Disable

0 = Enable Check Function

1 = Disable Check Function – the CHECKN pin is not used by configuration during downloads.

SCR[2]: Cascade Control Disable

0 = Enable Cascading

1 = Disable Cascading – the CSOUTN pin is not used by configuration during downloads.

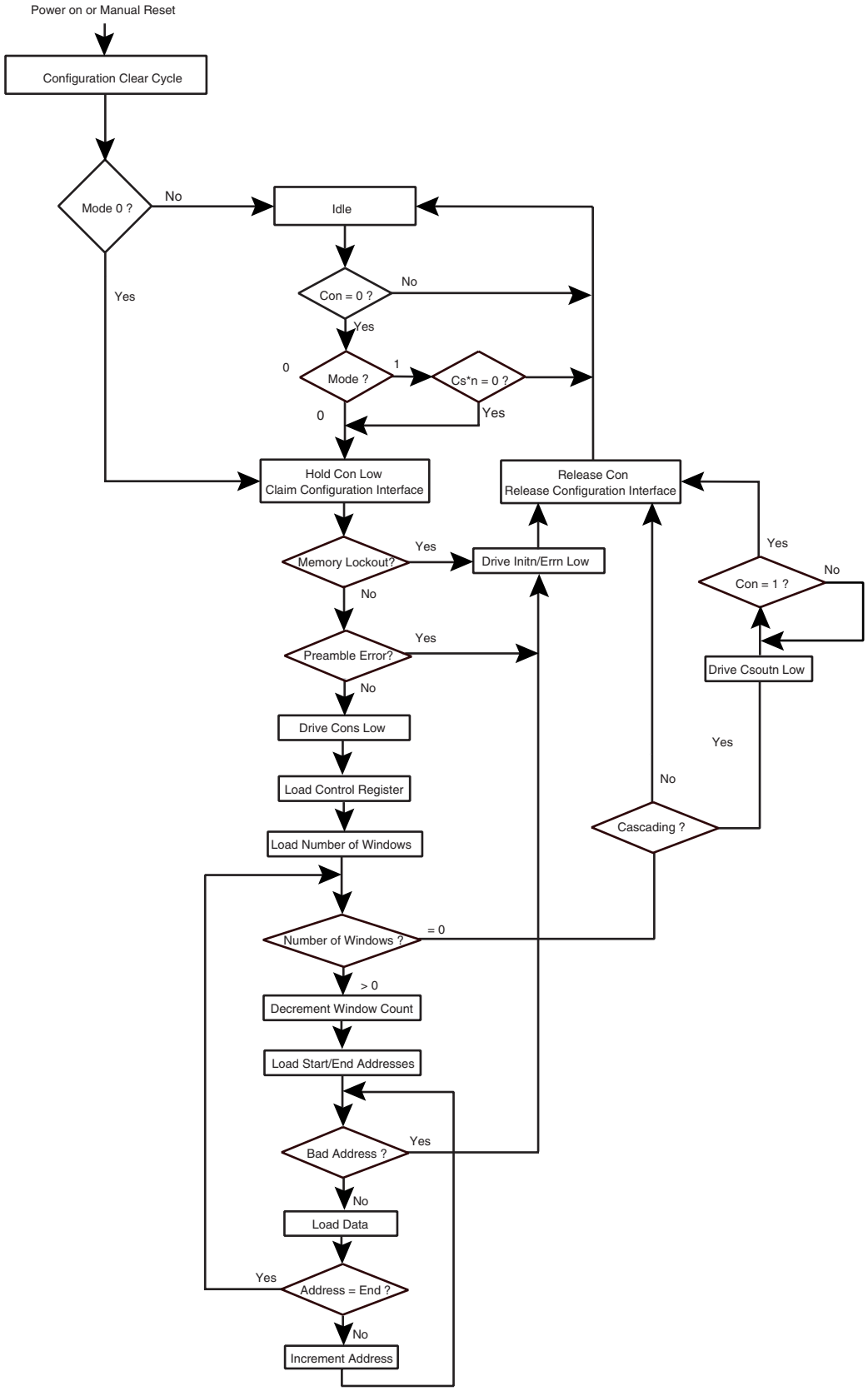
SCR[1]: *Reserved*

SCR[0]: *Reserved*

Configuration Downloads

The initiation of writing, reading or checking design specific data into the FPSLIC configuration SRAM is called configuration download. Configuration downloads are executed by a synchronous state machine that controls the flow of data into the FPSLIC (Figure 3). The state machine is clocked by CCLK. On the rising edge of each CCLK a bit or byte of the configuration data bitstream is clocked into the device. Table 9 displays a sample bitstream for an AT94K Series device.

Figure 3. Configuration Download State Machine



Note: Mode 4 Download is discussed in a separate application note.

Table 9. Sample 8-bit wide stream

8-bit Wide Stream	Description
00000000	Null Byte
10110111	Preamble
00000100	SCR(31:24)
00100000	SCR(23:16)
00000000	SCR(15:08)
10000001	SCR(7:0)
00000000	# Windows MSB
00000010	# Windows LSB
00000000	Start Address Window 0
00000000	Start Address Window 0
11010100	Start Address Window 0
00000000	End Address Window 0
00000000	End Address Window 0
11010111	End Address Window 0
01000000	SCR(63:56)
00000010	SCR(55:48)
00010000	SCR(47:40)
01000010	SCR(39:32)
00000000	Start Address Window 1
00001001	Start Address Window 1
01100100	Start Address Window 1
00000000	End Address Window 1
00001001	End Address Window 1
01100101	End Address Window 1
10101010	Data Byte
01010101	Data Byte
11100111	Postamble

Note: Serial data is read in MSB first. Not applicable to Mode 4.

When CON and the chip select (CS_0) are activated from the power-on-reset, manual reset or the configuration idle state, the device begins clocking data. For AT94K Series devices, the timing relationships are fixed and no additional data is allowed at the front of the bitstreams. Serial data is read in most-significant-bit first.

The null byte is read in, followed by the preamble. If the expected preamble value is not seen as the second byte of data, an error is reported by driving INIT low and terminating the configuration download.

After the preamble check, the state machine loads the system control register, which controls various features of the configuration process.

Small areas of the AT94K arrays can be programmed independently of each other. Each of these areas is known as a window. After the system control register, the device loads the number of configuration windows. A single bitstream can have up to 64-Kbit windows. The minimum data block size for a window is 1 word.

Next, the start and End addresses of the first window are loaded. An invalid Start address will cause an error; the INIT pin is driven low, and the configuration download is terminated.

Next, data is loaded into the configuration SRAM, FPSLIC Data SRAM or the AVR Program SRAM (unless the CHECK function is activated).

Next, if more than one window is to be downloaded, start and End addresses are loaded, followed by another data block. This process is repeated until all windows are downloaded.

Finally, the postamble byte is downloaded. If the expected postamble value is not seen as the last byte of data, an error is reported by driving INIT low and terminating the configuration download.

Full vs. Partial Bitstreams

In programming an AT94K Series FPSLIC, the user will normally load the entire configuration SRAM memory map from start to finish. This requires a full bitstream. Bitstream sizes are shown in Table 10.

It is possible, by using the windowing mechanism, to download the SRAM memory map in smaller segments. By this means, the user may load portions of the array before others, eliminate the loading of unused portions of the array, and overwrite previously written portions of configuration SRAM with new design information.

AT94K software tools (System Designer) supports bitstream compression. .

Table 10. AT94K Series Bitstream Sizes

Device	FPGA Array Size	FPGA Array Bytes[1]	FPGA Array Bits	Data/ Program SRAM Size (Max) Bytes	Data/ Program SRAM Size Bits	Total Configurator Bits[2]	Suggested Configurator
AT94K05AL	16 x 16	7835	62680	20 Kbits (20480)	163840	226520	AT17LV256
AT94K10AL	24 x 24	16947	135576	36 Kbits (36864)	294912	430488	AT17LV512
AT94K40AL	48 x 48	65115	520920	36 Kbits (36864)	294912	815382	AT17LV010

Notes: 1. FPGA configuration bytes assume the low power option is enabled in the software, if the low power option is disabled, the device requires fewer configuration bits
2. Unused configurator bits may be used for nonvolatile memory data storage in-system. For more information see the “C Code for Interfacing FPSLIC AVR Core to AT17 Series Configuration Memories” application note.

Check Function

The AT94K family supports a Check Function on configuration SRAM data (a write verify). This is accomplished by normally initiating a configuration download while driving CHECK low. Instead of writing the contents of the bitstream to memory, the contents of memory are read and compared to the bitstream on a byte-by-byte basis in the configuration logic. Any differences are reported by driving the INIT pin low. The INIT pin will lower two clocks after the mis-compare. The Check Function is available after power-on-reset and manual reset, and can be performed on an “empty” FPSLIC prior to the first programming of the device. Windowed or non-windowed bitstreams may be checked. Although the check function does not write the configuration SRAM contents, the system control register is written. The system control register is not checked. Start and End addresses are examined for integrity, as they are in every download, but only the data at those addresses is “checked”. The contents of the Checksum registers cannot be verified with the Check Function.

The maximum CCLK frequency when performing a Check Function is much lower than that of a normal download. Exact timing specifications are listed under the mode descriptions later in this document.

The bitstream download will not be terminated on a Check Function error (mis-compare).

Checksum Function

The AT94K family supports a Checksum Function. During a configuration download, an accumulated Checksum is calculated after each word (8 bits) of the bitstream is downloaded to the FPSLIC. During the bitstream download, the user may write to a series of registers in a special window known as the Checksum Page.

Table 11. Checksum Page

Byte	Comment
Byte 0	Evaluate Checksum, bits 7:0
Byte 1	Evaluate Checksum, bits 15:8
Byte 2	Seed, bits 7:0
Byte 3	Seed, bits 15:8

After power-on-reset, the Checksum and Seed are cleared to zero. Just prior to the start of a configuration download, the Seed value is loaded into the Checksum . Whenever the Evaluate Checksum register(s) are written, a new Checksum is calculated. If the new value does not equal “FF”, the INIT pin is driven low to indicate an error has occurred. Whenever the Seed is written, the Checksum accumulator is also written with the new Seed value.

The bitstream will not be terminated on a Checksum Function error. Contact fpslic@atmel.com for more details.

Bitstream Errors

The INIT pin is driven low by the FPSLIC for a number of reasons. In all cases, the INIT pin will be driven low two clocks after the byte which caused the error. Some errors will cause a bitstream to be terminated. Some will not. If a bitstream is terminated, all configuration pins are released by the configuration logic and the configuration state returns to Idle.

A bad preamble causes the INIT pin to be driven low and causes the bitstream is terminated.

A bad window Start address or End address causes the INIT pin to be driven low two clocks after the third byte of the End address is seen by the device. The bitstream is terminated.

If the number of windows has been decremented to zero and the expected postamble is not seen by the device, the INIT pin is driven low two clocks after the bad byte is seen by the FPSLIC. The bitstream is terminated.

During a Check Function, a mismatched write-verify error results in the INIT pin being driven low two clocks after the byte. The INIT pin will remain low until the end of the bitstream. The bitstream will not terminate.

If the Security Flag bit was set in the previous bitstream, the FPSLIC will drive the INIT pin low two clocks after CON was driven low by the user. The bitstream will immediately terminate.

If a Checksum error is detected during a bitstream download, the INIT pin is driven low two clocks after the write to the Checksum Page. The INIT pin will remain low until the end of the bitstream. The bitstream will not terminate.

Synchronous RAM Configuration Downloads (Mode 4)

The AT94K family supports the writing and reading of design specific data to or from the FPSLIC configuration SRAM (configuration data and AVR program) by means of a simple single port synchronous SRAM type interface. This interface requires no configuration state machine during the download process.

To protect user designs, detailed bitstream information and detailed use of this mode are not published in this document. For further information on using AT94K devices in dynamically reconfigurable systems using Mode 4, please contact your local Atmel sales office; a Non-disclosure Agreement (NDA) will be required for this document to be disclosed.

Configuration and System Level Integration

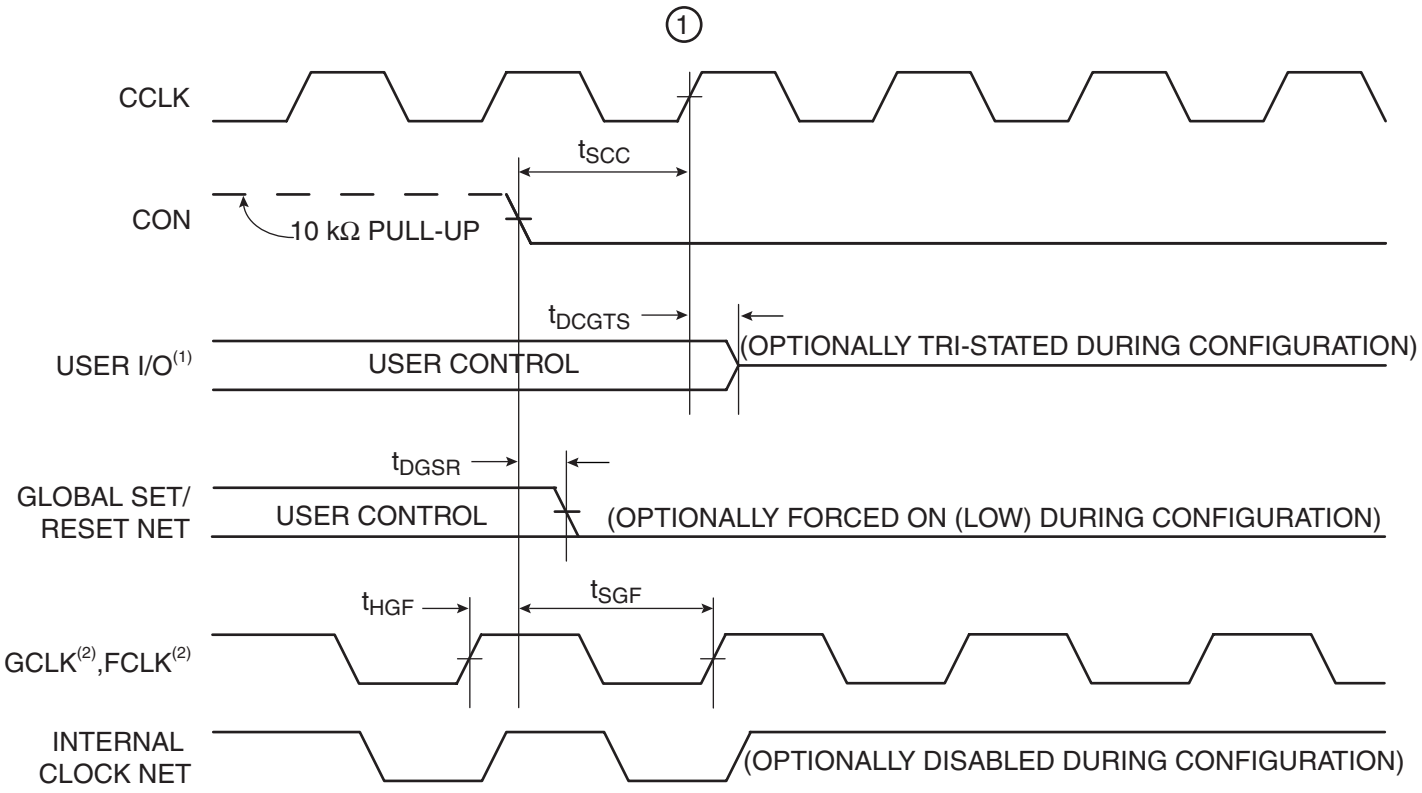
To aid in system level integration, AT94K Series devices have available a number of bits in the system control register which cause the I/O pins to tri-state, the Global Set/Reset network to activate (low), and the Global and Fast Clock input buffers to be disabled (high).

At the start of configuration, these functions go through a fixed timing sequence whereby they are enabled (if selected by the system control register). When CON is driven low by the user, HDC, LDC, INIT and any Dual Use I/O pins needed for the appropriate FPSLIC mode are claimed immediately by the configuration logic. All I/O not needed by the configuration logic are tri-stated on the falling edge of CON. The Global Set/Reset net is forced low on the falling edge of CON. The Global and Fast Clock nets are disabled (driven high) on the first rising edge of the appropriate GCLK or FCLK signal after the falling edge of CON. Figure 4 shows the timing relationships of these functions at the start of configuration.

At the end of configuration, these functions go through a fixed timing sequence whereby they are disabled. When CON is released and pulled high by the FPSLIC, HDC, LDC, INIT and any Dual Use I/O pins needed for the appropriate FPSLIC mode are released immediately by the configuration logic. All other I/O become active (as programmed by the user) on the rising edge of CON. The Global Set/Reset net is released on the second rising edge of CCLK after the rising edge of CON. The Global and Fast Clock nets are released on the first rising edge of the appropriate GCLK or FCLK signal after the second rising edge of CCLK after the rising edge of CON. Figure 5 shows the timing relationships of these functions at the end of configuration.

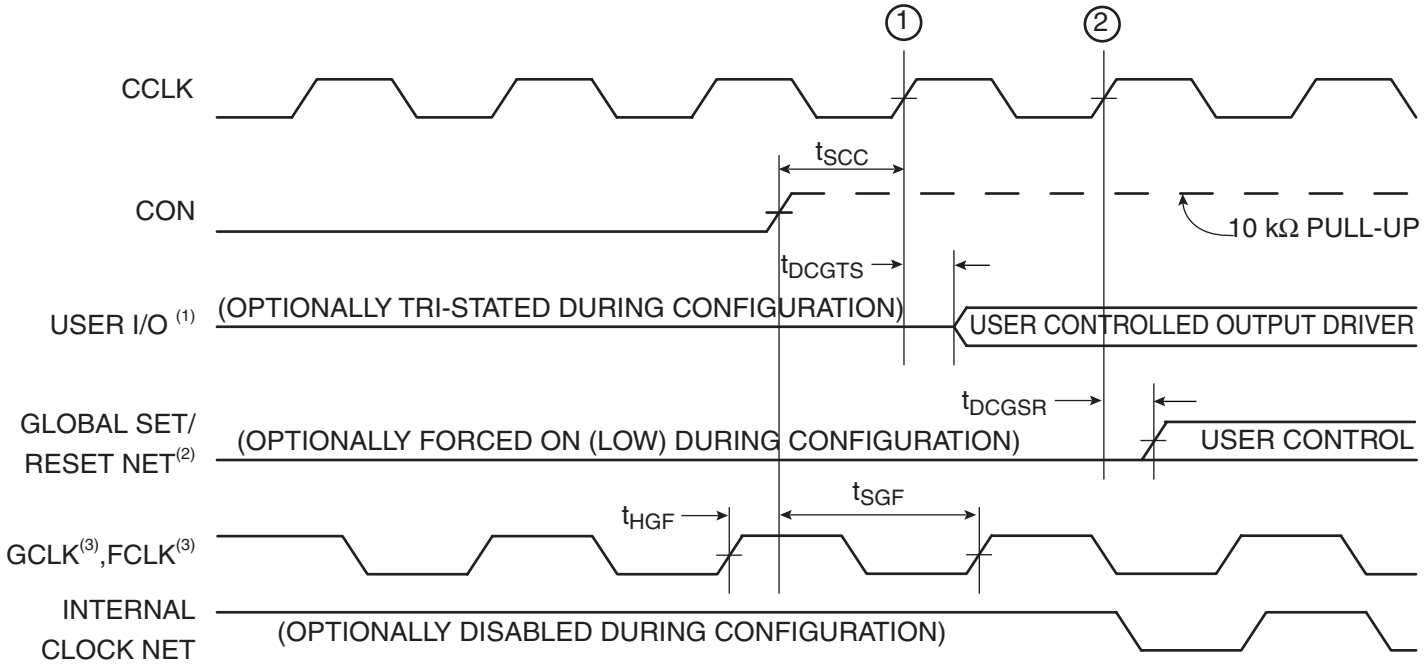
During a normal download, the I/O, the clock tree and the Global Set/Reset nets are loaded near the very end of configuration. The system control register is loaded at the beginning of the bitstream, so the system integration bits for I/O tri-state, Global and Fast Clocks and Global Set/Reset nets can be set while those portions of the FPSLIC are still inactive. This implies that no system integration problems will occur on the first download after power-on-reset or manual reset.

Figure 4. System Level Integration: Start of Configuration



Notes: 1. User I/O are tri-stated on the first rising edge of CCLK after CON has been driven low
2. The appropriate Global and Fast Clock nets are disabled on the first rising edge of the associated Global or Fast Clock input signal after CON is driven low. The nets are forced high for glitchless suppression of activity.

Figure 5. System Level Integration: End of Configuration



Notes:
1. User I/O output drivers are enabled on the first rising edge of CCLK after CON has been released high.
2. The Global Set/Reset net is no longer forced on (low) on the second rising edge of CCLK after CON has been released high.
3. The appropriate Global and Fast Clock nets are enabled on the first rising edge of the associated Global or Fast Clock input signal after CON is released high. The nets are released high for glitchless operation.

Table 12. System Level Integration Timing Parameters @ 3.3V ± 10% Industrial/Commercial Range

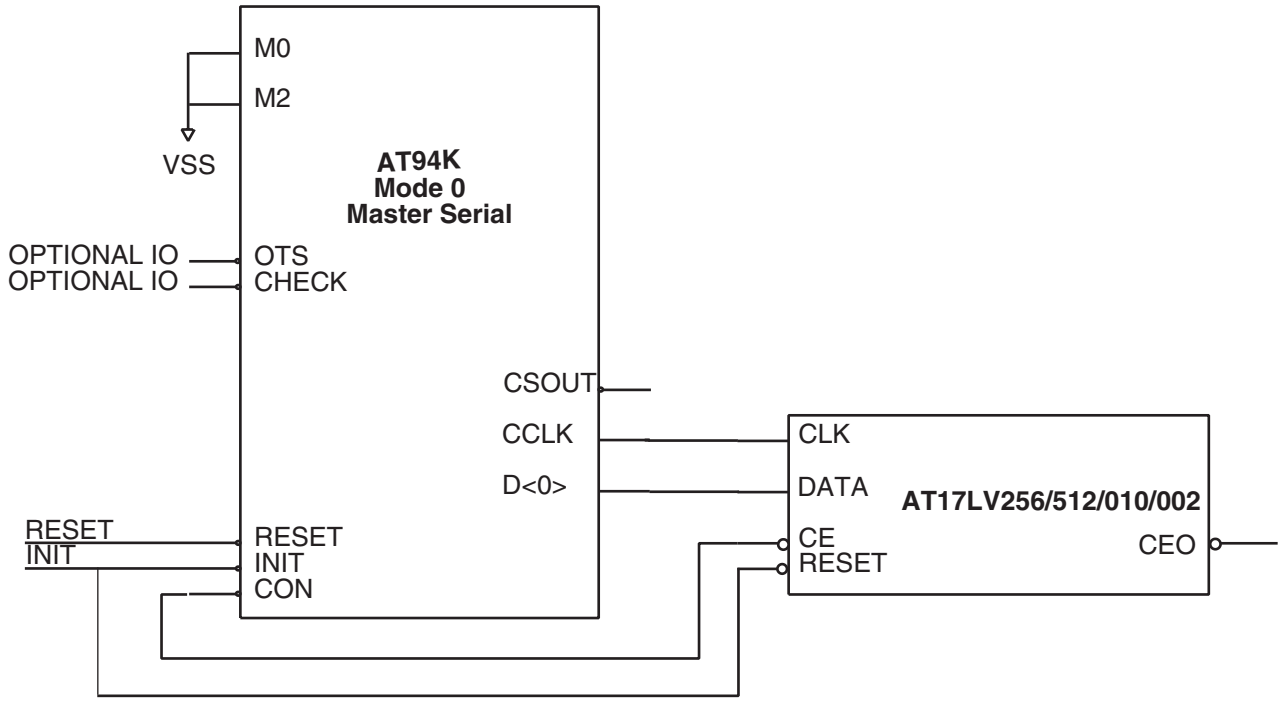
Parameter	Description	Min	Typ	Max	Units
t_{SCC}	Setup time for CON and CS* with respect to CCLK to initiate the start or end of configuration System Startup	6	10	16	ns
t_{DGSR}	Delay from falling edge of CON to a forced low on the Internal Global Set/Rest net	10	16	26	ns
t_{DCGSR}	Delay from rising edge of CCLK to the release of the Internal Global Set/Reset net to full user control	10	16	26	ns
t_{DCGTS}	Delay from rising edge of CCLK to the activation or deactivation of output drivers on User I/O	10	16	26	ns
t_{HGF}	Hold time for the rising edge of GCLK of FCLK with respect to the rising or falling edge of CON for activation or deactivation of one of the Global or Fast Clock nets	0	0	0	ns
t_{SGF}	Setup time for the rising edge of GCLK or FCLK with respect to the rising or falling edge of CON for activation or deactivation of one of the disabled Global or Fast Clock nets. Varies depending on the GCLK or FCLK chosen.	3		24	ns

Mode 0: Master Serial

Configuration Data Source:	Serial EEPROM
Dedicated Configuration Pins:	RESET, CON M_0, M_2, CCLK
Dual Use I/O:	D_0, INIT, LDC, HDC
Optional Dual Use I/O:	CSOUT, CHECK.OTS

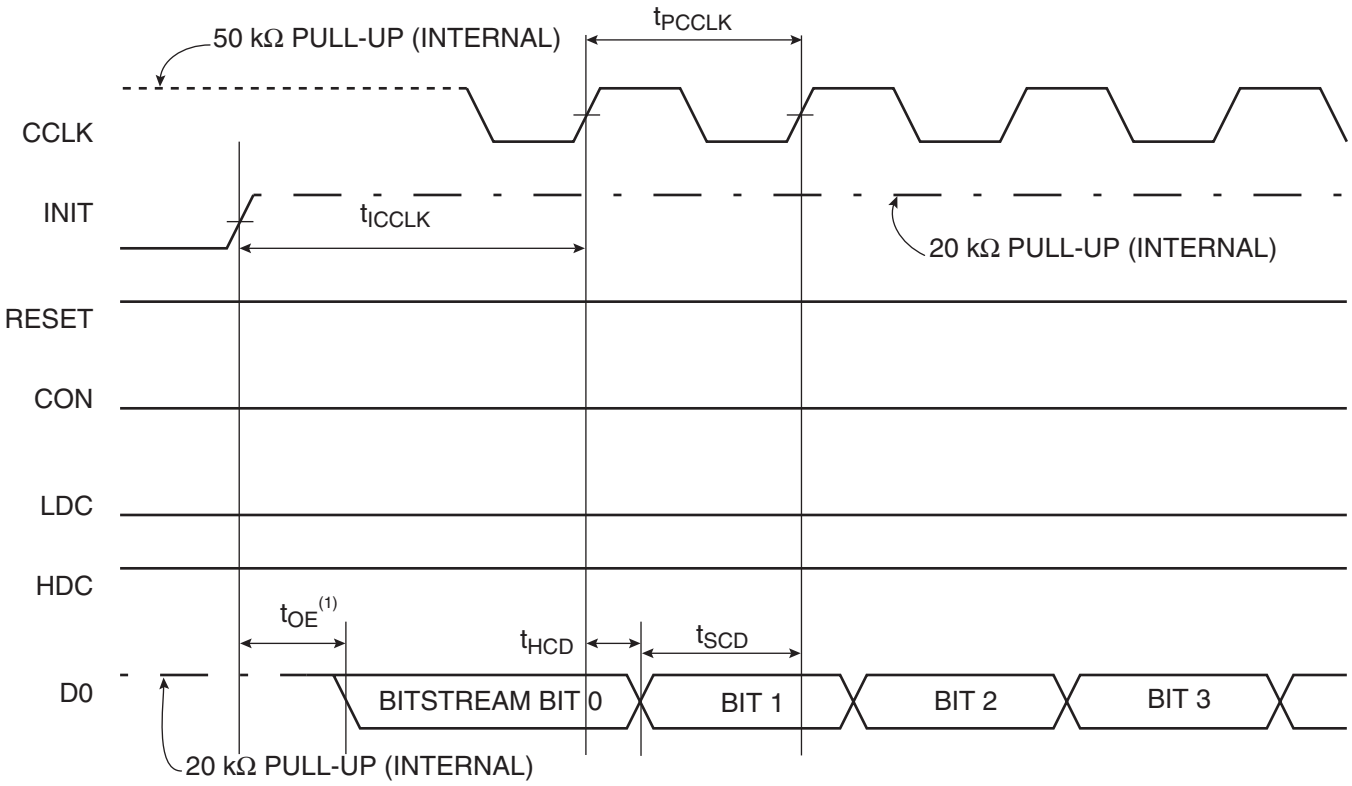
In Mode 0, CCLK is driven by the Master Serial AT94K FPSLIC into an Atmel Configurator that drives data out its DATA pin and into the D0 pin of the FPSLIC. Each CCLK increments the Configurator internal address counter and serial data is presented to the FPSLIC. Once the bitstream is completed, CON is released by the FPSLIC, indicating the device is completely ready for user operation. Configuration time depends on the frequency of the internal clock driving CCLK (approximately 1 MHz) and on the structure of the bitstream.

Figure 6. Standalone Configurator System Application



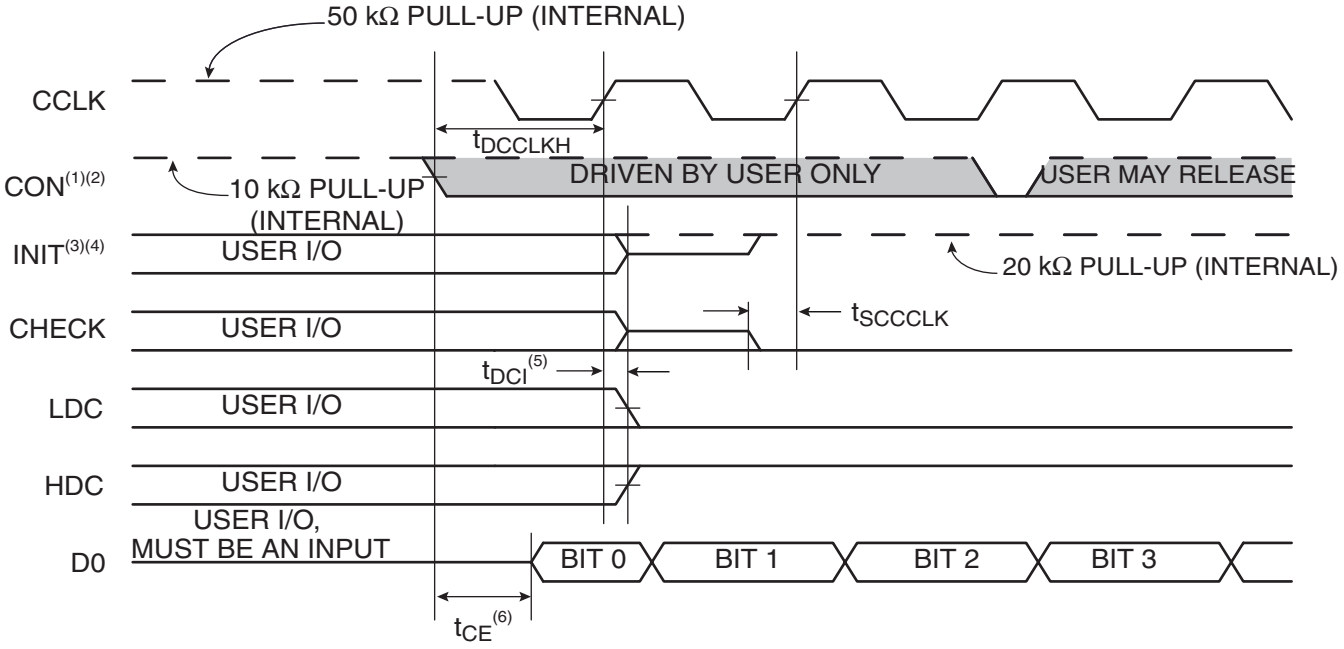
For the AT94K Series devices, the RESET or the INIT pin is tied to the Configurator OE/RESET pin, and CON is tied to the Configurator chip enable (CE). Figure 7 shows the timing of the configuration interface after power-on-reset or manual reset and at the start of download. Figure 8 shows the timing of the configuration interface after manually initiating a configuration download from the idle state (without reset). Figure 9 shows the timing of the configuration interface at the end of configuration download. Table 13 shows the configuration timing parameters for these timing diagrams.

Figure 7. Master Serial Start of Auto-Configuration Download



Note: 1. Parameter t_{OE} is taken from the AT17 Series datasheet.

Figure 8. Master Serial Start of Reconfiguration (without reset)



Notes:
1. Users must drive CON low for 3 rising edge of CCLK, and then should release.
2. During reconfiguration, when CON is driven low, the EEPROM begins driving immediately, but the FPSLIC will not claim the configuration interface until after the first rising edge of CCLK after CON goes low. The D_0 pin is a Dual Use I/O, but must remain an input in order for reconfiguration to operate properly. Failure to do so will cause contention between the Serial EEPROM and the FPSLIC when CON goes low.
3. INIT is an open drain pin during configuration downloads, so this pin must be driven only by an open drain driver. The pull-up value should be properly chosen to allow the pin to be pulled high prior to the first rising edge of CCLK. Failure to do so will not cause the part to abort the download, but may cause the user confusion if the FPSLIC does drive the pin low.
4. The EEPROM's OE/RESET pin is wired to the INIT pin of the FPSLIC in the example wiring shown in Figure 6. The internal counters of the EEPROM are reset by a low pulse on the OE/RESET pin. The user must either load both the reconfiguration bitstream and the auto-configuration bitstream sequentially into the EEPROM, or pulse the OE/RESET pin low to reset the EEPROM and then reload the auto-configuration bitstream.
5. For configuration interface inputs, t_{DCI} indicates the time for the user I/O to tri-state.
6. Parameter t_{CE} is taken from the AT17 Series datasheet.

Figure 9. Master Serial End of Configuration Download

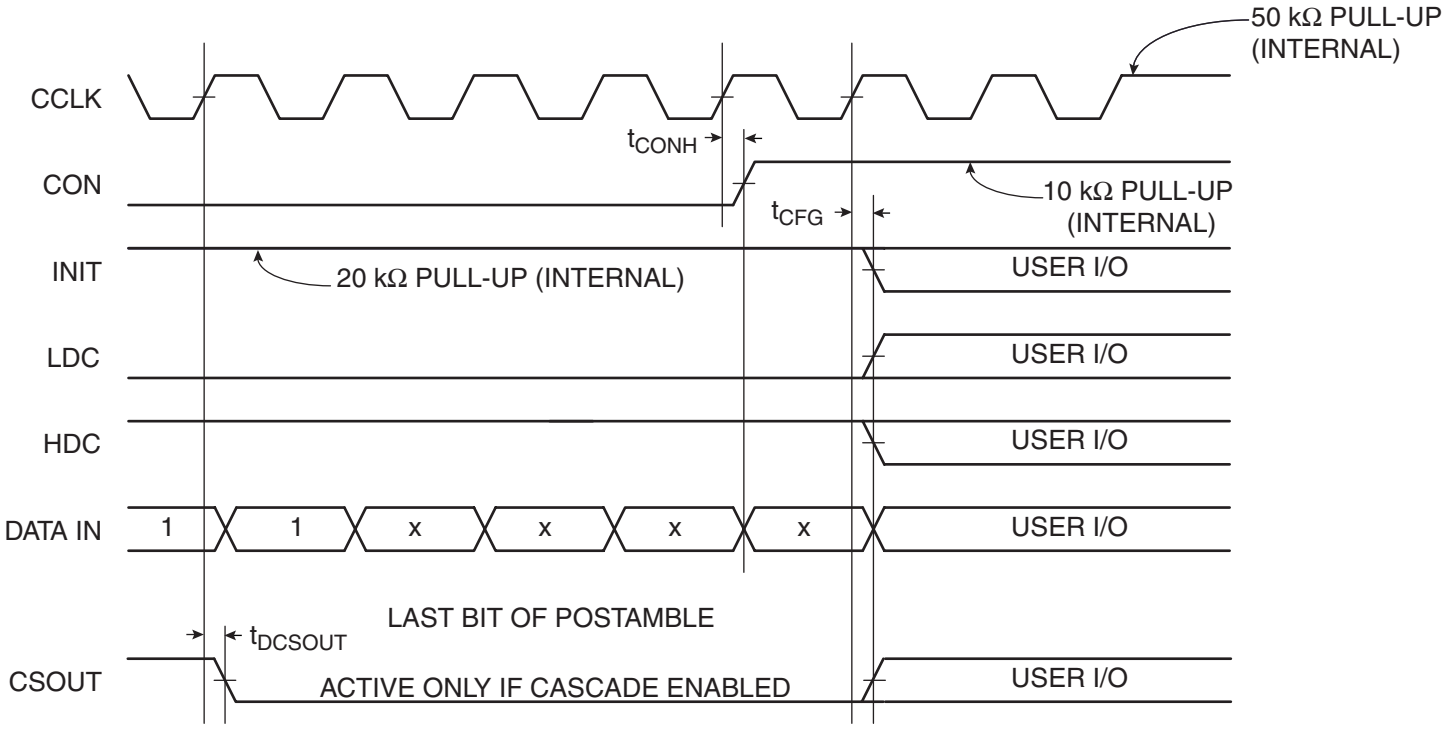


Table 13. Master Serial Configuration Timing Parameters @ 3.3V ± 10% Industrial/Commercial Range

Parameter	Description	Min	Typ	Max	Units
t_{PPCCLK}	Period of CCLK	0.6	1	1.6	µs
t_{ICCLK}	Delay from rising edge of INIT after reset to first rising edge of CCLK	1.8	3	4.8	ns
t_{SCD}	Setup time for DATA with respect to rising edge of CCLK	6	10	16	ns
t_{HCD}	Hold time for DATA with respect to rising edge of CCLK	0	0	0	ns
t_{DCCLKH}	Delay from falling edge of CON to first rising edge of CCLK to start recognition	0.6	1	1.6	µs
t_{SCCCLK}	Setup time for CHECK with respect to rising edge of CCLK at the start of a configuration download	6	10	16	ns
t_{DCI}	Delay from rising edge of CCLK to activation of configuration interface pins at the start of recognition	6	10	16	ns
t_{OE}	Delay from rising edge of OE/RESET of AT17 Series Configurator EEPROM to data valid on Data Out of Configurator. Data taken from the AT17 Series datasheet.			150	ns
t_{CE}	Delay from falling edge of CON to Data valid from AT17 Series Configurator EEPROM. Data taken from the AT17 Series datasheet.			45	ns
t_{CONH}	Delay from rising edge of CCLK to rising edge release of CON at the end of configuration. Timing is measured with a 50-pg load and a 2.7 kΩ pull-up resistor on CON. Actual time will depend on system loading of CON.		130		ns
t_{CFG}	Delay from rising edge of CCLK to the release of Dual Use pins to full user functionality	6	10	16	ns
t_{DCSOUT}	Delay from rising edge of CCLK to CSOUT active at end of configuration	6	10	16	ns

Mode 1: Slave Serial

Configuration Data Source:	Serial EEPROM, Microprocessor
Dedicated Configuration Pins:	RESET, CON M_0, M_2, CCLK
Dual Use I/O:	D_0, INIT, LDC, HDC
Optional Dual Use I/O:	CSOUT, CHECK, OTS

A Mode 1 Slave Serial device is usually configured in a system whereby data comes either from a serial EEPROM or from the data port of a microprocessor. Figure 10 shows a typical system application with a microprocessor. Figure 11 shows a typical system application with a Mode 1 device serial EEPROM in a cascade chain with a Mode 0 device as the master in the chain.

In Mode 1, CCLK is driven by an external device, most often either a microprocessor or a Master Serial FPSLIC, in cascade mode. Like the Master Serial device, serial data is driven into the D_0 pin of the FPSLIC. To begin configuration, CON must be driven low. Once the bitstream is completed, CON is released by the FPSLIC, indicating the device is completely ready for user operation. Configuration time depends on the frequency of the external clock driving CCLK. The maximum frequency in which a Mode 1 device can be downloaded is 25 MHz.

Figure 10. Standalone 1 Microprocessor System Application

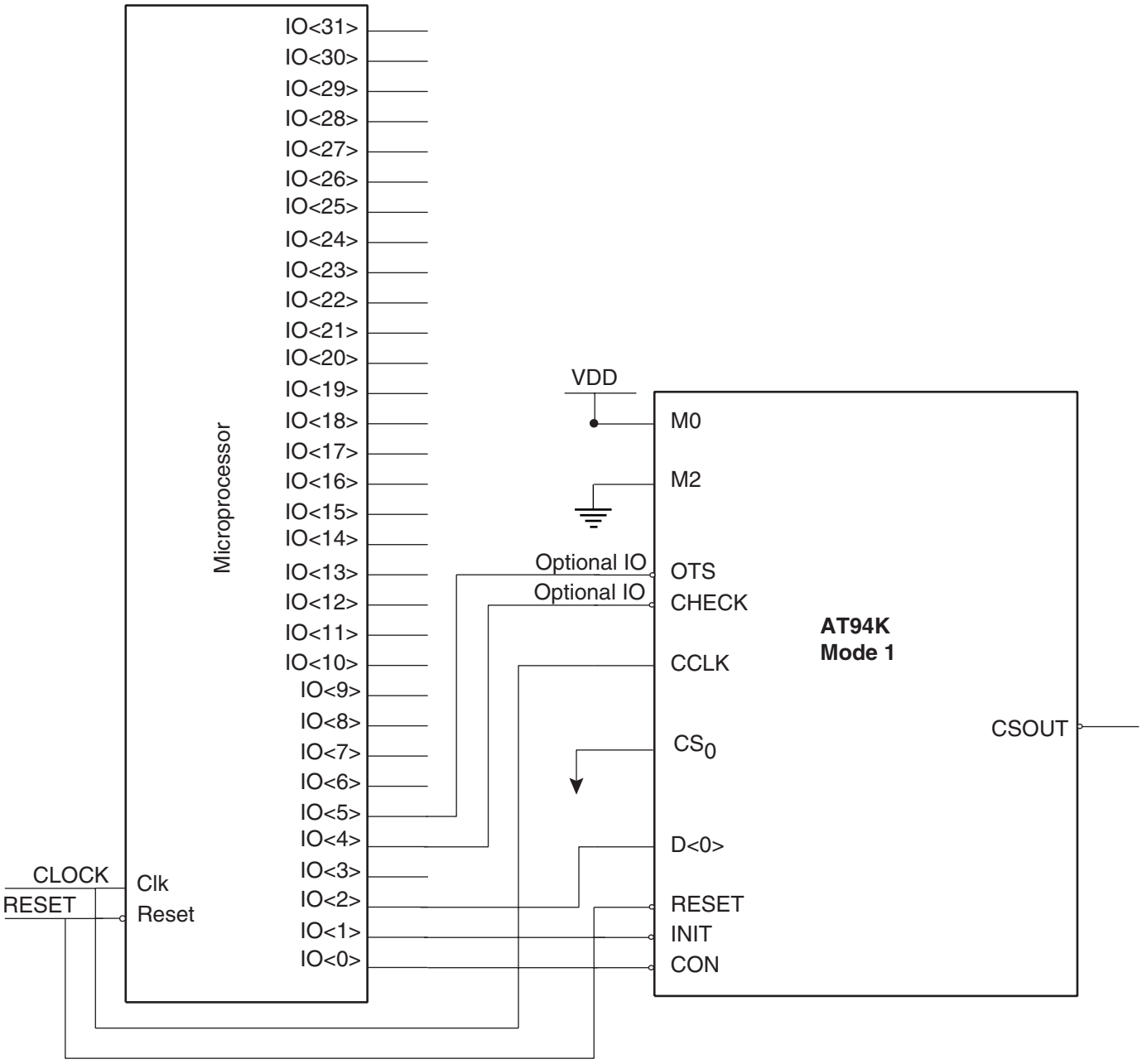
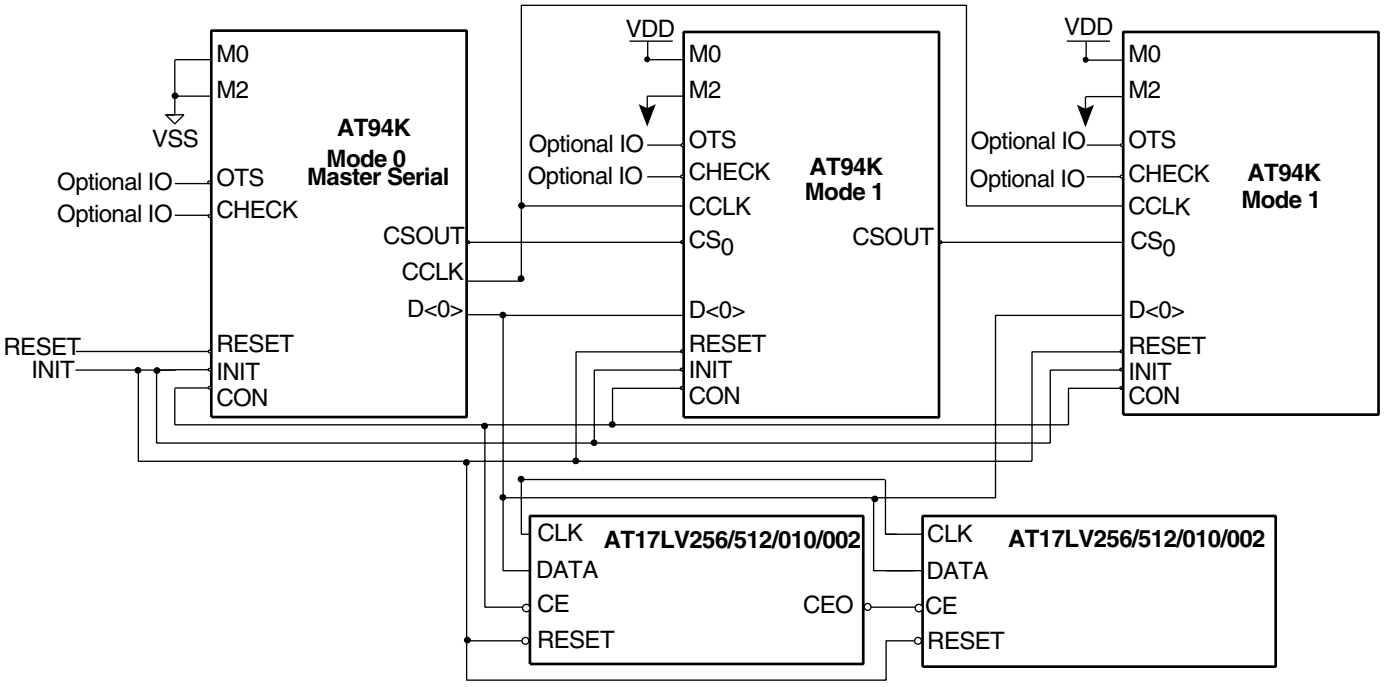


Figure 11. Cascade 0 11 Configurator System Application

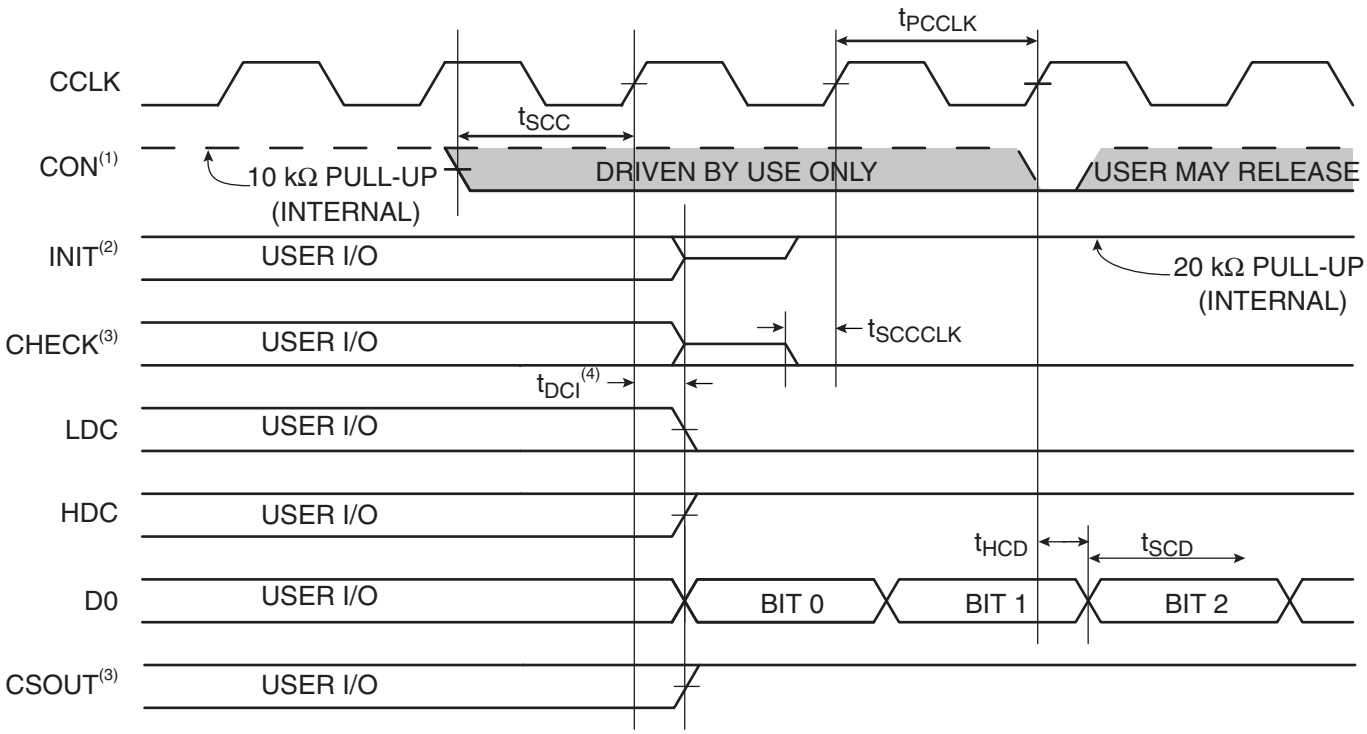


All D_0 inputs for the FPSLICs in the cascade chain are tied in parallel. The Master Serial device does not accept data intended for downstream devices and does not propagate it to the next device; instead, it simply passes a chip select downstream. Note that CSOUT of the upstream Master Serial device is connected to the CS_0 of the downstream device.

CS_0 is a Dual Use I/O pin is required as a chip select to enable the part to claim the configuration, so care must be taken by the user not to use the CS_0 pin in such a manner that the part may not be reconfigured. As an example, if the user programs CS_0 as an output driving high, then CS_0 cannot be lowered and the part will never reconfigure without first either powering down or manually resetting. It is recommended therefore that for Slave Serial mode, the user leaves CS_0 as an input.

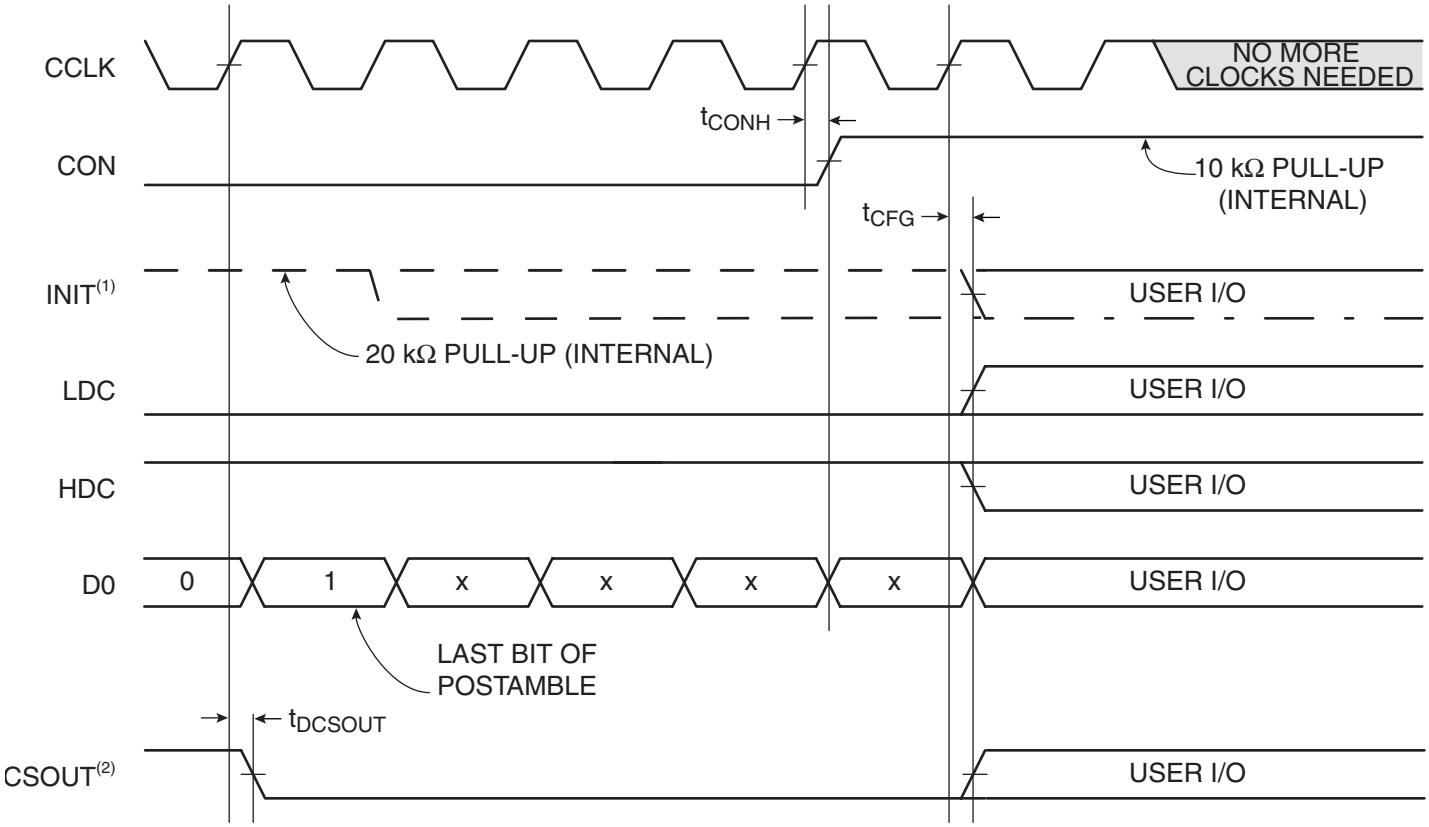
Figure 12 shows the timing of the configuration interface after manually initiating a configuration download from the idle state (without reset). Figure 13 shows the timing of the configuration interface at the end of configuration download. Figure 14 shows the timing of the configuration interface at the interface of the upstream and downstream devices in the cascade chain. Table 14 shows the configuration timing parameters pertaining to these timing diagrams.

Figure 12. Slave Serial Start of Configuration



Notes:
1. Users must drive CON low for 3 rising edges of CCLK, and then should release it.
2. INIT is an open drain pin during configuration downloads, this pin must be driven by only an open drain driver. The pull-up value should be properly chosen to allow the pin to be pulled high prior to the first rising edge of CCLK. Failure to do so will not cause the part to abort the download, but may cause the user confusion if the FPSLIC does drive the pin low.
3. The pins CSOUT and CHECK are claimed by the configuration interface only if enabled by the control register. Both are enabled by default after power-on-reset or manual reset.
4. For configuration interface inputs, t_{DCI} indicates the time for the user I/O to tri-state.

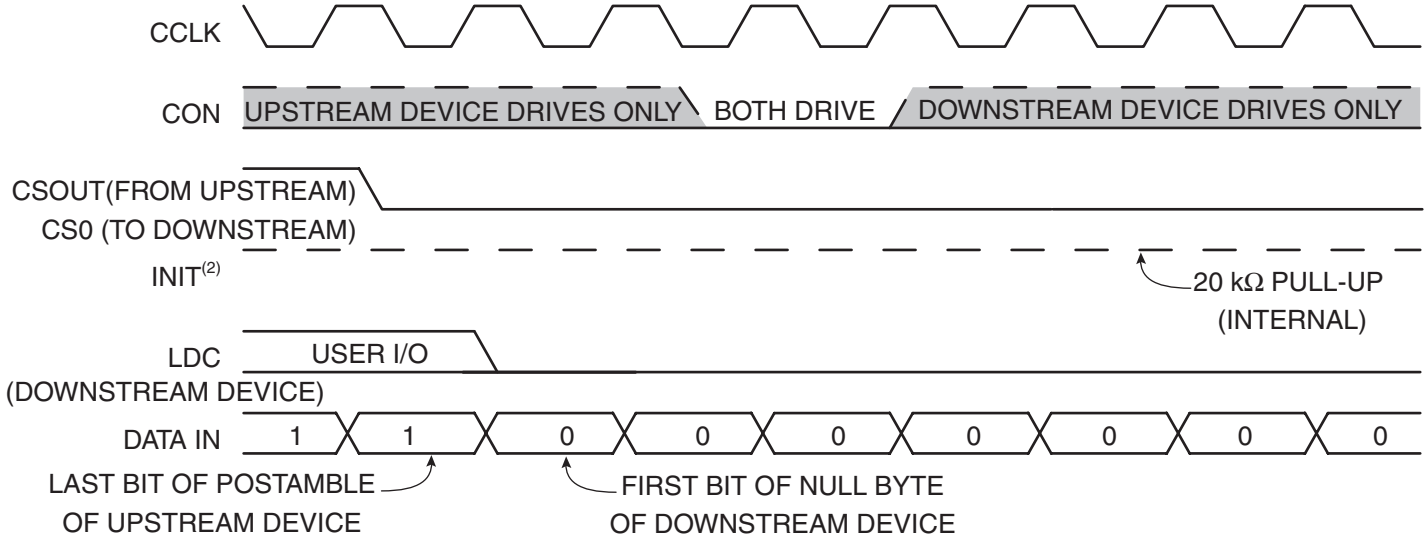
Figure 13. Slave Serial End of Configuration Download



Notes: 1. For a configuration bitstream error, INIT is driven low on the second rising edge after the bitstream error is detected. In the above example, the “0” in the second to last bit of the postamble is inserted to produce the error shown. The proper value is “1”. The error is shown for timing purposes only; under normal circumstances the bitstream download would terminate prematurely.

2. The pins CSOUT and CHECK are claimed by the configuration interface only if enabled by the control register. Both are enabled by default after power-on-reset or manual reset.

Figure 14. Serial Cascade Chain Interface Timing Diagram[1]



Notes: 1. Cascade bitstream is formed by simple concatenation of upstream and downstream bitstreams.
2. INIT of upstream and downstream devices are tied together for above example.

Table 14. Slave Serial Configuration Timing Parameters @ 3.3V ± 10% Industrial/Commercial Range

Parameter	Description	Min	Typ	Max	Units
t_{PPCCLK}	Period of CCLK for configuration downloads	30			ns
	Period of CCLK for configuration downloads with the check functions enabled	1000			ns
t_{SCC}	Setup time for CON and CSO with respect to rising edge of CCLK	6	10	16	ns
t_{SCD}	Setup time for data with respect to rising edge of CCLK	6	10	16	ns
t_{HCD}	Hold time for data with respect to rising edge of CCLK	0	0	0	ns
t_{SCCCLK}	Setup time for CHECK with respect to rising edge of CCLK at the start of a configuration download	6	10	16	ns
t_{DCI}	Delay from rising edge of CCLK to activation of configuration interface at the start of reconfiguration	6	10	16	ns
t_{DCSOUT}	Delay from rising edge of CCLK to falling edge of CSOUT by upstream device during a cascade configuration	6	10	16	ns
t_{CONH}	Delay from rising edge of CCLK to rising edge release of CON at the end of configuration. Timing is measured with a 50pf load and a 2.7 kΩ pull-up resistor on CON. Actual time will depend on system loading of CON.		130		ns
t_{CFG}	Delay from rising edge of CCLK to the release of dual use pins to full user functionality	6	10	16	ns

System Designer Bitstream Generation

The System Designer software is responsible for generating the file that configures the AT94K FPSLIC device. The Bitstream Dialog is shown in Figure 15, from this dialog the user can select the AVR and FPGA file used for configuration, and specify the output file. The tool does allow the capability of generating an FPGA only or AVR only bitstream for download. The Data RAM section also allows the user to configure the Data RAM within in the FPSLIC device. The user can provide the Data RAM configuration data in two formats, either Intel Hex or the Atmel Text Format (see Figure 16), details of which are provided in the online help. By clicking on the Control Register Settings tab, the user can configure the System Control Register Bits, previously mentioned in this document.

Figure 15. System Designer Bitstream Dialog

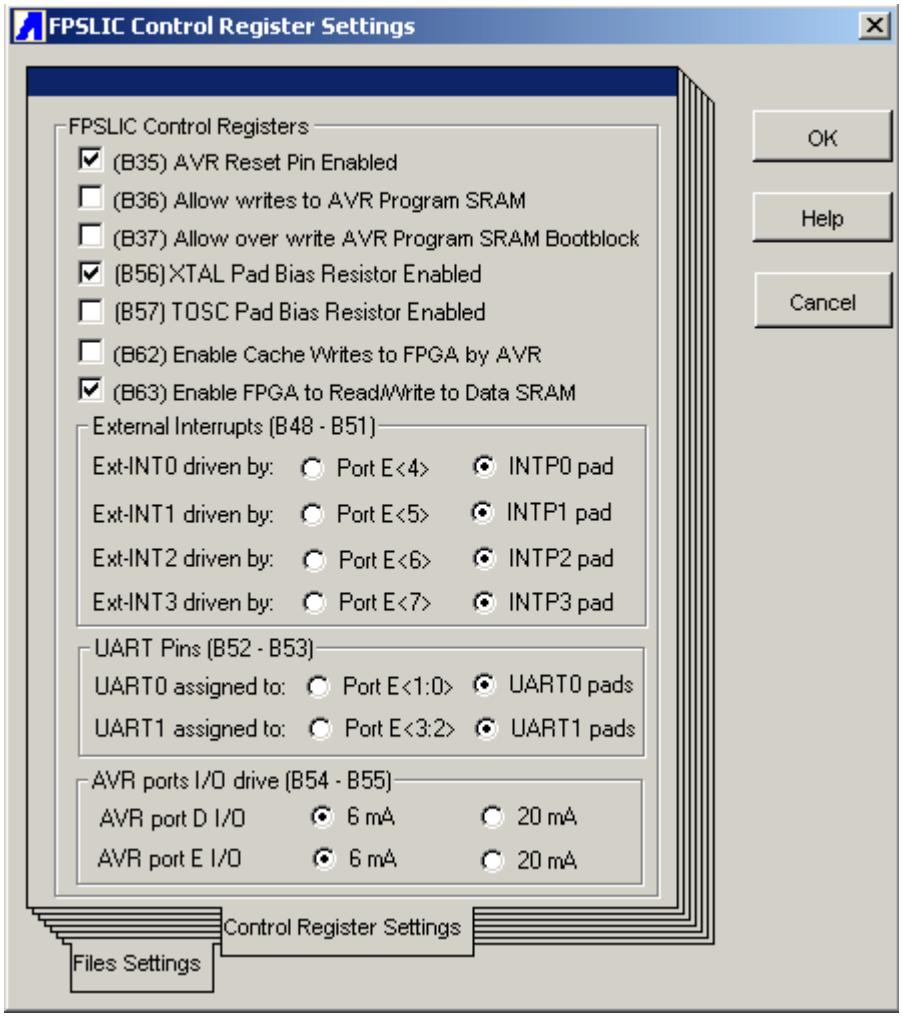
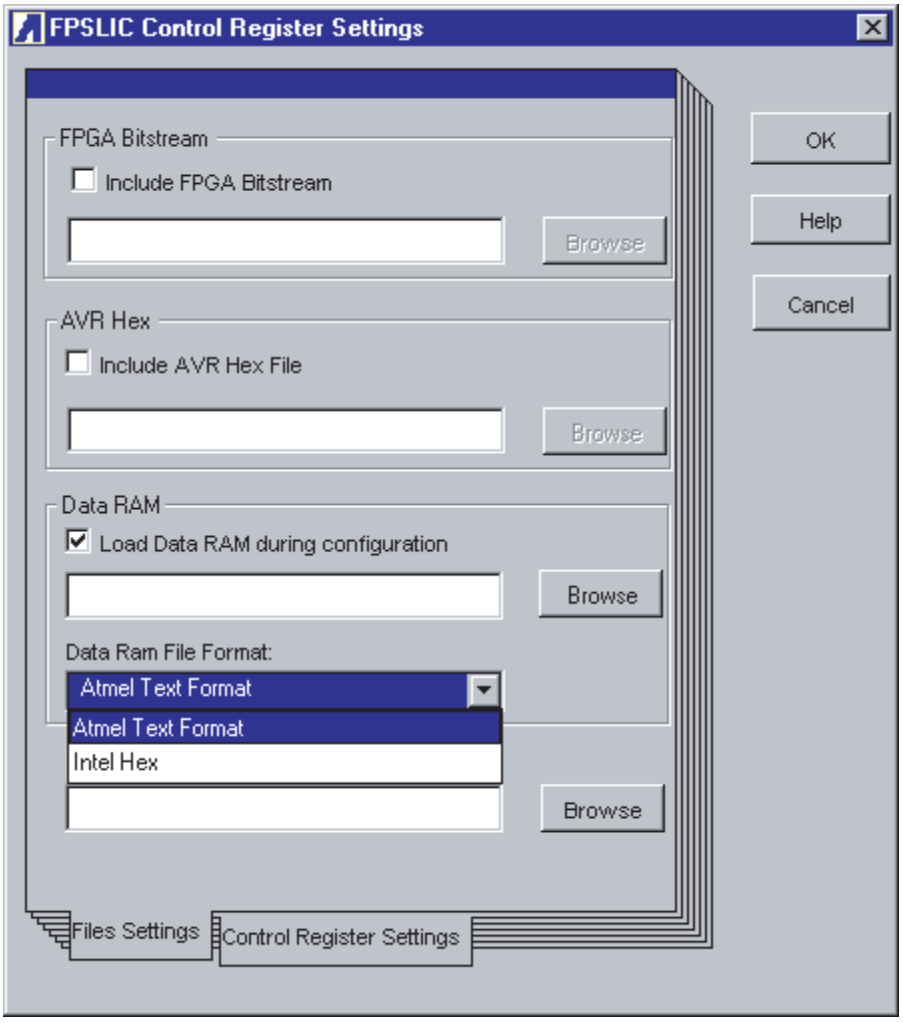


Figure 16. System Designer Bitstream Dialog – Data SRAM



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