

Implementing the test_bitstream design on the ATSTK94 FPSLIC Starter Kit

Features

- Test_bitstream design description
- Implemented on the ATSTK94 FPSLIC Starter Kit
- AVR counting from 1-255 displayed on LED tests AVR and LED functions
- FPGA outputting to alphanumeric tests FPGA programs outputs to alphanumeric
- Verifies ATSTK94 is functional

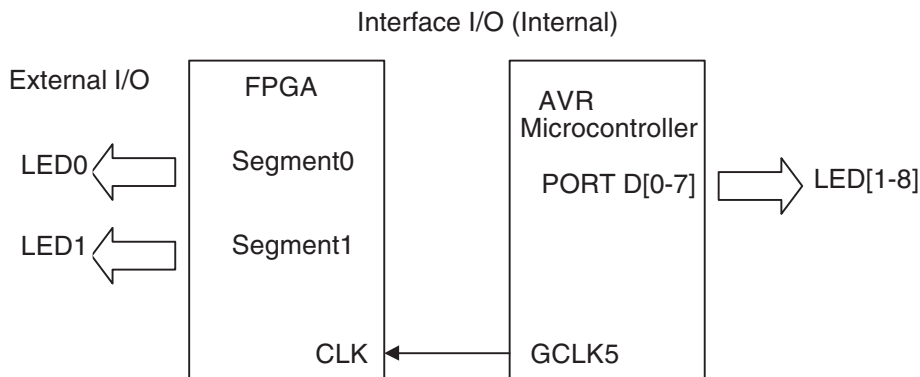
Introduction

The main purpose of the Test_bitstream design is to test the functions of the starter kit such as LEDs, the alphanumeric display, the clocks, etc. The design directory (CD:\examples\AT94K\ATSTK94 Designs\test_bitstream) contains vhd and C code for ImageCraft C compiler, an AVR™-FPGA interface constraints file, and a pin lock file for Figaro place and route tool.

Test_bitstream design description

The FPGA will start counting from 0-9 and A-Z displayed on the alphanumeric after power up, once it reaches Z the sequence it will restart. The AVR will increment from 1-255 and display on the LED, then it will restart. Figure 1 shows the test_bitstream design.

Figure 1. Functional Block Diagram of Test_bitstream design



**ATST94K Field
Programmable
System Level
Integrated
Circuit**

**Application
Note**



Design Implementation

Synthesize test_bitstream.vhd

Compile timer0Interrupt.c.

Implement the FPGA-AVR Interface as shown in Table 1.

Using fpslic_test_bitstream.pin to perform place and route of the PPGA position. This is done by using file import constraints after selecting Figaro and running open EDF.

Use the bitstream utilities to generate a combined bitstream file containing test_bitstream.bst, generated by the placement route step and the timer0Interrupt.hex file generated by the C compiler.

At this point you should use CPS provided with System Designer™ to program the starter kit. See the “Starter Kit user Guide” supplied with the Kit for more details.

After CPS reports successful completion you can switch from Program to Run. When you have programmed the starter kit, you should make sure that all the jumpers for the LED are set to the A position, meaning connected to the AVR PortD.

The test_bitstream design starts to run. The Alphanumeric will show a count from 0-9, A-Z and then repeat. The LED will increment from 1 to 255 and repeat.

Set JP19 to AVRRESET and press SW12 RESET; only AVR will be reset (LED1-8 are reset), the alphanumeric display should continue counting.

If the design does not run immediately you can set JP19 to RESET and use the RESET button SW12 to force a download from the Configurator to the FPSLIC device. Or you can power cycle the board.

Table 1. FPGA-AVR Interface Connection

FPGA Design Port Name		AVR Port Name	Tab Label (Left)
Clk12	<<Connect>>	GCLK5	FPGA Clocks

Troubleshooting

If the board does not perform as described:

1. Check that you switched from Prog to Run.
2. Power-cycle the board.
3. Check the jumper positions on the board.
4. Retry the programming with CPS.
5. Contact the FPSLIC Hotline as listed on the next page, or your local FAE.



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