Implementing AVR-like I/O Ports on the AT94K FPGA

Features

- **Full Source Code for Input and Output Ports**
- **Target Implementation Based on AT94K Starter Kit**

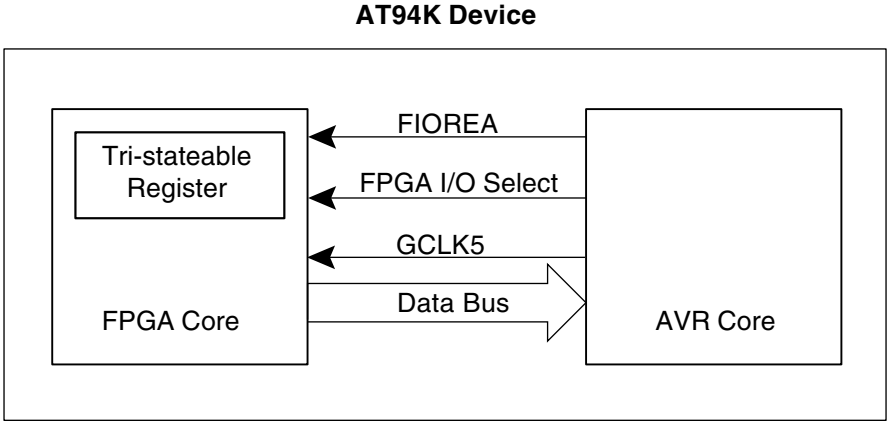
Introduction

The purpose of this application note is to explain how the FPGA Core of the AT94K Field Programmable System Level Integrated Circuit (FPSLIC™) device can be used to expand the peripherals of the AVR® Core, from two (Port D and Port E) to more peripherals. This application note uses the bi-directional data bus between the two cores of the FPSLIC device.

Input Port Description

The Input Port consists of an 8-bit register, which is enabled when the AVR I/O Read Enable (FIOREA) signal and the corresponding FPGA I/O Select are both active. For more information on the AVR I/O Read Enable, please refer to the “AT94K FPSLIC” datasheet, available on the Atmel web site (http://www.atmel.com/atmel/products/prod317.htm). See Figure 1 for further architectural information of the Input Port.

Figure 1. Input Port Block Diagram



Programmable SLI

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Application Note

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When implementing the Input Port in the FPGA Core using System Designer™, the following connections in the “AVR-FPGA Interface” dialog must be performed, see Table 1.

Table 1. Input Port AVR-FPGA Interface

Tab Label (Right)	Input Design Ports	AVR Port Name	State
AVRIOSelects	enable	IOSELA0	<<Connect>>
DataToAVR	dataout(0)	ADOUTA0	<<Connect>>
DataToAVR	dataout(1)	ADOUTA1	<<Connect>>
DataToAVR	dataout(2)	ADOUTA2	<<Connect>>
DataToAVR	dataout(3)	ADOUTA3	<<Connect>>
DataToAVR	dataout(4)	ADOUTA4	<<Connect>>
DataToAVR	dataout(5)	ADOUTA5	<<Connect>>
DataToAVR	dataout(6)	ADOUTA6	<<Connect>>
DataToAVR	dataout(7)	ADOUTA7	<<Connect>>
AVRControls	fiorea	FIOREA	<<Connect>>
FPGAClocks	clock	GCLK5	<<Connect>>

Finally, it is also necessary to make the following pin locks in Atmel’s Integrated Development System (IDS) for usage on the AT94K Starter Kit. The pin lock file is included with the design files. The LED Jumpers (Ln) on the ATSTK94 are set to “A” while the Switch Jumpers (SWn) are set to “F”, see Table 2.

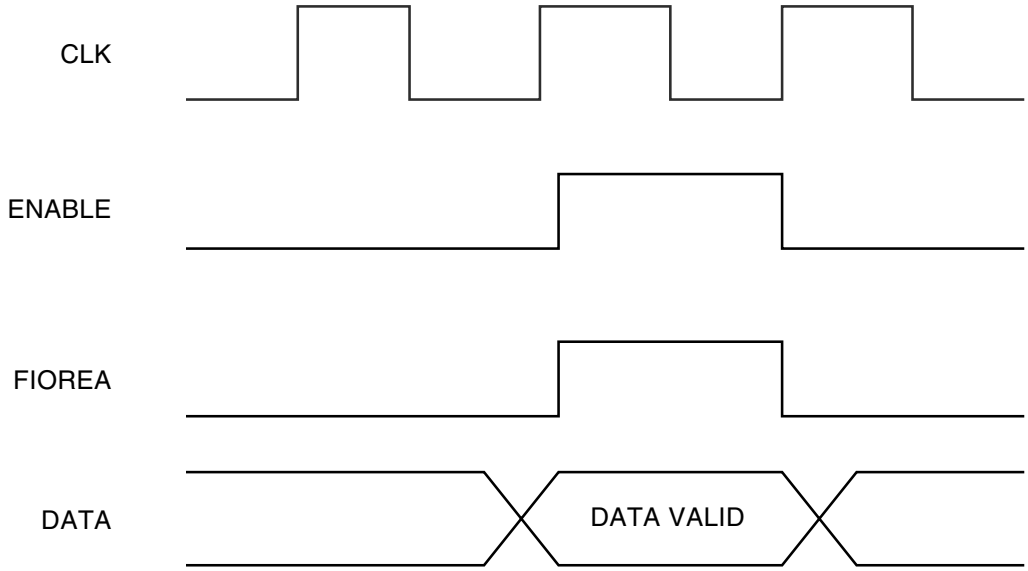
Table 2. Connect Switches to FPGA User I/O

Switch	Design I/O	Usable Pins
SW1	PINx(0)	202
SW2	PINx(1)	198
SW3	PINx(2)	192
SW4	PINx(3)	188
SW5	PINx(4)	180
SW6	PINx(5)	176
SW7	PINx(6)	172
SW8	PINx(7)	168

From the AVR core, the commands to access the Input Port implemented in the FPGA core depend upon the FPGA I/O Select Line used. For this application note it is assumed that FPGA I/O Select 0 has been used, but if another FPGA I/O Select Line is used, the XFIS1 and XFIS0 bits must be set correctly, see Figure 2. The following code snippet reads the FPGA-based Input Port and stores the value in Scratch Register r16.

```
ldi r16, ((0 << XFIS1) + (0 << XFIS0))
out FISCR, r16 ;Configure for Bi-directional Bus
in r16, FISUA ;Read Bi-directional Bus
```

Figure 2. Input Port Timing Diagram



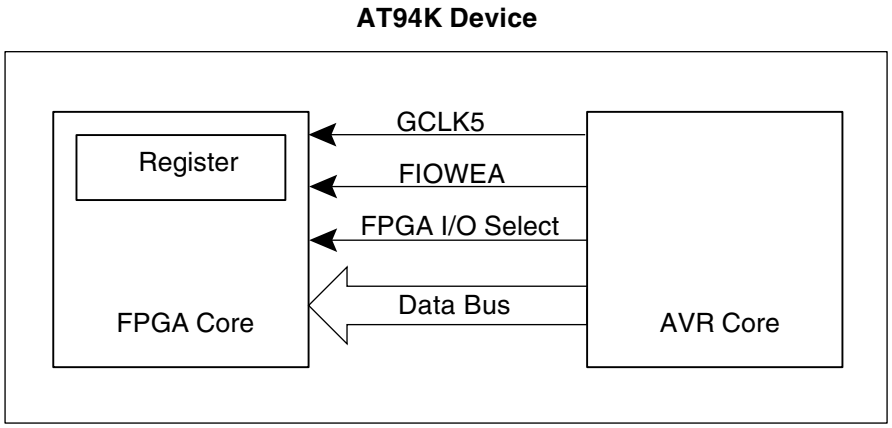
See below for the **portin.vhd** source file:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity PORTIN is
        port (
                CLOCK    : in    std_logic;
                ENABLE   : in    std_logic;
                FIOREA   : in    std_logic;
                PINx     : inout std_logic_vector(7 downto 0);
                DATAOUT  :   out std_logic_vector(7 downto 0)
              );
end PORTIN;


architecture BEHAV of PORTIN is
begin
        process (CLOCK, ENABLE, FIOREA, PINx)
        begin
                        if CLOCK'event and CLOCK = '0' then
                                if (ENABLE = '1' and FIOREA = '1') then
                                        DATAOUT <= PINx;
                                else
                                        PINx <= "ZZZZZZZZ";
                                        DATAOUT <= "ZZZZZZZZ";
                                end if;
                        end if;
        end process;
end BEHAV;
```

Output Port Description

The Output Port consists of an 8-bit register, which is enabled when the AVR I/O Write Enable (FIOWEA) signal, the corresponding FPGA I/O Select and the clock are all active. See Figure 3 for further architectural information of the Output Port.

Figure 3. Output Port Block Diagram



When implementing the Output Port in the FPGA Core using System Designer, perform the following connections in the “AVR-FPGA Interface” dialog, see Table 3.

Table 3. Output Port AVR-FPGA Interface

Tab Label (Left)	Input Design Ports	AVR Port Name	State
AVRIOSelects	enable	IOSELA0	<<Connect>>
DataFromAVR	datain(0)	ADINA0	<<Connect>>
DataFromAVR	datain(1)	ADINA1	<<Connect>>
DataFromAVR	datain(2)	ADINA2	<<Connect>>
DataFromAVR	datain(3)	ADINA3	<<Connect>>
DataFromAVR	datain(4)	ADINA4	<<Connect>>
DataFromAVR	datain(5)	ADINA5	<<Connect>>
DataFromAVR	datain(6)	ADINA6	<<Connect>>
DataFromAVR	datain(7)	ADINA7	<<Connect>>
AVRControls	fiowea	FIOWEA	<<Connect>>
FPGAClocks	clock	GCLK5	<<Connect>>

Finally, it is also necessary to perform the following pin locks in Atmel’s Integrated Development System (IDS) for usage on the AT94K Starter Kit. The pin lock file is included with the design files. The LED Jumpers (Ln) on the ATSTK94 are set to “F” while the Switch Jumpers (SWn) are set to “A”.

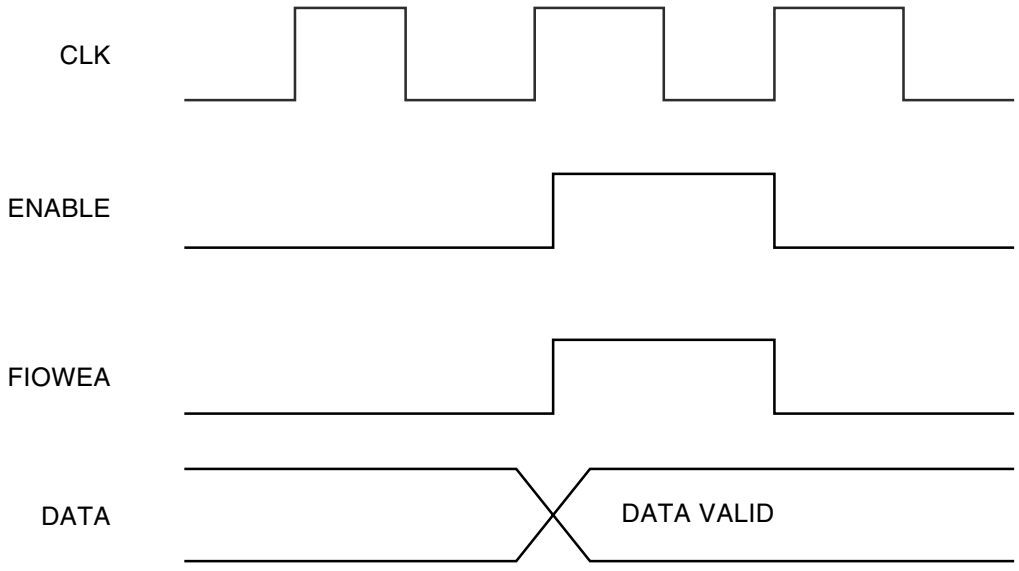
Table 4. Pin Lock

LED	FPGA Design Port Name	Usable Pins
L1	PORTx(0)	200
L2	PORTx(1)	196
L3	PORTx(2)	190
L4	PORTx(3)	186
L5	PORTx(4)	178
L6	PORTx(5)	174
L7	PORTx(6)	170
L8	PORTx(7)	166

From the AVR Core, the commands to access the Output Port implemented in the FPGA Core depend upon the FPGA I/O Select Line used. For this application note it is assumed that FPGA I/O Select 0 has been used, if another FPGA I/O Select Line is used the XFIS1 and XFIS0 bits must be set correctly, see Figure 4. The following code snippet writes the FPGA-based Output Port assuming the desired value is already present in Scratch Register r17.

```
ldi r16, ((0 << XFIS0) + (0 << XFIS1))
out FISCR, r16 ;Configure for Bi-Directional Bus
out FISUA, r17 ;Write to Bi-Directional Bus
```

Figure 4. Output Timing Diagram



See below for the portin.vhd source file:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

entity PORTOUT is
        port (
                CLOCK    :  in std_logic;
                LOAD     :  in std_logic;
                FIOWEA   :  in std_logic;
                DATAIN   :  in std_logic_vector(7 downto 0);
                PORTX    : out std_logic_vector(7 downto 0)
             );
end PORTOUT;


architecture BEHAV of PORTOUT is
begin
        process (CLOCK, LOAD, FIOWEA, DATAIN)
                variable PORTXINT : std_logic_vector(7 downto 0);
        begin
                if (rising_edge(CLOCK) and CLOCK'event) then
                        if (LOAD = '1' and FIOWEA = '1') then
                                PORTXINT := DATAIN;
                        end if;
                end if;

        PORTX <= PORTXINT;

        end process;
end BEHAV;
```

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