Implementing FreeRAM™ inside the FPGA or AT94K Series FPSLIC™ Using VHDL with IP Core Generator

Features

- **Generating the RAM Component Using the IDS Macro Generator**
- **Checking the Design with Simulation**
- **Creating a New Library**
- **Using IP Core Generator**
- **Switchable for AT40K, AT40KAL and AT94K**

Introduction

The purpose of this application note is to inform users of how to use VHDL with IP Core Generator to implement the FreeRAM inside the AT40K Field Programmable Gate Array (FPGA) for the AT94K Field Programmable System Level Integrated Circuit (FPSLIC).

testram.vhd and **testram_test_bench.vhd** are required for this example. These files can be found under **C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram**.

Note: This particular example describes how to implement a 32 x 4 asynchronous dual-port RAM cell in your VHDL file using LeonardoSpectrum™.

Programmable SLI

AT40K

AT40KAL

AT94K

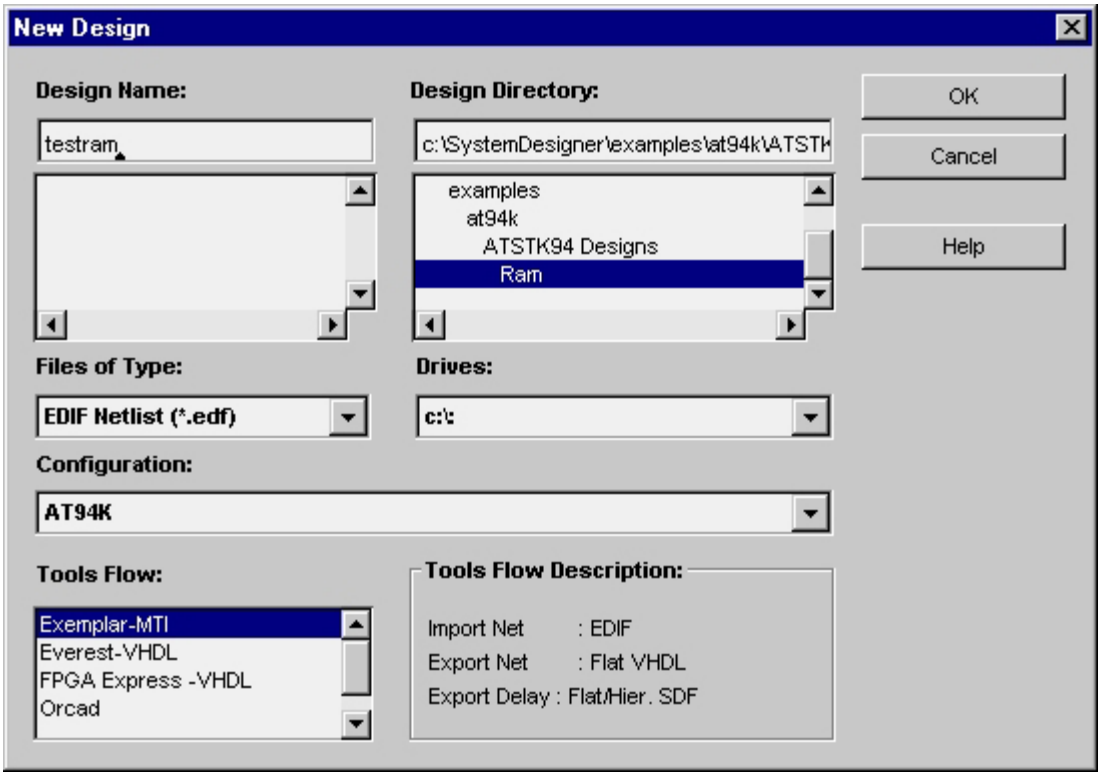
Application Note

Rev. 2298A–08/01

Generate the RAM Component Using the IDS Macro Generator

1. Open Figaro IDS.
2. Launch the design setup by pressing the  button.
3. Click on **New Design**.
4. Set up the design directory to: **C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram**.
5. Set up the configuration to **AT94K**, the design name to **testram** and the tool flow to **Exemplar**, see Figure 1.
6. Click on the **IP Core Generator**  button.
7. Select **Memory** from the bottom tab and **RAM-Dual Port** from the right hand tab.
8. Type 5 for Address Width and 4 for Width. (Address Width is 5 since 2^5 = 32)
9. Select **Asynchronous** for **RAM Type**, and type the macro name **dramasync**. Steps 6, 7, and 8 are shown in Figure 2.

Figure 1. New Design Window

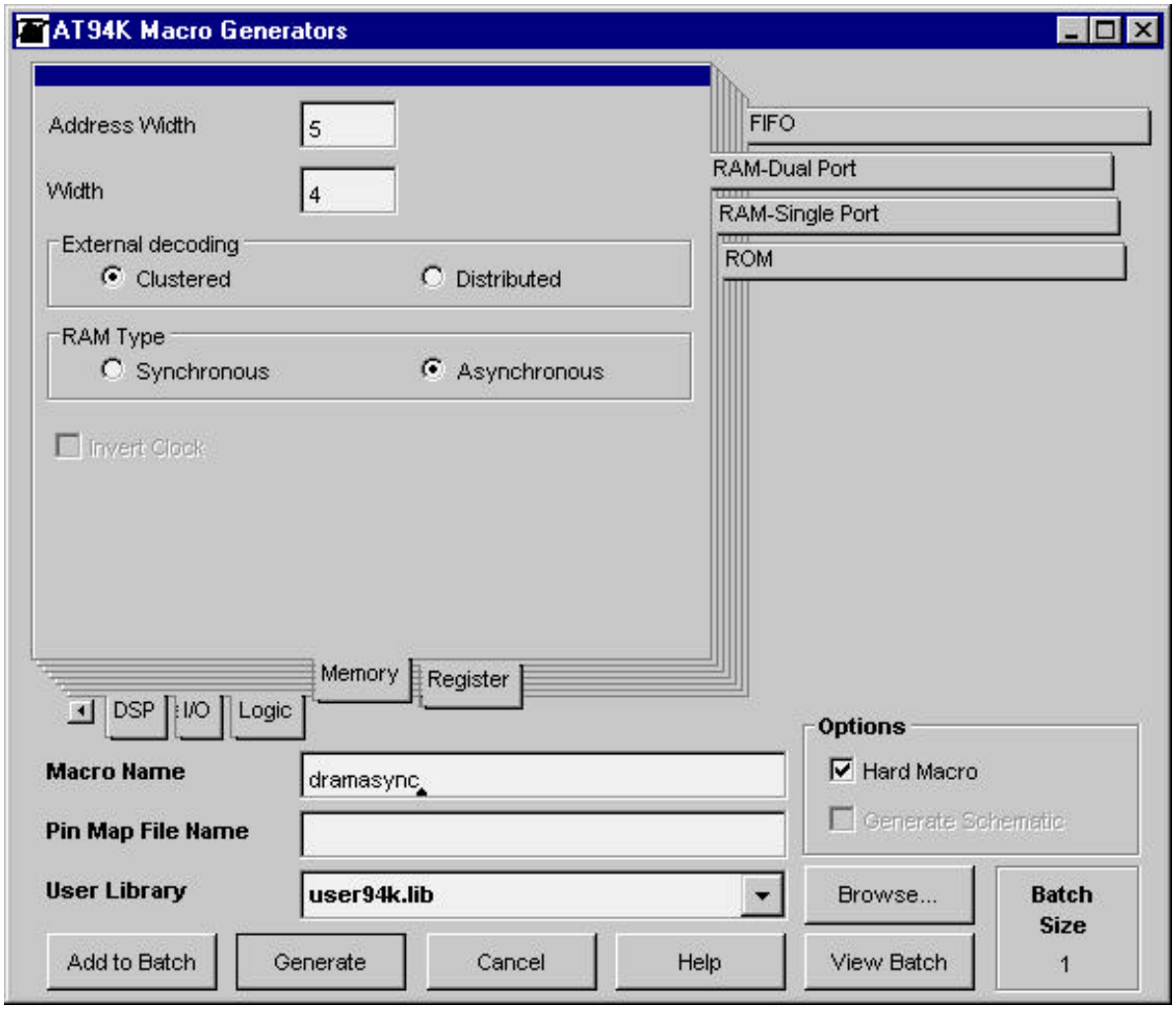


10. If there is no user library, click on the **Browse** button to add a new library.

    By default, IDS creates **user94k.lib**, if this file was not created, refer to the Create a New Library section on page 9 for more details.
11. Now click on the **Generate** button.

    After finishing generating this RAM block, IDS brings up a dialog box, see Figure 3.
12. Click on **OK** to dismiss the dialog box, and click on **CANCEL** to dismiss IP Core Generator.

Figure 2. AT94K IP Core Generator Window



Follow the steps below to instantiate this RAM component in the **testram.vhd** file. The **dramasync.vht** file is located under:
C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram\user94k\dramasync.

1. Copy the contents of **dramasync.vht** and paste them onto **testram.vhd** as shown below. Paste the words in *Italic,* and type manually the words in **bold**.

```
library ieee ;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

ENTITY testram IS

PORT (
        DATAIN : IN std_logic_vector(3 downto 0);
        DATAOUT : OUT std_logic_vector(3 downto 0);
        ADDRIN : IN std_logic_vector(4 downto 0);
        ADDOUT : OUT std_logic_vector(4 downto 0);
        WRITEN : IN std_logic;
```

```
        READN : IN std_logic
);

END testram ;
ARCHITECTURE behv OF testram IS

    Component dramasync
port (
        DOUT : out std_logic_vector(3 downto 0);
        AIN : in std_logic_vector(4 downto 0);
        AOUT : in std_logic_vector(4 downto 0);
        DIN : in std_logic_vector(3 downto 0);
        OEN : in std_logic;
        WEN : in std_logic
);
end component;

BEGIN

U1 : dramasync
             PORT MAP(
                     DOUT  => DATAOUT,
                     AIN   => ADDRIN,
                     AOUT  => ADDOUT,
                     DIN   => DATAIN,
                     OEN   => READN,
                     WEN   => WRITEN
             );

END behv;
```

Figure 3. AT94K IP Core Generator Statistics Window

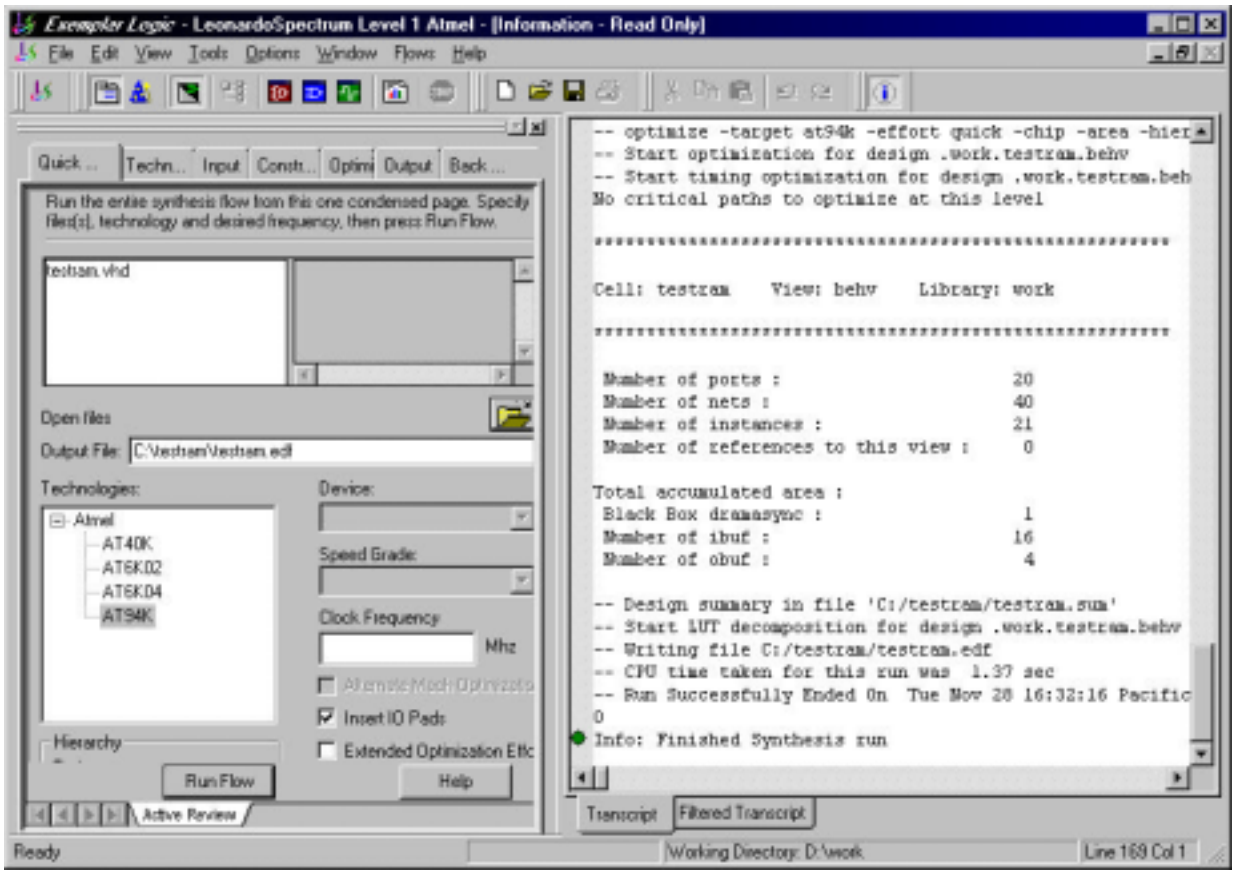
After modifying the **testram.vhd** file, the code needs to be synthesized to generate the "edf" file.

1. Click on the  button on the IDS window, the LeonardoSpectrum window appears.
2. Browse to select **testram.vhd** file.
3. Change the technology to **AT94K**, then click on **Run Flow**.

   If an error appears, check the **testram.vhd** file again.

   Figure 4 is an example of an LeonardoSpectrum window with all the correct setup.
4. After generating the **testram.edf** file, close LeonardoSpectrum and return to the IDS main window.

Figure 4. Exemplar Logic – LeonardoSpectrum Window

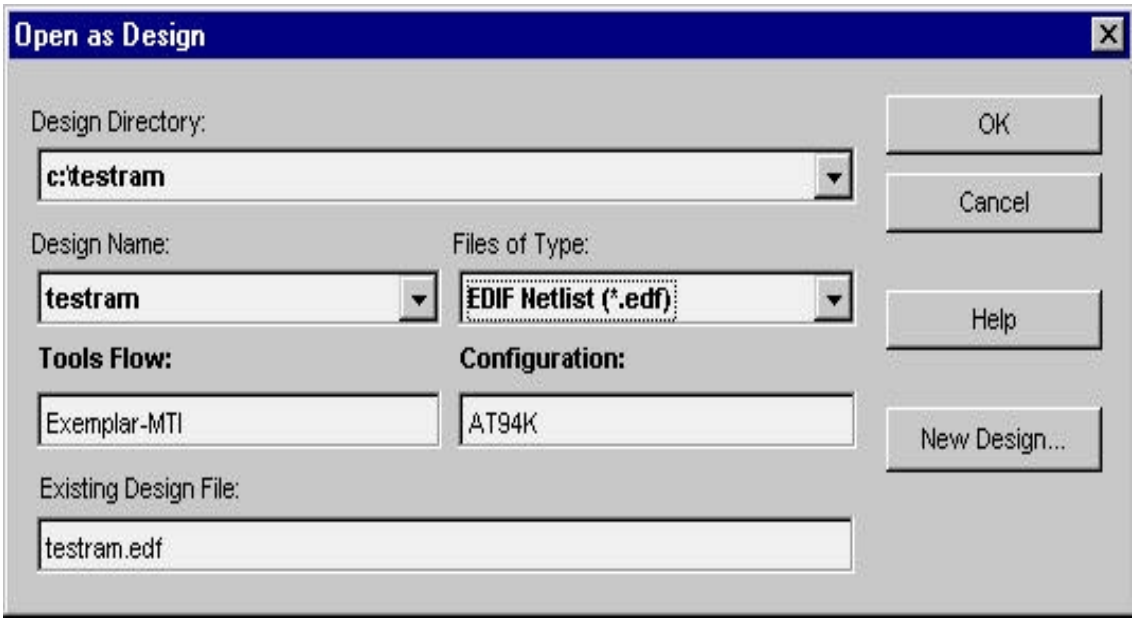


The step below imports the **testram.edf** file into IDS.

1. Click on the **Open** button and select **Design**.
2. Change the **Files of Type** box to ***.edf**; IDS automatically selects the **testram.edf** file, see Figure 5.
3. Click on **OK**. The design browser appears.
4. Click on the **Map** button. The mapping browser appears.
5. Click on the **Parts** button to select the part . This example uses **AT94K40-25DQC**.
6. Click on the **Compile** button.
7. Click on the  button. IDS will generate back-annotated vhdl and test bench files for simulation purposes.

   The vhdl files are located under:
   C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram\figba

Figure 5. Open a Design Window

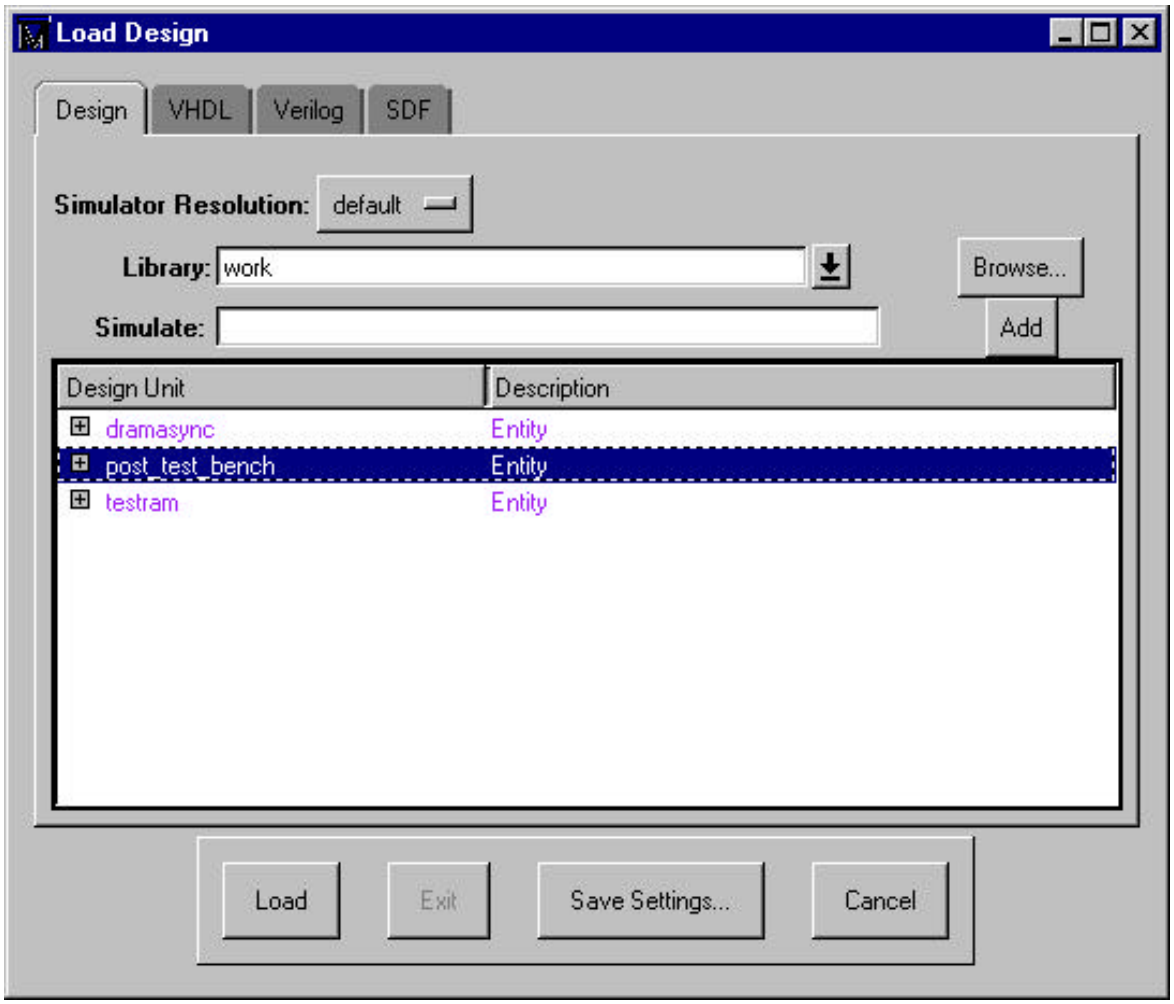


Check the Design with Simulation

To check the design with simulation, copy:
C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram\testram_test_bench.vhd to **C:\SystemDesigner\examples\at94k\ATSTK94 Designs\Ram\figba\testram_test_bench.vhd**.

1. Open the **ModelSim** window.
2. Click on **File > Change directory**.
3. Browse to the **C:\System Designer\examples\at94k\ATSTK94 Designs\Ram\figba** directory and click on **OPEN**.
4. To setup the ModelSim library, on the window, type the following commands:
   - vlib work
   - vmap work ./work
5. Click on **Design > Compile**
6. Select **dramasync.vhd** and click on **Compile**.
7. Select **testram.vhd** and click on **Compile**.
8. Select **testram_test_bench.vhd** and click on **Compile**.
9. Click on **Done** to dismiss the dialog.
10. Go to **Design > Load New Design**.
11. Select **post_test_bench** and click on **Load**, see Figure 6.
12. Go back to the ModelSim window and type the following command:
    - Add wave –r /*
    - Run –all
13. Let it run for 50 microseconds
14. Go to the wave window and click the  button.

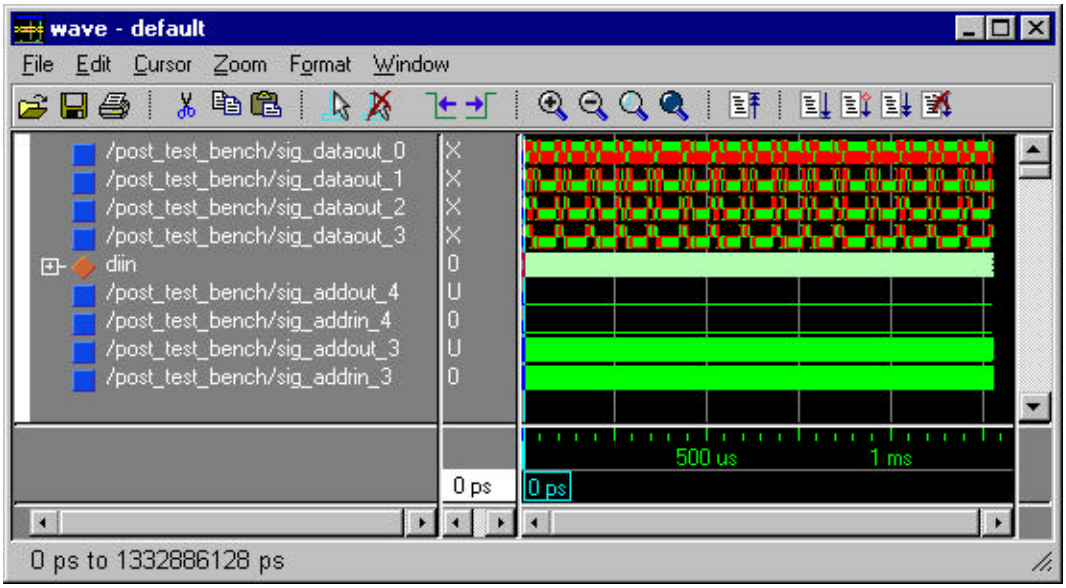
Figure 6. Load Design Window



15. A waveform similar to the one shown in Figure 7 appears.
16. Check the results.

Note: This design has loaded values 0000 to 1111 to memory locations 00000 to 01111 respectively. Later it will read back from those memory locations. The signal READN is asserted for 100 ns and de-asserted for 100 ns, some undefined states in between the DATAOUT will be visible.

Figure 7. Wave Window



Create a New Library

Follow the steps below to set up a new user library:

1. Click on **Library** on IDS main window.
2. Select **Library Setup**, see Figure 8.
3. Click on **Add Before**.
4. Select the directory, type the library name and then click on **OK**, see Figure 9 on page 10.
5. Click on **OK** to dismiss the **Library Setup**.

Figure 8. Library Setup Window

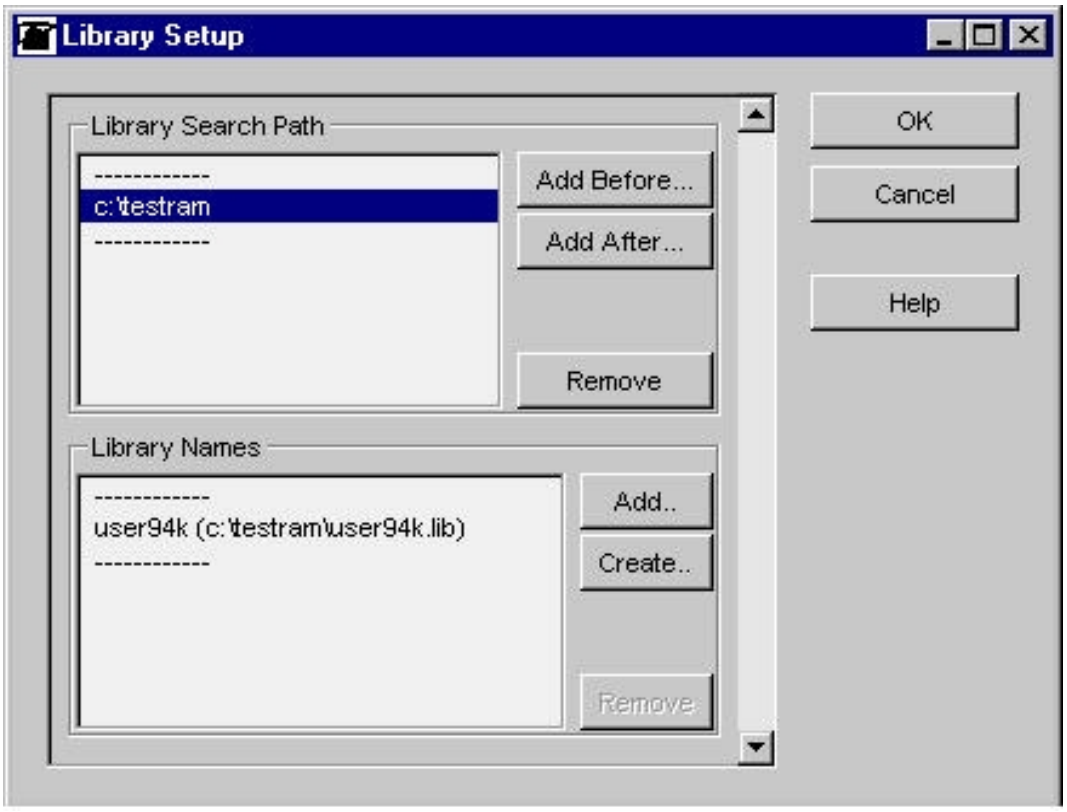
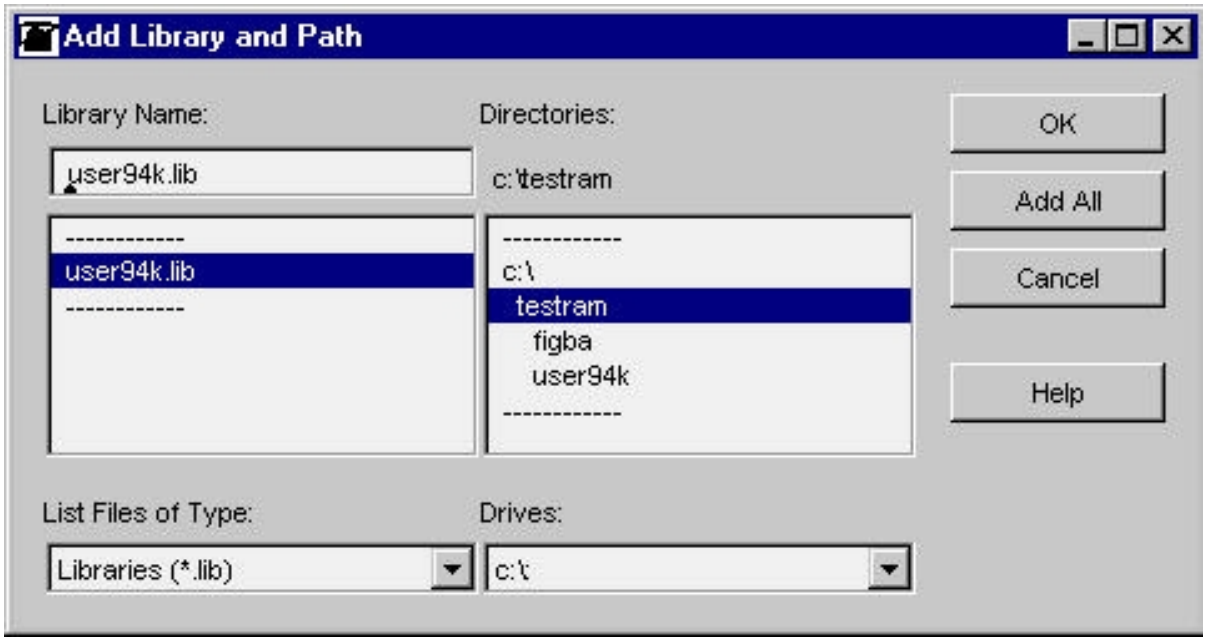


Figure 9. Add Library Window



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