AT94K, Field Programmable System Level Integration Chip (FPSLIC), Interrupt Macros

Features

- **Global Interrupt**
- **External Interrupts**
- **FPGA Interrupts**
- **Timer Interrupts**
- **UART Interrupts**
- **2-wire Serial Interrupt**

Introduction

Atmel's AT94K Interrupt Macros are provided to familiarize and assist customers in programming the AVR® microcontroller as part of the AT94K FPSLIC™ product offering. The Interrupt Macros provide customers with a simple method for enabling and disabling the interrupts on the AT94K device.

Application

Atmel's AT94K Interrupt Macros are implemented in such a way that they can be used interchangeably between embedded C compilers, assuming that the proper register definitions have been made in the ioat94k.h file. The ioat94k.h file must declare the register names corresponding to the names found in the Atmel AT94K device datasheet. These macros have been extensively tested with ImageCraft ICCAVR v6.13a and above and IAR Systems IAR Embedded Workbench AT90S v1.50B/WIN compilers.

A software macro is essentially a name with a corresponding text string, which is commonly referred to as the body. When a macro is called, the compiler replaces the name with the corresponding macro body.

To use the AT94K Interrupt Macros, the user must include the at94k_interrupts.h file available from the AT94K area of Atmel's web site. Furthermore, all of the AT94K Interrupt Macros require a parameter, either ENABLE or DISABLE. The AT94K Interrupt Macros are used in the following manner:

- To Enable an Interrupt: INTERRUPT_MACRO_NAME(ENABLE);
- To Disable an Interrupt: INTERRUPT_MACRO_NAME(DISABLE);

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Application Note

Rev. 2285A–04/01

Description

Macro Name: GLOBAL_INT

Description: The Global Interrupt Enable bit must be enabled (one) for any of the interrupts to be enabled. The individual interrupt enable control is then preformed in separate control registers. If the Global Interrupt Enable bit is disabled (zero) none of the interrupts are enabled independent of the individual interrupt settings.

Macro Name: EXTERNAL_INTS

Description: When enabled, all four of the External Interrupt Enable bits are enabled (one), and the Global Interrupt is enabled, all of the External Pin Interrupts are enabled. The External Interrupts are always low level triggered.

Macro Name: EXTERNAL_INT3

EXTERNAL_INT2

EXTERNAL_INT1

EXTERNAL_INT0

Description: When enabled, the corresponding External Interrupt Enable bit is enabled (one), and the Global Interrupt is enabled, the corresponding External Pin Interrupt is enabled. The External Interrupts are always low level triggered.

Macro Name: FPGA_INT_ALL

Description: When enabled, all sixteen of the FPGA Interrupt Mask bits are enabled (one), and the Global Interrupt is enabled, all sixteen of the FPGA Interrupts are enabled. The corresponding interrupt handling vector is executed when the given FPGA Interrupt Flag bit is set (one) by a low signal on the associated interrupt line from the FPGA.

Macro Name: FPGA_INT_MASKD

FPGA_INT_MASKC

FPGA_INT_MASKB

FPGA_INT_MASKA

Description: When enabled, all four of the FPGA Interrupt Mask bits in the specified bank are enabled (one), and the Global Interrupt is enabled, all four of the FPGA Interrupts are enabled. The corresponding interrupt handling vector is executed when the given FPGA Interrupt Flag bit is set (one) by a low signal on the associated interrupt line from the FPGA.

Macro Name: FPGA_INT_MASK15

FPGA_INT_MASK14

FPGA_INT_MASK13

FPGA_INT_MASK12

FPGA_INT_MASK11

FPGA_INT_MASK10

FPGA_INT_MASK9

FPGA_INT_MASK8

FPGA_INT_MASK7

FPGA_INT_MASK6

FPGA_INT_MASK5

FPGA_INT_MASK4

FPGA_INT_MASK3

FPGA_INT_MASK2

FPGA_INT_MASK1

FPGA_INT_MASK0

Description: When enabled, the FPGA Interrupt Mask bit is enabled (one), and the Global Interrupt is enabled, the FPGA Interrupt is enabled. The corresponding interrupt handling vector is executed when the given FPGA Interrupt Flag bit is set (one) by a low signal on the associated interrupt line from the FPGA.

Macro Name: TIMER_INTS

Description: When enabled (one) and the Global Interrupt is enabled, all of the Timer/Counter Interrupts are enabled, when disabled (zero) all of the Timer/Counter Interrupts are disabled. See individual interrupt calls for descriptions.

Macro Name: TIMER1_INPUT_CAPTURE_INT

Description: When the Input Capture bit is enabled (one) and the Global Interrupt is enabled, the Timer/Counter1 Input Capture Event Interrupt is enabled. The corresponding interrupt handler is executed if a capture-triggering event occurs.

Macro Name: TIMER2_OVERFLOW_INT

TIMER1_OVERFLOW_INT

TIMER0_OVERFLOW_INT

Description: When the Overflow Interrupt bit is enabled (one) and the Global Interrupt is enabled, the corresponding Timer/Counter Overflow Interrupt is enabled. The corresponding interrupt handler is executed if an overflow in the corresponding Timer/Counter occurs.

Macro Name: TIMER2_OUTPUT_COMPARE_INT

TIMER1_OUTPUT_COMPAREA_INT

TIMER1_OUTPUT_COMPAREB_INT

TIMER0_OUTPUT_COMPARE_INT

Description: When the Output Compare bit is enabled (one) and the Global Interrupt is enabled, the corresponding Timer/Counter Compare Match Interrupt is enabled. The corresponding interrupt handler is executed if a compare match occurs.

Macro Name: UART1_INTS

UART0_INTS

Description: When enabled (one) and the Global Interrupt is enabled, all of the corresponding UART Interrupts are enabled, when disabled (zero) all of the UART Interrupts are disabled. See individual interrupt calls for descriptions.

Macro Name: UART1_DATA_REG_EMPTY

UART0_DATA_REG_EMPTY

Description: When enabled (one), a setting of the UDREn, where n is the corresponding UART either 0 or 1, bit in UCSRnA will cause the UART Data Register Empty Interrupt routine to be executed provided that the global interrupt is enabled.

Macro Name: UART1_RX_COMPLETE_INT

UART0_RX_COMPLETE_INT

Description: When enabled (one), a setting of the RXCn, where n is the corresponding UART either 0 or 1, bit in UCSRnA will cause the Receive Complete Interrupt routine to be executed provided that the global interrupt is enabled.

Macro Name: UART1_TX_COMPLETE_INT

UART0_TX_COMPLETE_INT

Description: When enabled (one), a setting of the TXCn, where n is the corresponding UART either 0 or 1, bit in UCSRnA will cause the Transmit Complete Interrupt routine to be executed provided that the global interrupt is enabled.

Macro Name: SERIAL_INT

Description: When enabled (one) and the Global Interrupt is enabled, the 2-wire Serial Interrupt will be activated for as long as the TWINT flag is HIGH.

Sample Code Snippet

The following sample C code demonstrates the usage of the AT94K Interrupt Macros. As previously stated, the corresponding AT94K Interrupt is either enabled or disabled based on the parameter passed to the macro.

```
/* Including AT94K Interrupts Macro File */
#include "at94k_interrupts.h"
/* Function Prototype */
void reset(void);
/* Main Entry Point of Software */
void main(void)
{
        reset();
        for(;;){}
}
/* Function Definition */
void reset()
{
    /* Disabling External, Timer, FPGA, UART1, and Serial Interrupts */
    EXTERNAL_INTS(DISABLE);
    TIMER_INTS(DISABLE);
    FPGA_INT_ALL(DISABLE);
    UART1_INT(DISABLE);
    SERIAL_INT(DISABLE);
/* Enabling FPGA0, UART0, and Global Interrupts */
    FPGA_INT0_MASK(ENABLE);
    UART0_INT(ENABLE);
    GLOBAL_INT(ENABLE);
}
/* FPGA_INT0 and UART0 ISR Definitions */
```

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Atmel Smart Card ICs
Scottish Enterprise Technology Park
East Kilbride, Scotland G75 0QR
TEL (44) 1355-357-000
FAX (44) 1355-242-743

Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex
France
TEL (33) 4-7658-3000
FAX (33) 4-7658-3480

Atmel FPSLIC Hotline
(408) 436-4119

Atmel FPSLIC e-mail
fpslic@atmel.com

FAQ
Available on web site

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

2285A–04/01/xM