AT40K Training Series

Software Requirements

IDS6.0 Basic Installation - The tutorial assumes a default install of C:\ATMEL.
If you installed the software elsewhere look for the examples directory in that location.
Patch Level4 installed if upgrading an existing system to Synplicity.

VHDL LAB 1 – Basic Synplicity Design Flow andgate.vhd

First of all a Design setup is performed in IDS. Then Synplicity is invoked from IDS. Synplicity Generates an EDF file, which is Opened in IDS and compiled.

VHDL LAB 2 – Synplicity with Automatic Macro Instantiation adder.vhd

Synplicity has the ability to recognize a number of standard Atmel Macro Generators from your source VHDL. These components will be synthesized through Synplicity as black boxes, which will then be replaced with Atmel Macro Generators when the EDF file is Opened in IDS.

VHDL LAB 3 – Synplicity with Macro Generators ramdesign.vhd

IDS has the ability to generate many Macros, using the Macro Generator utility. These can then be instantiated in your VHDL code and synthesized as black boxes in Synplicity.
The advantages of these components is that it allows you to generate standard functions without defining them all in VHDL and it generates an optimized layout for each component. Timing and power calculations are also generated for each Macro.

Verilog LAB 1 – Basic Synplicity Design Flow andgate.v

First of all a Design setup is performed in IDS. Then Synplicity is invoked from IDS. Synplicity Generates an EDF file, which is Opened in IDS and compiled.

Verilog LAB 2 – Synplicity with Automatic Macro Instantiation adder.v

Synplicity has the ability to recognize a number of standard Atmel Macro Generators from your source Verilog. These components will be synthesized through Synplicity as black boxes, which will then be replaced with Atmel Macro Generators when the EDF file is Opened in IDS.

LAB 1 – Basic Synplicity Design Flow

Design Setup

New Design

Design Name = andgate
Design Directory = C:\atmel\examples\at40k\synplicity\vhdl
Configuration = AT40K
Tools Flow = Synplicity - VHDL

Press OK - to close New Design Dialog
Press OK – to Complete Design Setup

Synplicity Synthesis

Press P to create a new Project

Add andgate.vhd as the design source

Press the Run Button. This will Synthesize your design and generate an EDF file. It will also generate a report file showing utilization and Timing.
Use View Log button to see this.

Return to the IDS window.

Open EDF File
You will be asked if you want to open as Design or Macro. Select Design
The Open as Design dialog should show the values we entered in Design Setup.
Check that Files of Type is set to EDIF and that the Existing Design File entry shows andgate.edf
Press OK

Provides additional packing of logic into LUTs.

Select the first part in the list. Press Add. A part is added to the Parts Window.
Press OK

This will partition, place and route the design and export a Bitstream.
After Compile has completed, Compile button goes green
Open a compile window to view the results.
Window -> New Compile Window.

Andgate.vhd

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY andgate IS
      PORT (      A, B  : IN std_logic;
                  Q     : OUT std_logic
            );
END andgate;

ARCHITECTURE behaviour of andgate IS

BEGIN

Q <= A AND B;

END behaviour;
```

LAB 2 – Synplicity with Automatic Macro Instantiation

Using the Existing Design Setup

Synplicity Synthesis

Press P to create a new Project – Save Previous Project.

Add adder.vhd as the design source

Press the Run Button. This will Synthesize your design and generate an EDF file. It will also generate a report file showing utilization and Timing.

Return to the IDS window.

Open EDF File
You will be asked if you want to open as Design or Macro. Select Design
Press New Design in the Design Setup Dialog. Select adder.edf from the file list.
Press OK.
Check that Files of Type is set to EDIF and that the Existing Design File entry shows adder.edf
Press OK.

The Macro Generator Dialog should open.
You will need to add a User Library -> Press Browse... -> Add Before....
Type Library Name User.lib and press OK to return to Macro Dialog.
When asked to update Cache library say yes.

Generates an 8 bit adder Macro

Add a Part

Window > New Compile Window - Or Double Click on the part in the Parts Assembler

Adder.vhd

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;
USE ieee.std_logic_unsigned.all;

ENTITY adder IS

     PORT (    A, B      : IN std_logic_vector(7 downto 0);
               Q         : OUT std_logic_vector(7 downto 0)
          );
END adder;

ARCHITECTURE behaviour of adder IS

BEGIN

Q <= A + B;

END behaviour;
```

LAB 3 – Synplicity with Macro Generators

Using the Existing Design Setup

Macro Generators

Category Tab	Memory
Macro Tab	RAM - Dual Port
Address Width	6
Width	16
External Decoding	Clustered
RAM Type	Synchronous
Macro Name	ramblock

A Macro Statistics dialog should appear if the generator ran successfully
Press Cancel to close the Macro Dialog

Copy adder.vhd and open in a text editor. Wordpad is best for this.
Use adder.vhd as a template for the ramdesign file on the next page.
You can cut and paste the component definition from the file ramblock.vht in c:/atmel/examples/synplicity/at40k/vhdl/user/ramblock

When complete do Save As ramdesign.vhd.
Make sure it is in the c:/atmel/examples/at40k/synplicity/vhdl directory.

Synplicity Synthesis

Press P to create a new Project

Add ramdesign.vhd as the design source

Press the Run Button.

Open EDF File
New Design
Design Name = ramdesign
Press OK

Ramdesign.vhd

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all;

ENTITY ramdesign IS
        PORT (      dataout     :  out std_logic_vector(15 downto 0);
                    address     :  in std_logic_vector(5 downto 0);
                    clock       :  in std_logic;
                    datain      :  in std_logic_vector(15 downto 0);
                    read        :  in std_logic;
                    write       :  in std_logic
        );
END ramdesign;

ARCHITECTURE behaviour of ramdesign IS

        -- Taken from file c:\atmel\examples\synplicity\at40k\vhdl\ramblock\ramblock.vht

  component ramblock
port (
    DOUT :  out std_logic_vector(15 downto 0);
    AIN :  in std_logic_vector(5 downto 0);
    AOUT :  in std_logic_vector(5 downto 0);
    CLK :  in std_logic;
    DIN :  in std_logic_vector(15 downto 0);
    OEN :  in std_logic;
    WEN :  in std_logic
   );
  end component;

BEGIN
U1 : ramblock
        PORT MAP (
                                DOUT => dataout,
                                AIN => address,
                                AOUT => address,
                                CLK => clock,
                                DIN => datain,
                                OEN => read,
                                WEN => write
        );
END behaviour;
```

LAB 1 – Basic Synplicity Design Flow

Design Setup

New Design

Design Name = andgate
Design Directory = C:\atmel\examples\at40k\synplicity\verilog
Configuration = AT40K
Tools Flow = Synplicity - Verilog

Press OK - to close New Design Dialog
Press OK – to Complete Design Setup

Synplicity Synthesis

Press P to create a new Project

Add andgate.v as the design source

Press the Run Button. This will Synthesize your design and generate an EDF file. It will also generate a report file showing utilization and Timing.
Use View Log button to see this.

Return to the IDS window.

Open EDF File
You will be asked if you want to open as Design or Macro. Select Design
The Open as Design dialog should show the values we entered in Design Setup.
Check that Files of Type is set to EDIF and that the Existing Design File entry shows andgate.edf
Press OK

Provides additional packing of logic into LUTs.

Select the first part in the list. Press Add. A part is added to the Parts Window.
Press OK

This will partition, place and route the design and export a Bitstream.
After Compile has completed, Compile button goes green
Open a compile window to view the results.
Window -> New Compile Window.

Andgate.v

```
module moduleName (a, b, q ) ;
      input             a, b;
      output      q;

      assign q = a && b;
endmodule
```

Adder.v

```
module moduleName (a, b, q ) ;

      input       [7:0]       a, b;
      output      [7:0]       q;

      assign q = a + b;

endmodule
```

LAB 2 – Synplicity with Automatic Macro Instantiation

Using the Existing Design Setup

Synplicity Synthesis

Press P to create a new Project – Save Previous Project.

Add adder.vhd as the design source

Press the Run Button. This will Synthesize your design and generate an EDF file. It will also generate a report file showing utilization and Timing.

Return to the IDS window.

Open EDF File
You will be asked if you want to open as Design or Macro. Select Design
Press New Design in the Design Setup Dialog. Select adder.edf from the file list.
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