Integrated Development System
Macro Library 1

June 2002

How the Databook is Organized

This databook describes the more than 200 macros available for use with the Atmel AT6000 Series of field-programmable gate arrays (FPGAs). The databook is split into two binders: Macro Library Volume 1 and Macro Library Volume 2. Volume 1 contains the set of "Functions" macros and Volume 2 contains the set of "Input/Output" macros. Macros are listed alphabetically in each volume. Symbol, schematic and truth table are provided for each macro, as are pin-to-pin propagation delays and setup and hold times. Each macro is available in two speeds: fast (-2) and slow (-4). Volume 2 also contains the physical layout drawing for each macro. Refer to Volume 2 for additional information.

Macro Naming Conventions

Macro names are abbreviated descriptions of the macro's function. For example, a 3-input XOR gate is named XO3. The "XO" refers to the XOR function, the "3" refers to the number of inputs. An "L" at the end of a name indicates active low, while an "H" denotes active high. For example, DC24L is a 2-to-4 decoder with active low outputs. Macros ending in "ST" can be cascaded to create functions of arbitrary bit length. For example, two SRPST (Shift Register with Parallel Load Stage) macros can be cascaded together to create a 3-bit shift register. Input and output macros use their own set of abbreviations:

I	=	Input
O	=	Output
B	=	Bidirectional
TTL	=	TTL on input
CMS	=	CMOS on input
P	=	Pull-up on pad
D	=	Full drive
S	=	Standard slew rate
F	=	Fast slew rate

OC = Open collector
EN = Tri-state enable (z)

For example, BTTLDF is a fast, bidirectional TTL input with full drive output.

Truth Table Conventions

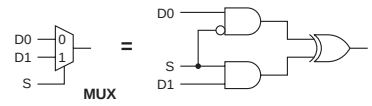
The following conventions are used in the Truth Tables:
z = Tri-State
w1 = Weak logical "one"

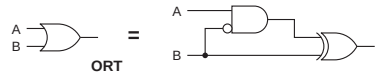
Transient Output Characteristics

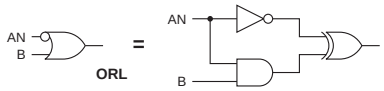
The functions, MUX, ORT and ORL are single cells configured with a two-input XOR gate and display transient output characteristics.

The output of MUX may not be constant when the select signal is toggled, even if the D0 and D1 signals are both the same value. The value of ORT may not be a constant 1, even if the A input is a constant 1 and the B input is toggling. Similarly, the output of ORL may not be a constant 1, even if the B input is a constant 1 and the A input is toggling.

Macros that use MUX, ORT and ORL as building blocks also display transient output characteristics. An asterisk appears in the Viewlogic symbol of these macros.

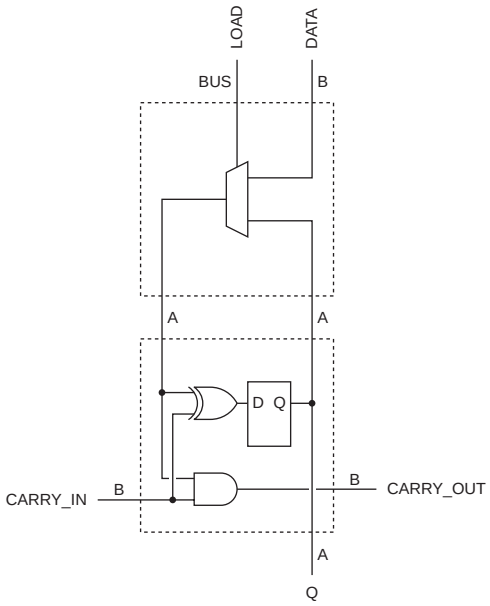






Building Complex Functions From Macros

Two-cell-per-bit counter with parallel load. CRPST and CRP4 can be combined to make two-cell-per-bit counters with parallel load. Connect the RCI pin of the least-significant bit to the active-low load signal in CRPST. CRPST uses two cells. The first cell is configured as a multiplexer, the second is a D-type flip-flop preceded by an XOR. With one of the inputs to the XOR active low, loaded data goes through the XOR and is passed to the flip-flop.



If the counter is to be loaded automatically when the maximum count is reached, the carry-out signal is first inverted and then connected to the load pin. When maximum count is reached, the carry-out signal goes high. Since the load signal must be active low, the inverted signal enables the load operation. Since the inverted carry-out signal is fed back into the carry-in pin, a feedback loop is created and the circuit turns into a ring oscillator. In order to avoid this, the carry-out signal should be

registered first before inverting it. By doing this, when maximum count is reached, the load operation is carried out first. Then on the following clock cycle, the carry-out signal is inverted, which causes the counter to resume operation.

Ripple-carry counter of arbitrary length and n number of bits. Ripple-carry counters are made using CR0, CR1 and CRST. Connect the Q0 output of CR0 to the RCI input of CR1, and connect the RCO output of CR1 to the RCI input of CRST. For counters with parallel load, use CRPST instead of CRST.

Shift register of arbitrary length and n number of bits. A shift register of any size is made by cascading a series of FD (D-type flip-flop) macros. Simply connect the Q output of the first flip-flop into the D input of the next. The shift register macros (SRP4 and SRPST) use FD as a building block and can be used to make more complex shift registers. To create a 5-bit shift register with parallel load, connect the Q3 output of SRP4 to the SI input of SRPST. Some or all of the bits in a shift register can be made loadable.

For More Information

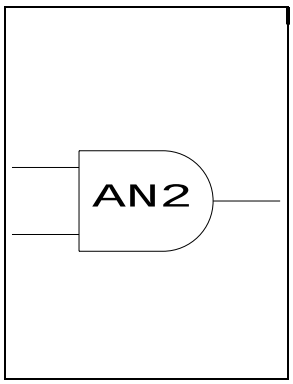
Assistance with any matter related to the IDS can be obtained by the following methods:

1. Calling Customer Service at 408.436.4119 between 9 am and 5 pm, Pacific Standard Time.
2. Sending electronic mail to fpga@atmel.com.
3. Using the bulletin board by calling 408.436.4309.
4. Faxing to 408.436.4200.
5. Writing to:

   Atmel Customer Service
   2325 Orchard Parkway
   San Jose, CA 95131
   USA

AN2 - 2-Input AND

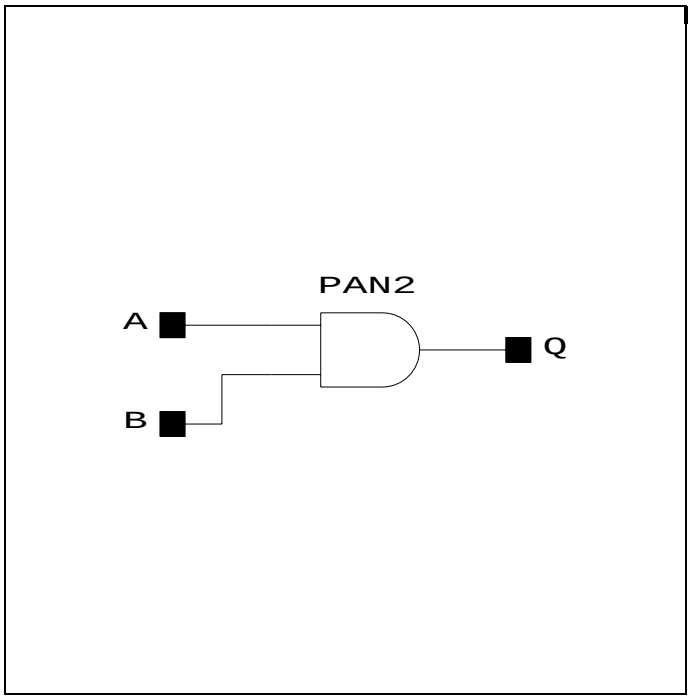
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

Switching Speeds for -2ns Parts

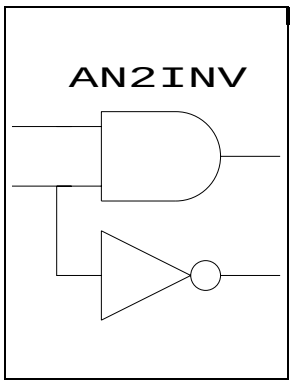
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	0.40	0.70	1.10	0.40	0.70	1.10
B → Q	0.40	0.70	1.10	0.50	0.80	1.20

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.00	1.30	1.70	1.00	1.20	1.70
B → Q	1.00	1.30	1.70	1.40	1.60	2.10

AN2INV - 2-Input AND with Inverted Input (A*B')

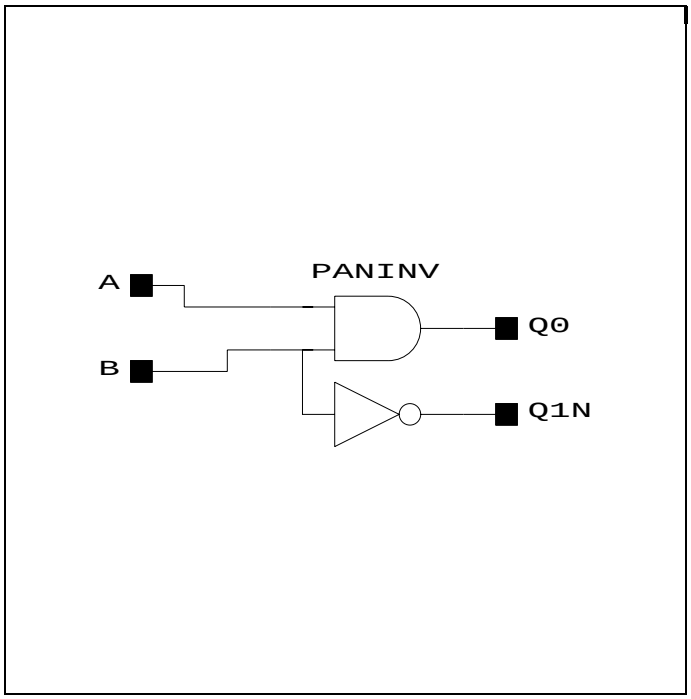
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	B	Q0	Q1N
0	0	0	1
0	1	0	0
1	0	0	1
1	1	1	0

Switching Speeds for -2ns Parts

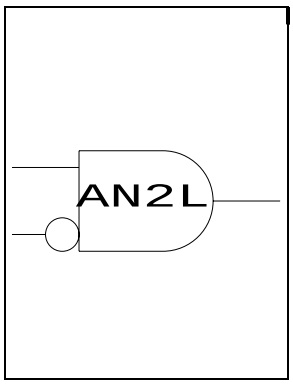
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q0	0.40	0.70	1.10	0.40	0.70	1.10
B → Q0	0.40	0.70	1.10	0.50	0.80	1.20
B → Q1N	0.70	1.10	1.50	0.90	1.30	1.70

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q0	1.00	1.30	1.70	1.00	1.20	1.70
B → Q0	1.00	1.30	1.70	1.40	1.60	2.10
B → Q1N	1.50	1.80	2.30	1.70	2.00	2.40

AN2L - 2-Input AND (AB')

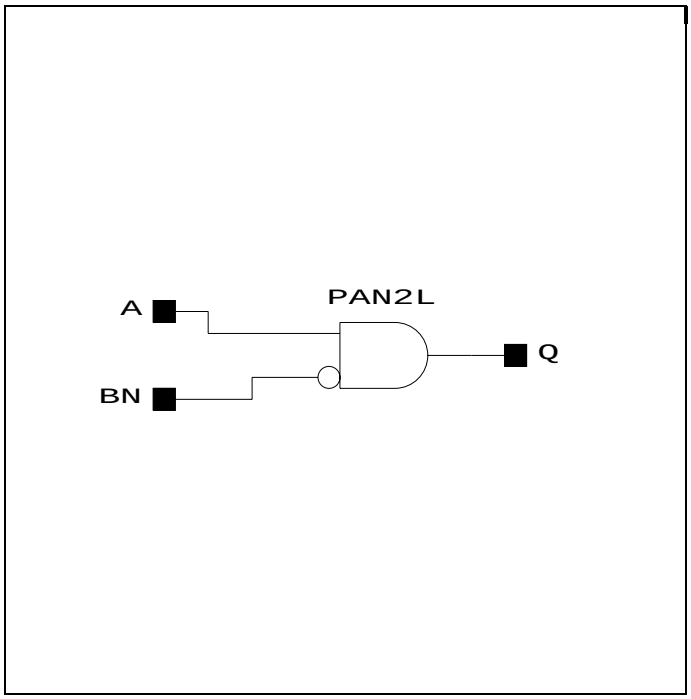
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	BN	Output Q
0	0	0
0	1	0
1	0	1
1	1	0

Switching Speeds for -2ns Parts

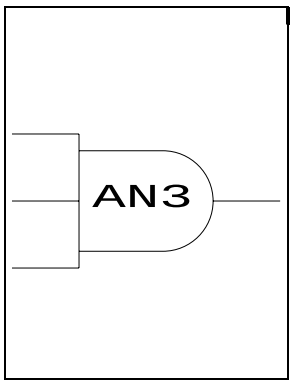
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
BN → Q	0.80	1.10	1.50	0.90	1.30	1.80
A → Q	0.40	0.70	1.10	0.40	0.70	1.10

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
BN → Q	1.50	1.80	2.40	1.60	2.00	2.50
A → Q	1.00	1.20	1.70	0.90	1.20	1.60

AN3 - 3-Input AND

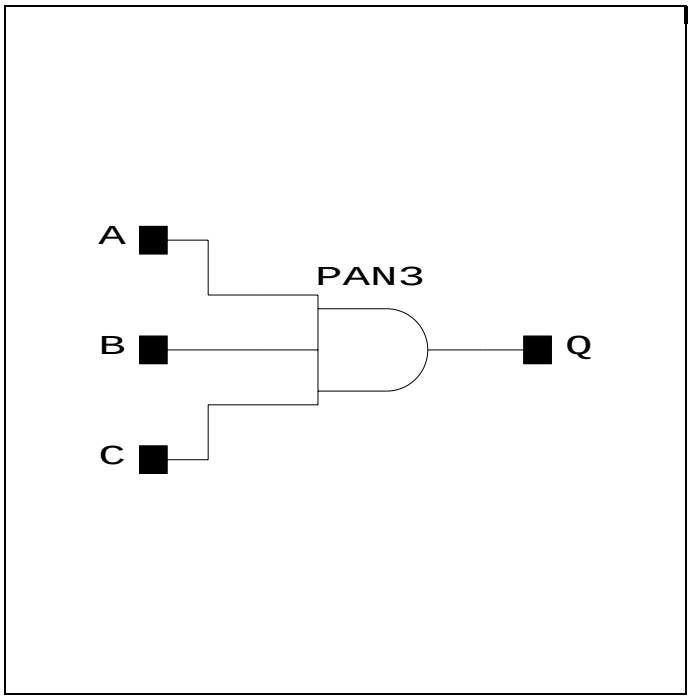
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	B	C	Output Q
0	x	x	0
x	0	x	0
x	x	0	0
1	1	1	1

Switching Speeds for -2ns Parts

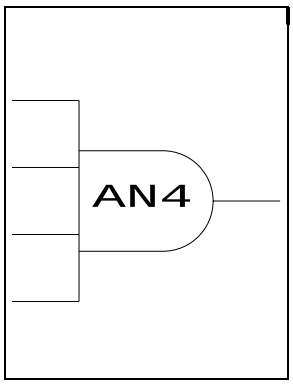
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	0.60	1.20	1.90	0.80	1.50	2.20
B → Q	0.60	1.20	1.90	0.80	1.50	2.20
C → Q	0.60	1.20	1.90	0.90	1.60	2.30

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.70	2.10	2.90	1.80	2.30	3.00
B → Q	1.70	2.10	2.90	1.80	2.30	3.00
C → Q	1.70	2.10	2.90	2.20	2.70	3.40

AN4 - 4-Input AND

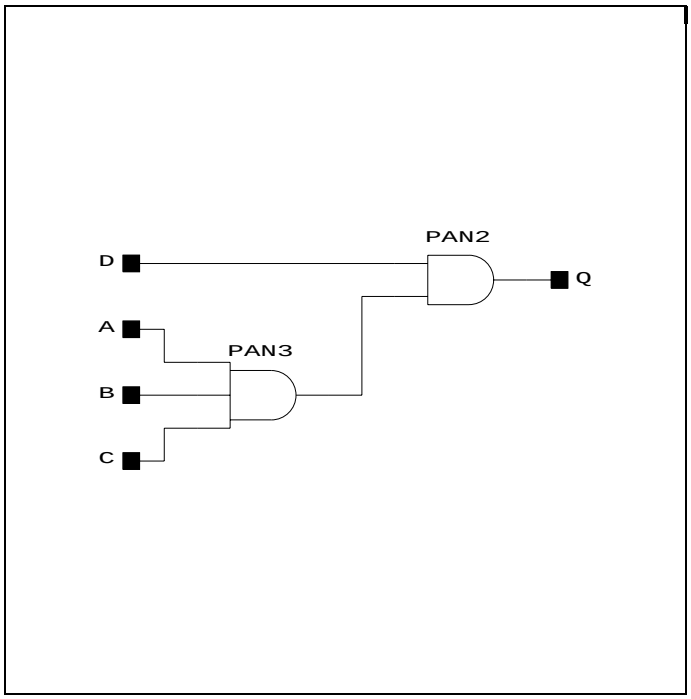
Symbol



Rectangular Area: 2x1 cells

Number of Cells: 2

Schematic



Truth Table

Input A	B	C	D	Output Q
0	x	x	x	0
x	0	x	x	0
x	x	0	x	0
x	x	x	0	0
1	1	1	1	1

Switching Speeds for -2ns Parts

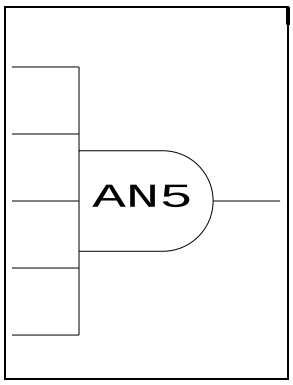
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → Q	1.28	2.49	3.90	1.69	3.11	4.52
B → Q	1.28	2.49	3.90	1.69	3.11	4.52
C → Q	1.28	2.49	3.90	1.79	3.20	4.62
D → Q	0.60	1.20	1.90	0.80	1.50	2.20

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → Q	3.47	4.29	5.92	3.68	4.71	6.15
B → Q	3.47	4.29	5.92	3.68	4.71	6.15
C → Q	3.47	4.29	5.92	4.08	5.11	6.55
D → Q	1.70	2.10	2.90	1.80	2.30	3.00

AN5 - 5-Input AND

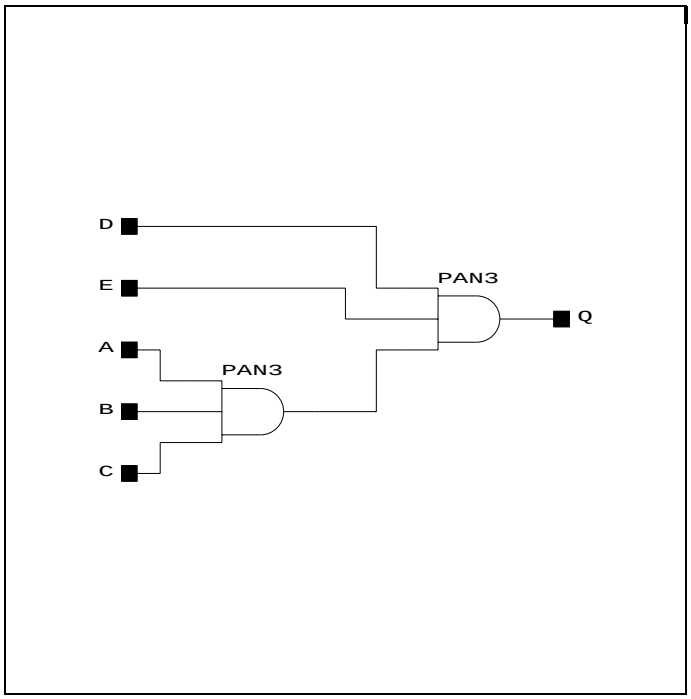
Symbol



Rectangular Area: 2x1 cells

Number of Cells: 2

Schematic



Truth Table

Input A	B	C	D	E	Output Q
0	x	x	x	x	0
x	0	x	x	x	0
x	x	0	x	x	0
x	x	x	0	x	0
x	x	x	x	0	0
1	1	1	1	1	1

Switching Speeds for -2ns Parts

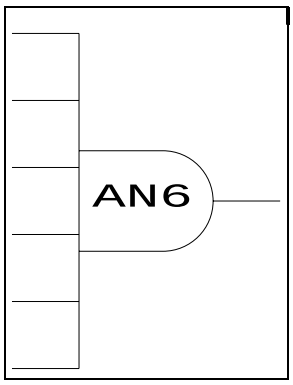
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
E → Q	0.60	1.20	1.90	0.90	1.60	2.30
D → Q	0.60	1.20	1.90	0.80	1.50	2.20
C → Q	1.28	2.49	3.90	1.79	3.20	4.62
B → Q	1.28	2.49	3.90	1.69	3.11	4.52
A → Q	1.28	2.49	3.90	1.69	3.11	4.52

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
E → Q	1.70	2.10	2.90	2.20	2.70	3.40
D → Q	1.70	2.10	2.90	1.80	2.30	3.00
C → Q	3.47	4.29	5.92	4.08	5.11	6.55
B → Q	3.47	4.29	5.92	3.68	4.71	6.15
A → Q	3.47	4.29	5.92	3.68	4.71	6.15

AN6 - 6-Input AND

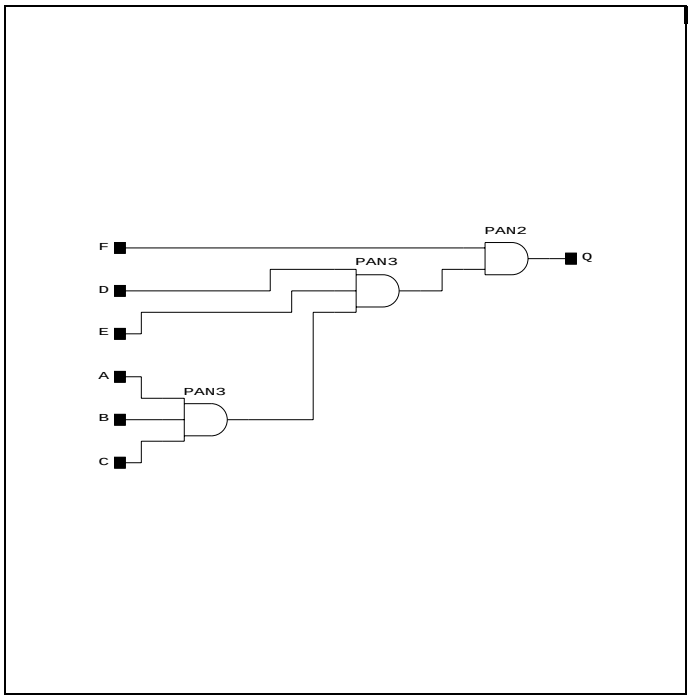
Symbol



Rectangular Area: 3x1 cells

Number of Cells: 3

Schematic



Truth Table

Input						Output
A	B	C	D	E	F	Q
0	x	x	x	x	x	0
x	0	x	x	x	x	0
x	x	0	x	x	x	0
x	x	x	0	x	x	0
x	x	x	x	0	x	0
x	x	x	x	x	0	0
1	1	1	1	1	1	1

Switching Speeds for -2ns Parts

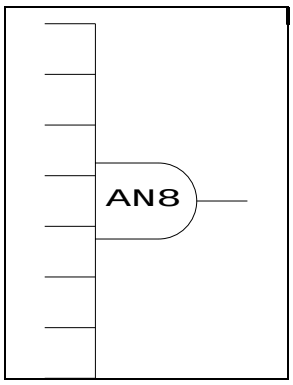
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
F → Q	0.60	1.20	1.90	0.80	1.50	2.20
E → Q	1.28	2.49	3.90	1.79	3.20	4.62
D → Q	1.28	2.49	3.90	1.69	3.11	4.52
C → Q	1.96	3.78	5.90	2.68	4.81	6.94
B → Q	1.96	3.78	5.90	2.58	4.71	6.84
A → Q	1.96	3.78	5.90	2.58	4.71	6.84

Switching Speeds for -4ns Parts

Pin	Rise			Fall		
	Min	Typ	Max	Min	Typ	Max
F → Q	1.70	2.10	2.90	1.80	2.30	3.00
E → Q	3.47	4.29	5.92	4.08	5.11	6.55
D → Q	3.47	4.29	5.92	3.68	4.71	6.15
C → Q	5.24	6.48	8.94	5.96	7.52	9.71
B → Q	5.24	6.48	8.94	5.56	7.12	9.31
A → Q	5.24	6.48	8.94	5.56	7.12	9.31

AN8 - 8-Input AND

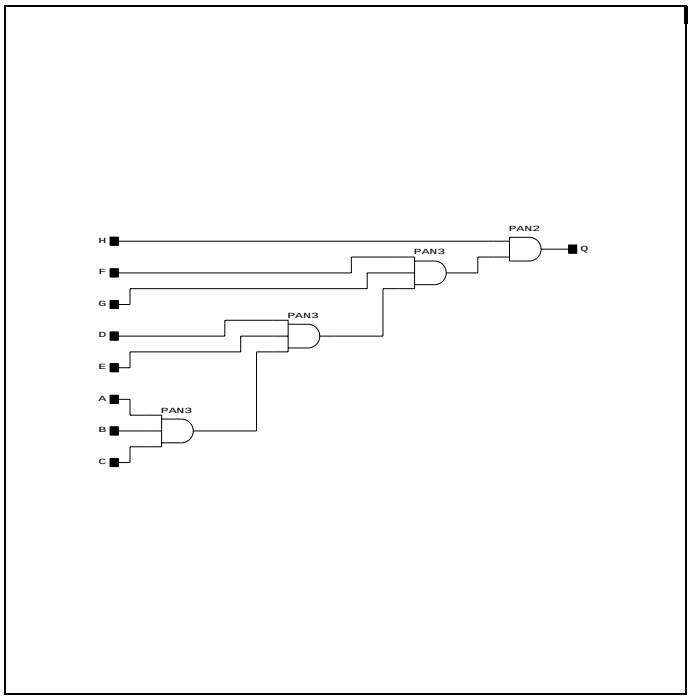
Symbol



Rectangular Area: 4x1 cells

Number of Cells: 4

Schematic



Truth Table

Input								Output
A	B	C	D	E	F	G	H	Q
0	x	x	x	x	x	x	x	0
x	0	x	x	x	x	x	x	0
x	x	0	x	x	x	x	x	0
x	x	x	0	x	x	x	x	0
x	x	x	x	0	x	x	x	0
x	x	x	x	x	0	x	x	0
x	x	x	x	x	x	0	x	0
x	x	x	x	x	x	x	0	0
1	1	1	1	1	1	1	1	1

Switching Speeds for -2ns Parts

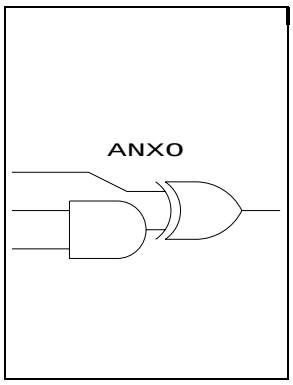
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
H → Q	0.60	1.20	1.90	0.80	1.50	2.20
G → Q	1.28	2.49	3.90	1.79	3.20	4.62
F → Q	1.28	2.49	3.90	1.69	3.11	4.52
E → Q	1.96	3.78	5.90	2.68	4.81	6.94
D → Q	1.96	3.78	5.90	2.58	4.71	6.84
C → Q	2.64	5.07	7.90	3.57	6.41	9.26
B → Q	2.64	5.07	7.90	3.47	6.32	9.16
A → Q	2.64	5.07	7.90	3.47	6.32	9.16

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
H → Q	1.70	2.10	2.90	1.80	2.30	3.00
G → Q	3.47	4.29	5.92	4.08	5.11	6.55
F → Q	3.47	4.29	5.92	3.68	4.71	6.15
E → Q	5.24	6.48	8.94	5.96	7.52	9.71
D → Q	5.24	6.48	8.94	5.56	7.12	9.31
C → Q	7.02	8.67	11.96	7.84	9.93	12.86
B → Q	7.02	8.67	11.96	7.44	9.53	12.46
A → Q	7.02	8.67	11.96	7.44	9.53	12.46

ANXO - 2-Input AND Feeding an XOR

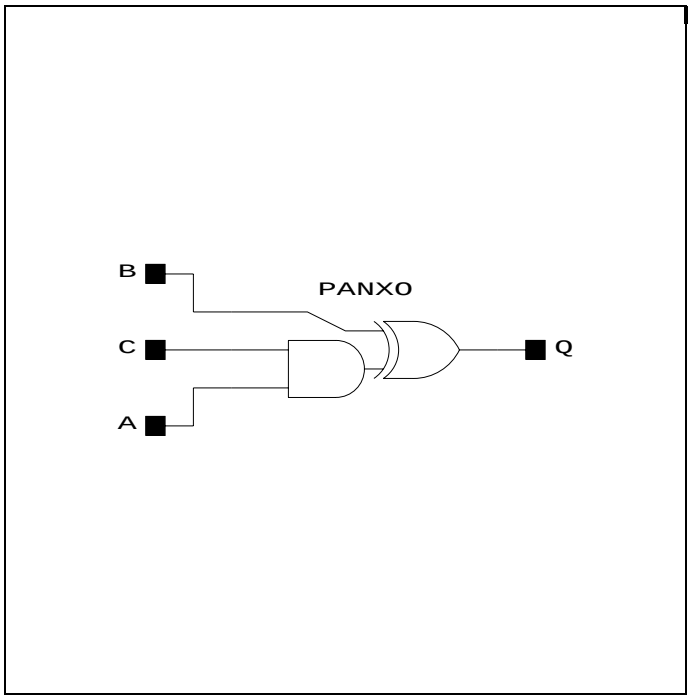
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input			Output
A	B	C	Q
0	0	0	0
x	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Switching Speeds for -2ns Parts

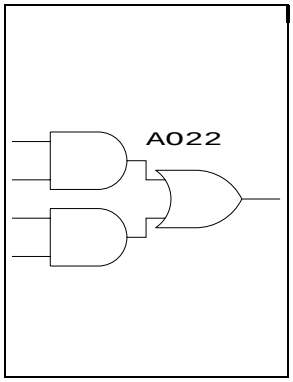
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	0.80	1.40	2.10	0.80	1.50	2.20
B → Q	0.80	1.40	2.10	0.80	1.50	2.20
C → Q	0.80	1.40	2.10	0.90	1.60	2.30

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.80	2.30	3.10	2.50	3.10	4.20
B → Q	1.80	2.30	3.10	2.50	3.10	4.20
C → Q	1.80	2.30	3.10	2.90	3.50	4.60

AO22 - AND-OR Inverter 2-2 Inputs

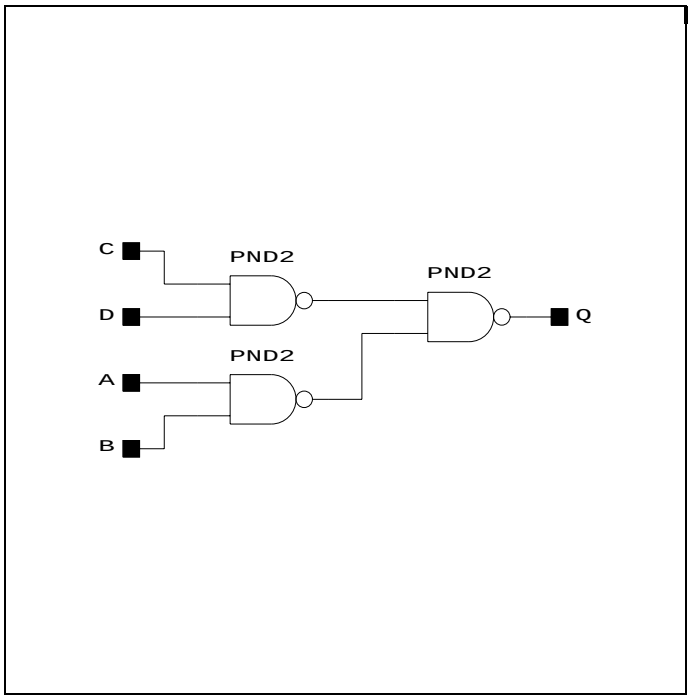
Symbol



Rectangular Area: 2x2 cells

Number of Cells: 4

Schematic



Truth Table

Input A	B	C	D	Output Q
0	x	0	x	0
0	x	x	0	0
x	0	0	x	0
x	0	x	0	0
1	1	x	x	1
x	x	1	1	1

Switching Speeds for -2ns Parts

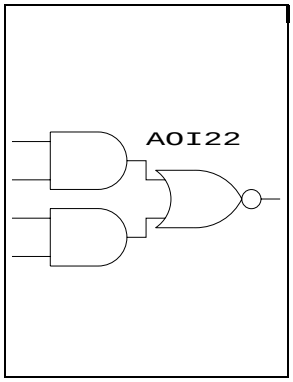
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D → Q	2.04	3.66	5.59	2.06	3.67	5.58
C → Q	2.04	3.66	5.59	2.06	3.67	5.58
B → Q	1.57	2.88	4.40	1.58	2.88	4.39
A → Q	1.57	2.88	4.40	1.58	2.88	4.39

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D → Q	4.64	5.77	7.75	4.64	5.88	7.85
C → Q	4.64	5.77	7.75	4.64	5.88	7.85
B → Q	3.56	4.48	6.02	3.56	4.49	6.02
A → Q	3.56	4.48	6.02	3.56	4.49	6.02

AOI22 - AND-OR Inverter 2-2 Inputs

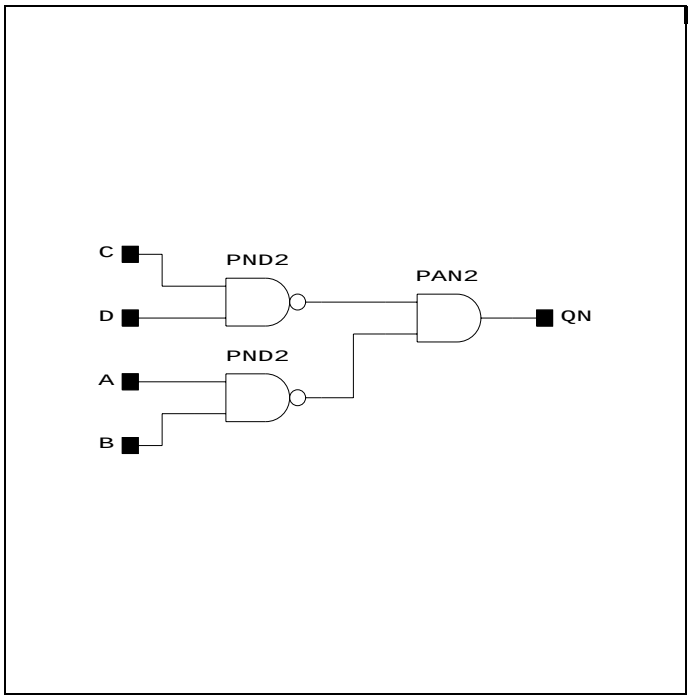
Symbol



Rectangular Area: 2x2 cells

Number of Cells: 4

Schematic



Truth Table

Input A	B	C	D	Output QN
0	x	0	x	1
0	x	x	0	1
x	0	0	x	1
x	0	x	0	1
1	1	x	x	0
x	x	1	1	0

Switching Speeds for -2ns Parts

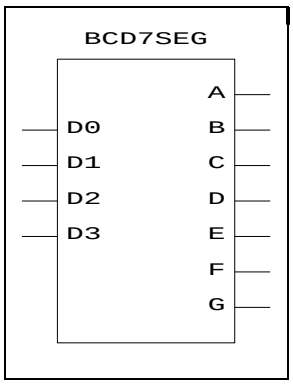
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
D → QN	1.96	3.47	5.38	2.04	3.76	5.59
C → QN	1.96	3.47	5.38	2.04	3.76	5.59
B → QN	1.48	2.68	4.19	1.57	2.99	4.40
A → QN	1.48	2.68	4.19	1.57	2.99	4.40

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
D → QN	4.54	5.68	7.75	4.74	5.97	7.85
C → QN	4.54	5.68	7.75	4.74	5.97	7.85
B → QN	3.46	4.29	5.92	3.66	4.68	6.12
A → QN	3.46	4.29	5.92	3.66	4.68	6.12

BCD7SEG - 7-Segment BCD Display (0 to 9)

Symbol



Rectangular Area: 4x21 cells

Number of Cells: 48

Truth Table

Input				Output						
D3	D2	D1	D0	A	B	C	D	E	F	G
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	0	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1

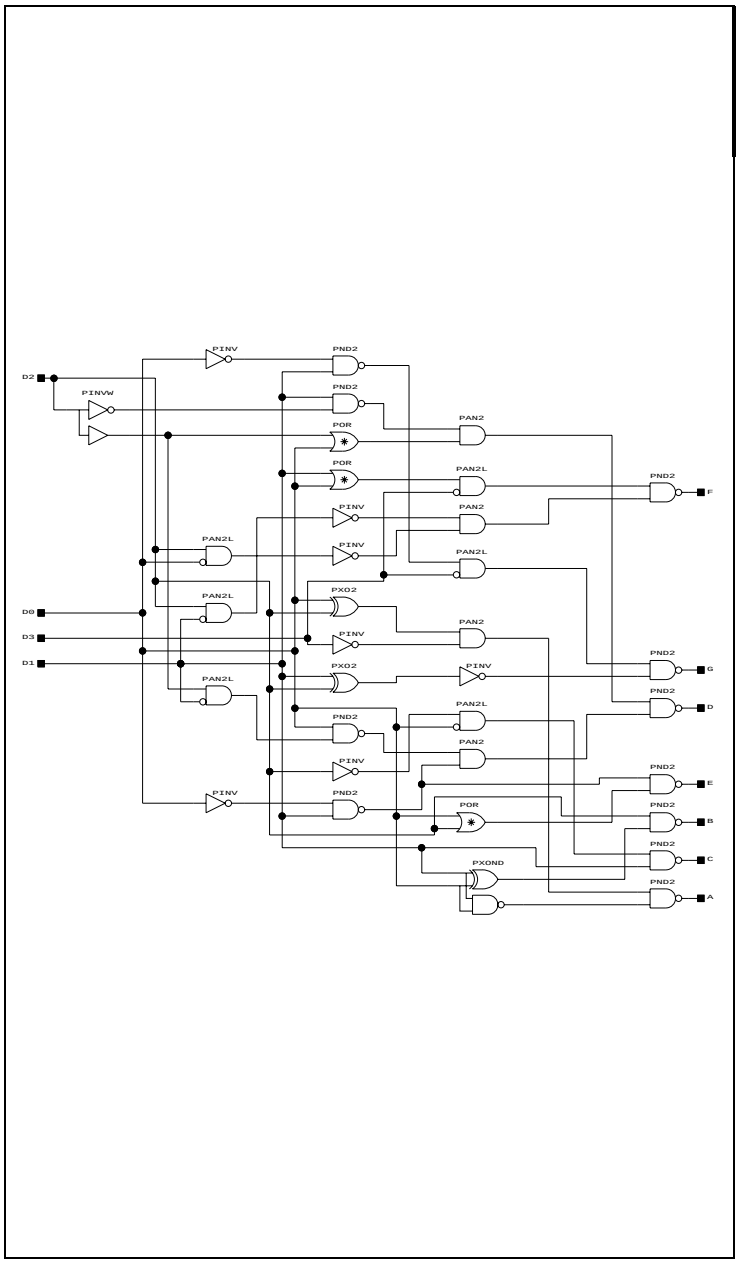
Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
D2 → G	2.44	4.56	6.78	2.44	4.66	6.78
D3 → G	2.24	3.56	5.28	2.06	3.37	4.88
D1 → G	2.44	4.56	6.88	2.34	4.50	6.68
D0 → G	3.39	5.63	8.37	3.51	5.84	8.46
D2 → F	2.94	5.66	9.10	2.72	5.44	8.67
D3 → F	2.71	4.34	6.47	2.54	4.16	6.08
D1 → F	3.34	5.88	9.25	3.22	5.88	9.06
D0 → F	3.65	6.33	9.50	3.49	6.18	9.37
D2 → E	1.67	2.98	4.49	1.57	2.88	4.29
D1 → E	2.21	3.84	5.77	2.23	3.85	5.67
D0 → E	1.77	4.06	7.36	1.57	4.01	7.36
D2 → D	4.14	7.80	12.76	3.77	7.44	12.43
D1→ D	3.13	6.18	10.47	2.74	5.84	10.05
D0 → D	3.13	6.78	12.06	2.74	6.47	11.74
D2 → C	2.24	3.56	5.08	2.06	3.47	4.98
D1 → C	0.90	1.50	2.20	0.80	1.50	2.20
D0 → C	1.77	2.78	3.99	1.68	2.68	3.79
D2 → B	0.80	1.40	2.20	0.70	1.40	2.10
D1 → B	1.57	2.88	4.39	1.57	3.08	4.49
D0 → B	1.67	2.98	4.49	1.57	3.08	4.49
D2 → A	2.46	4.49	6.71	2.25	4.37	6.49
D3 → A	2.66	4.39	6.31	2.16	3.88	5.69
D1 → A	2.14	3.66	5.59	2.06	3.67	5.48
D0 → A	2.24	4.18	6.81	2.06	4.02	6.49

Switching Speeds for -4ns Parts

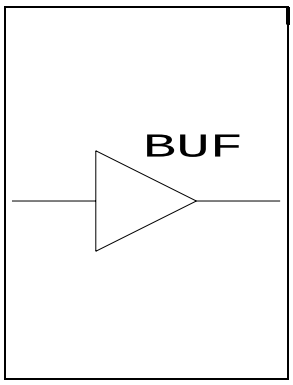
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D2 → G	5.74	7.07	9.53	6.24	7.67	10.03
D3 → G	4.34	5.48	7.26	4.44	5.48	7.34
D1 → G	5.51	7.02	9.53	5.84	7.42	10.16
D0 → G	7.08	8.85	11.91	7.58	9.26	12.29
D2 → F	6.72	8.88	12.73	6.52	8.76	12.69
D3 → F	5.52	6.77	9.10	5.52	6.97	9.17
D1 → F	7.22	9.71	14.25	7.22	9.56	13.52
D0 → F	7.99	10.41	14.65	7.96	10.15	13.59
D2 → E	4.26	5.28	7.22	3.67	4.69	6.21
D1 → E	5.41	6.66	9.08	5.22	6.57	8.57
D0 → E	4.66	7.16	11.62	3.67	6.48	10.81
D2 → D	9.16	12.55	18.36	8.73	12.43	18.53
D1 → D	6.42	9.86	15.70	6.91	10.01	15.26
D0 → D	6.52	10.86	18.24	6.91	10.90	17.49
D2 → C	4.64	5.68	7.36	5.14	6.38	8.45
D1 → C	2.20	2.70	3.50	2.50	3.10	4.20
D0 → C	3.57	4.39	5.73	4.07	5.09	6.73
D2 → B	1.70	2.10	2.90	1.80	2.30	3.00
D1 → B	3.76	4.68	6.32	3.77	4.69	6.21
D0 → B	4.16	5.08	6.72	3.77	4.69	6.21
D2 → A	5.64	7.09	9.48	5.54	6.88	9.23
D3 → A	5.35	6.60	8.59	5.14	6.38	8.44
D1 → A	4.64	5.67	7.75	4.74	5.98	7.95
D0 → A	4.64	6.58	9.88	5.14	6.63	9.23

Schematic



BUFFER/BUFFERB - Buffer

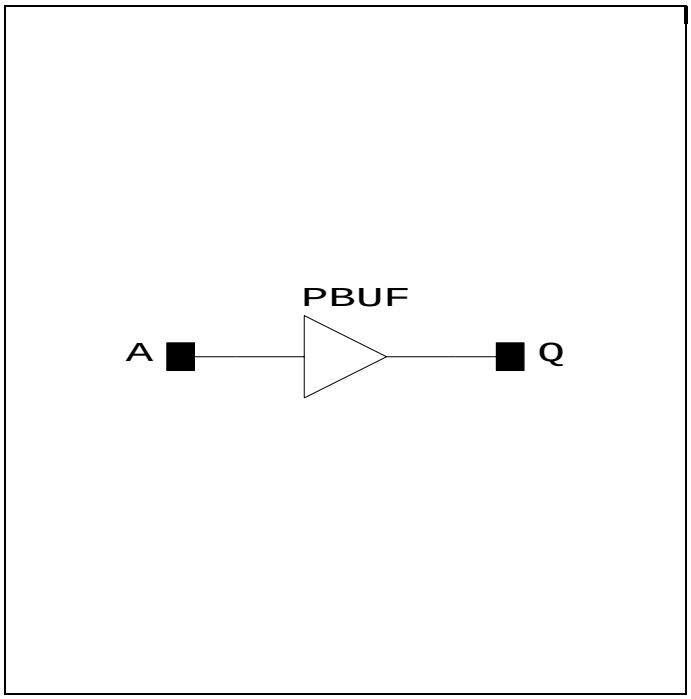
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output Q
0	0
1	1

Switching Speeds for -2ns Parts

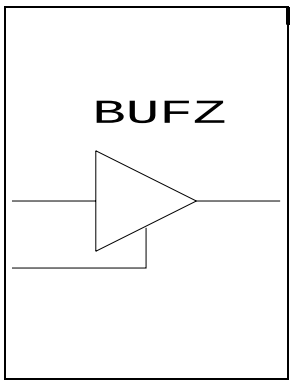
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	0.40	0.70	1.10	0.40	0.70	1.10

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.00	1.30	1.70	1.00	1.20	1.60

BUFZ - Tristate Buffer

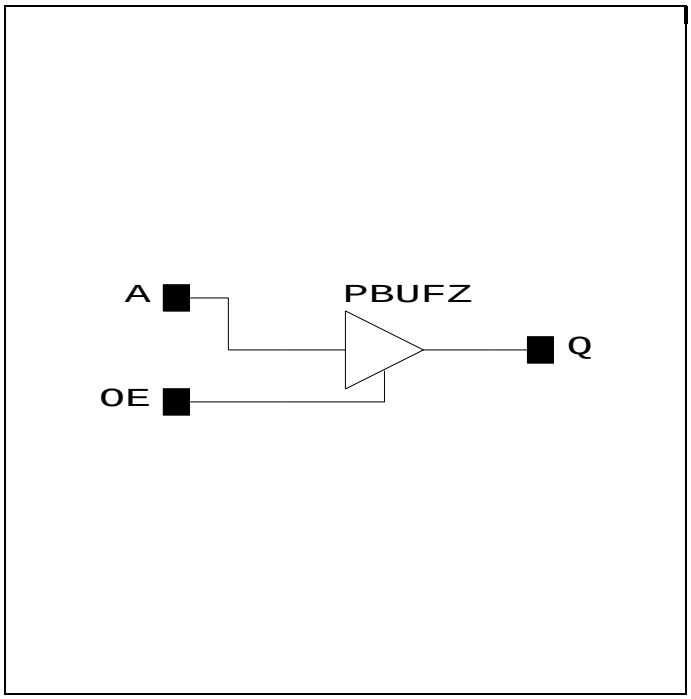
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input OE	A	Output Q
0	x	z
1	a	a

Switching Speeds for -2ns Parts

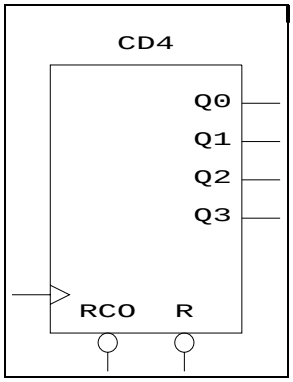
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q	0.80	1.41	2.38	0.94	1.67	2.63
A → Q	1.30	2.01	2.88	1.44	2.27	3.13

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q	2.27	2.91	4.20	3.22	4.07	5.77
A → Q	2.77	3.41	4.80	3.72	4.57	6.37

CD4 - 4-Bit Decade Counter

Symbol



Rectangular Area: 4x15cells

Number of Cells: 19

Truth Table

Input		Output				
R	**CLK**	**Q3**	**Q2**	**Q1**	**Q0**	**RCO**
0	x	0	0	0	0	1
1	x	q	q	q	q	(q3*q0)'
1	r	present state + 1				(q3*q0)'

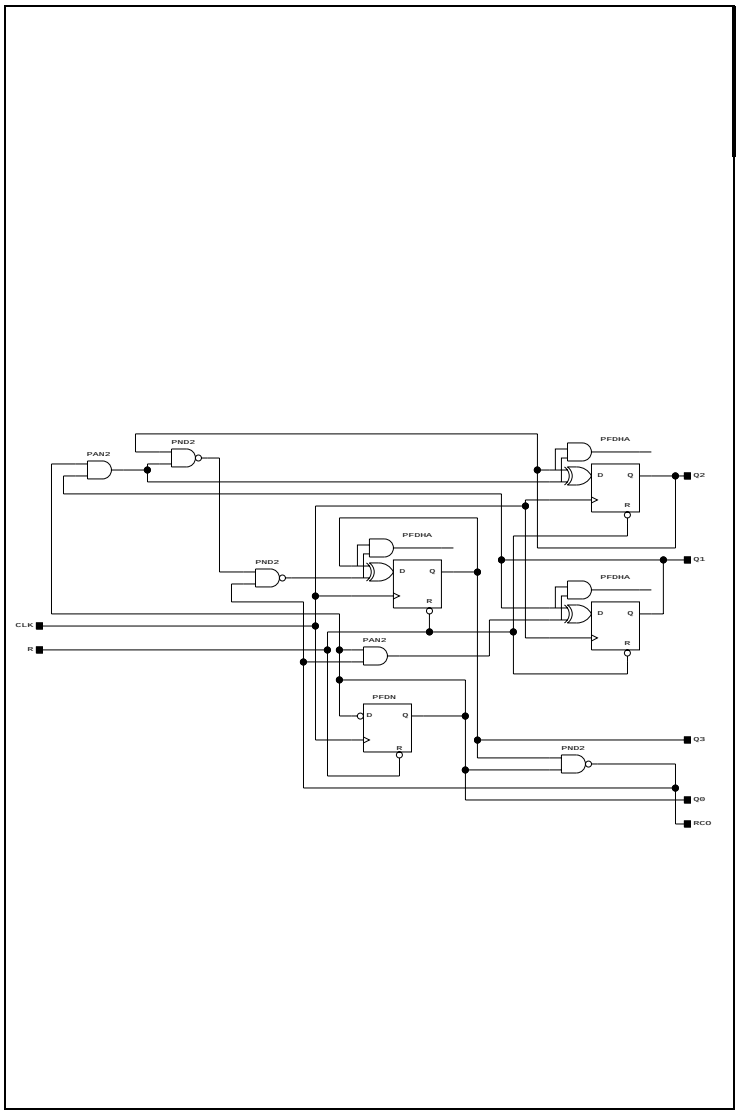
Switching Speeds for -2ns Parts

Pin	Rise			Fall		
	Min	Typ	Max	Min	Typ	Max
R → RCO	2.52	3.82	5.72	-	-	-
CLK → RCO	2.92	4.22	6.12	2.42	3.82	5.62
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.56	1.82	2.06
CLK → Q0	1.58	1.81	2.04	1.96	2.22	2.46
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.56	1.82	2.06
CLK → Q3	1.58	1.81	2.04	1.96	2.22	2.46
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33

Switching Speeds for -4ns Parts

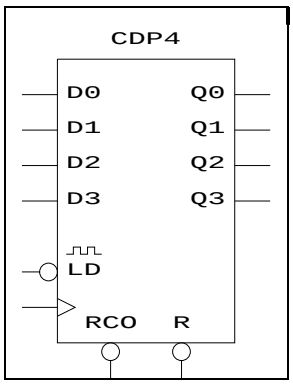
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → RCO	4.39	5.89	8.31	-	-	-
CLK → RCO	4.99	6.49	8.91	4.47	6.08	8.45
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.56	2.92	3.31
CLK → Q0	2.54	2.88	3.24	3.16	3.52	3.91
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.56	2.92	3.31
CLK → Q3	2.54	2.88	3.24	3.16	3.52	3.91
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75

Schematic


PND2
PAN2
PFDHA
D
Q
R
Q2
PFDHA
PND2
Q1
PFDHA
CLK
R
PAN2
PFDN
PND2
Q3
Q0
RCO

CDP4 - 4-Bit Decade Counter w/ Parallel Load

Symbol



Rectangular Area: 3x8cells

Number of Cells: 23

Truth Table

Input				Output	
R	**CLK**	**LD**	**D3...D0**	**Q3...Q0**	**RCO**
0	x	x	x...x	0...0	wand (q3...q0)
1	x	x	x...x	q3...q0	
1	r	0	d3...d0	d3...d0	
1	r	1	x...x	present state + 1	

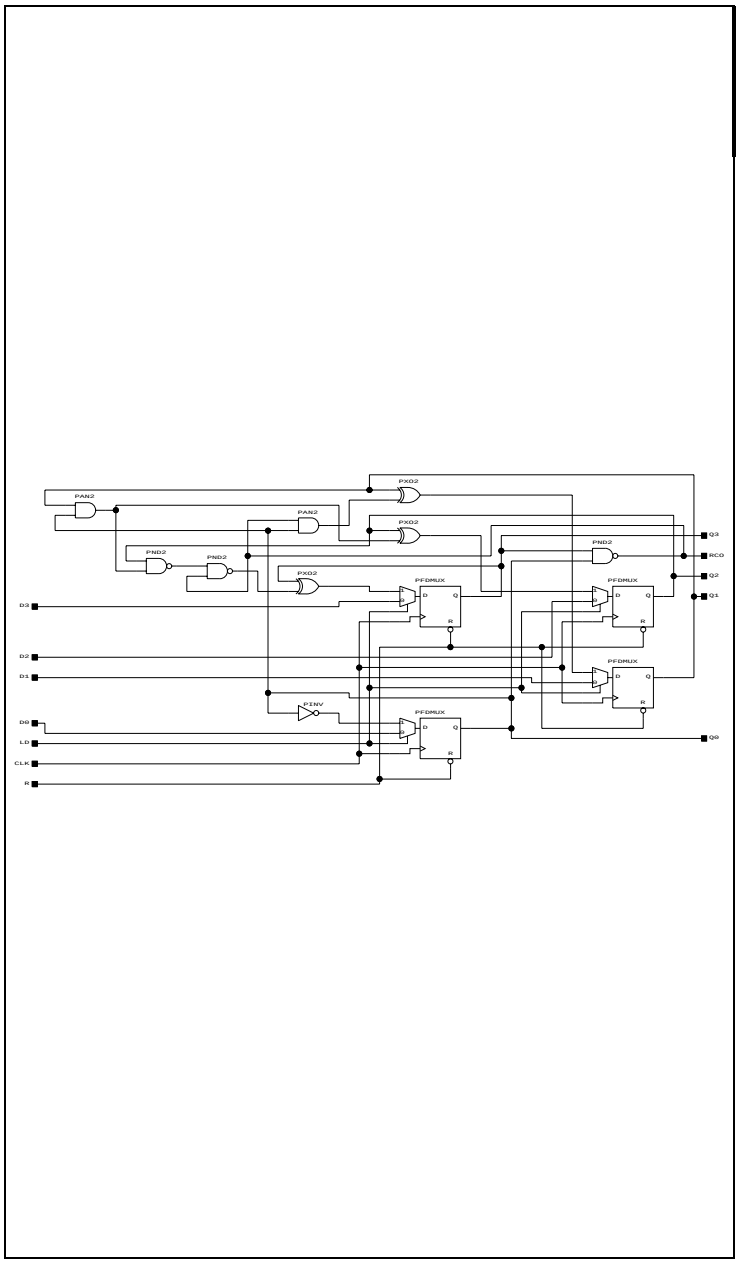
Switching Speeds for -2ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
R → RCO	2.99	4.25	5.81	-	-	-
CLK → RCO	3.39	4.65	6.21	2.90	4.26	5.71
R → Q0	-	-	-	1.56	1.82	2.06
CLK → Q0	1.58	1.81	2.04	1.96	2.22	2.46
R → Q1	-	-	-	1.56	1.82	2.06
CLK → Q1	1.58	1.81	2.04	1.96	2.22	2.46
R → Q2	-	-	-	1.56	1.82	2.06
CLK → Q2	1.58	1.81	2.04	1.96	2.22	2.46
R → Q3	-	-	-	1.56	1.82	2.06
CLK → Q3	1.58	1.81	2.04	1.96	2.22	2.46

Switching Speeds for -4ns Parts

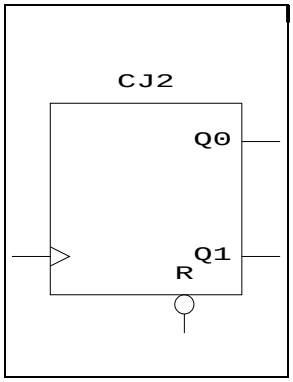
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
R → RCO	5.46	6.58	8.45	-	-	-
CLK → RCO	6.06	7.18	9.05	5.54	6.82	8.58
R → Q0	-	-	-	2.56	2.92	3.31
CLK → Q0	2.54	2.88	3.24	3.16	3.52	3.91
R → Q1	-	-	-	2.56	2.92	3.31
CLK → Q1	2.54	2.88	3.24	3.16	3.52	3.91
R → Q2	-	-	-	2.56	2.92	3.31
CLK → Q2	2.54	2.88	3.24	3.16	3.52	3.91
R → Q3	-	-	-	2.56	2.92	3.31
CLK → Q3	2.54	2.88	3.24	3.16	3.52	3.91

Schematic


PXO2
PAN2
PAN2
PXO2
PND2
PND2
PXO2
PFDMUX
PND2
PFDMUX
PFDMUX
PFDMUX
PINV
D3
D2
D1
D0
LD
CLK
R
Q3
RCO
Q2
Q1
Q0

CJ2 - 2-Bit Johnson Counter

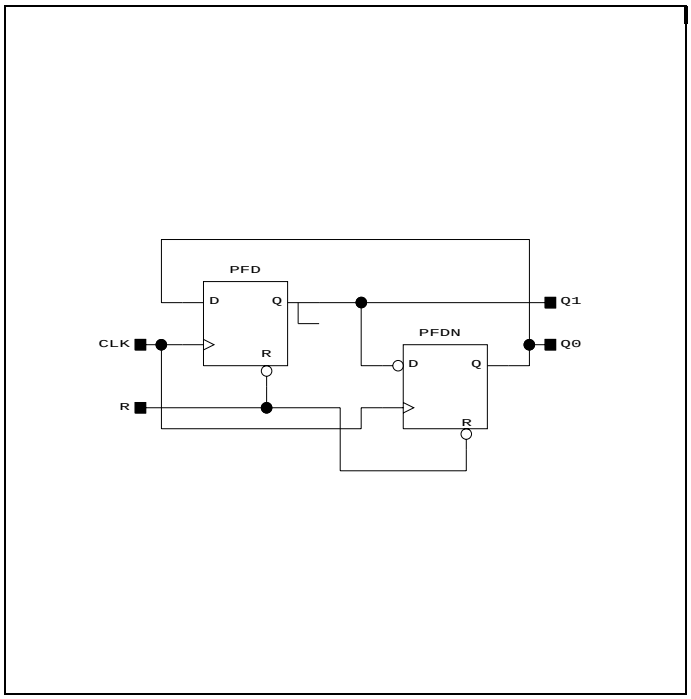
Symbol



Rectangular Area: 1x2 cells

Number of Cells: 2

Schematic



Truth Table

Input		Output	
R	**CLK**	**Q1**	**Q0**
0	x	0	0
1	r	q0	q1'

Switching Speeds for -2ns Parts

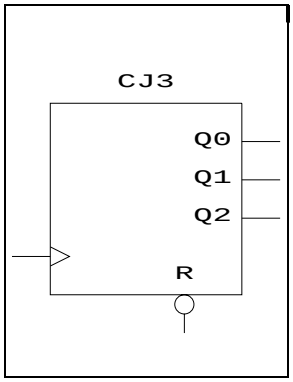
	Rise			Fall		
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.56	1.82	2.06
CLK → Q1	1.58	1.81	2.04	1.96	2.22	2.46

Switching Speeds for -4ns Parts

Pin	Rise			Fall		
	Min	Typ	Max	Min	Typ	Max
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.56	2.92	3.31
CLK → Q1	2.54	2.88	3.24	3.16	3.52	3.91

CJ3 - 3-Bit Johnson Counter

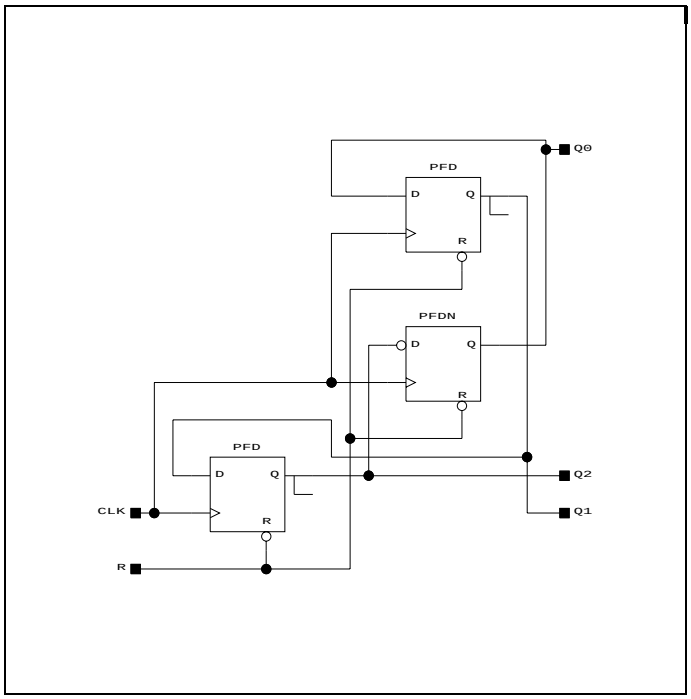
Symbol



Rectangular Area: 2x2 cells

Number of Cells: 4

Schematic



Truth Table

Input		Output		
R	CLK	Q2	Q1	Q0
0	x	0	0	0
1	r	q1	q0	q2'

Switching Speeds for -2ns Parts

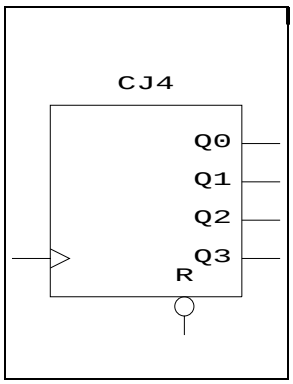
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

Switching Speeds for -4ns Parts

Pin	Rise			Fall		
	Min	Typ	Max	Min	Typ	Max
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

CJ4 - 4-Bit Johnson Counter

Symbol



Rectangular Area: 2x2 cells

Number of Cells: 4

Truth Table

Input		Output			
R	**CLK**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	0	0	0	0
1	r	q2	q1	q0	q3'

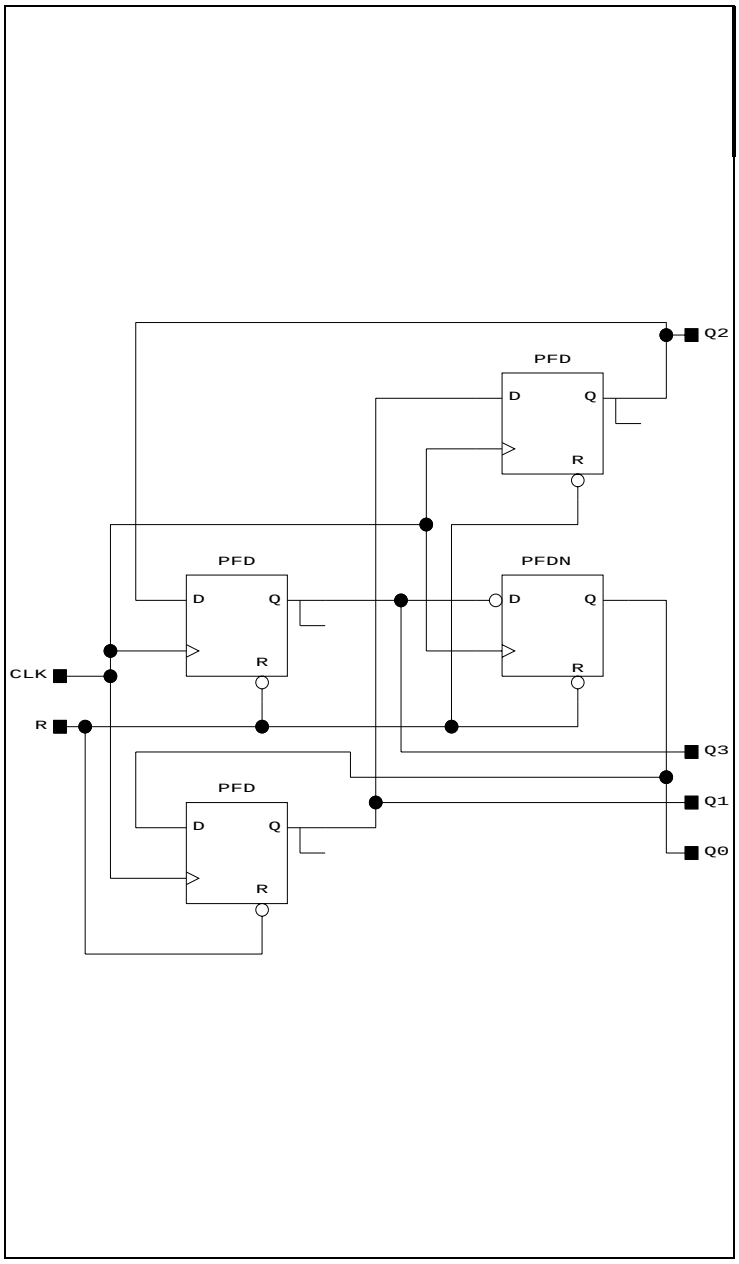
Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.56	1.82	2.06
CLK → Q3	1.58	1.81	2.04	1.96	2.22	2.46
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS.	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

Switching Speeds for -4ns Parts

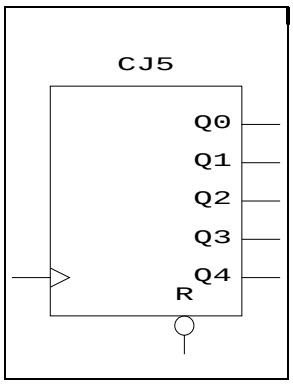
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.56	2.92	3.31
CLK → Q3	2.54	2.88	3.24	3.16	3.52	3.91
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

Schematic



CJ5 - 5-Bit Johnson Counter

Symbol



Rectangular Area: 2x3 cells

Number of Cells: 6

Truth Table

Input		Output				
R	**CLK**	**Q4**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	0	0	0	0	0
1	r	q3	q2	q1	q0	q4'

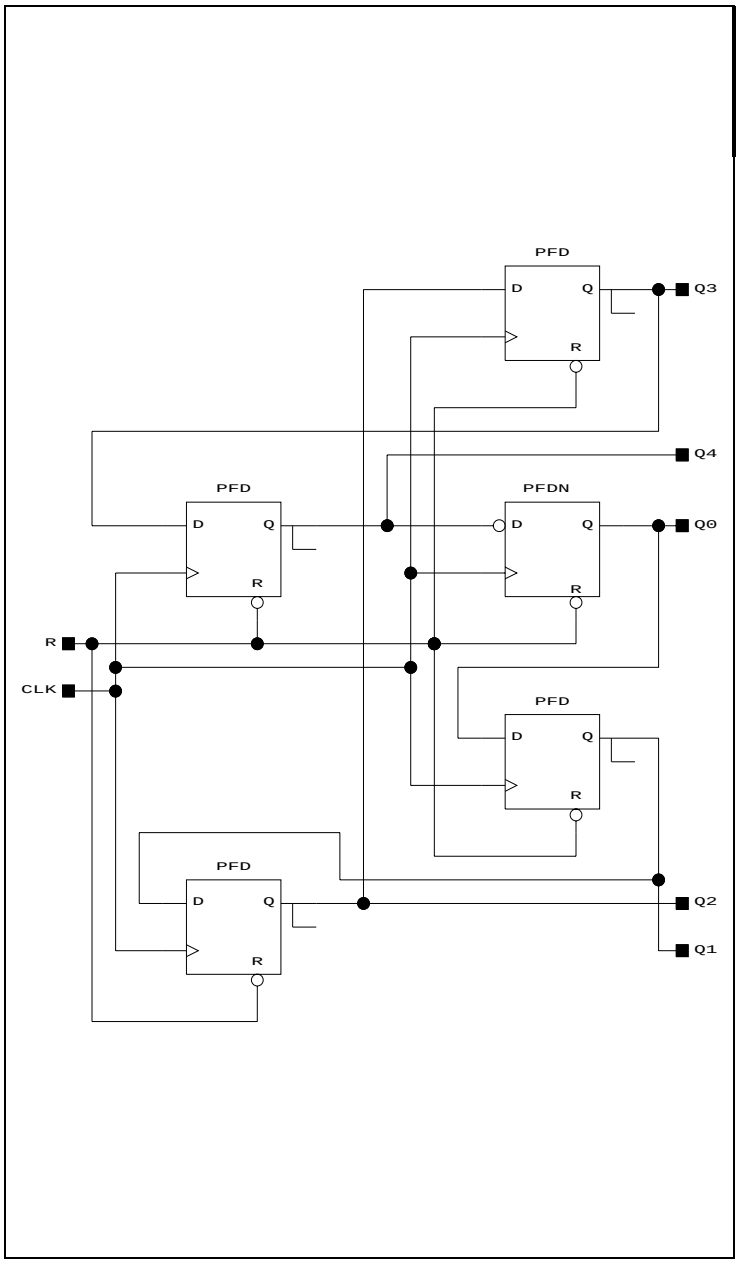
Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q4.BUS	-	-	-	1.90	2.20	2.50
CLK → Q4.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q4	-	-	-	1.48	1.71	1.93
CLK → Q4	1.49	1.71	1.92	1.88	2.11	2.33
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.48	1.71	1.93
CLK → Q3	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

Switching Speeds for -4ns Parts

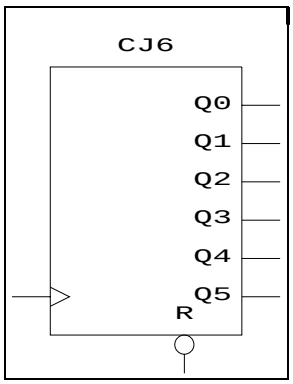
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q4.BUS	-	-	-	3.40	3.90	4.80
CLK → Q4.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q4	-	-	-	2.48	2.81	3.15
CLK → Q4	2.47	2.79	3.12	3.08	3.41	3.75
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.48	2.81	3.15
CLK → Q3	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

Schematic



CJ6 - 6-Bit Johnson Counter

Symbol



Rectangular Area: 2x3 cells

Number of Cells: 6

Truth Table

Input		Output					
R	**CLK**	**Q5**	**Q4**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	0	0	0	0	0	0
1	r	q4	q3	q2	q1	q0	q5'

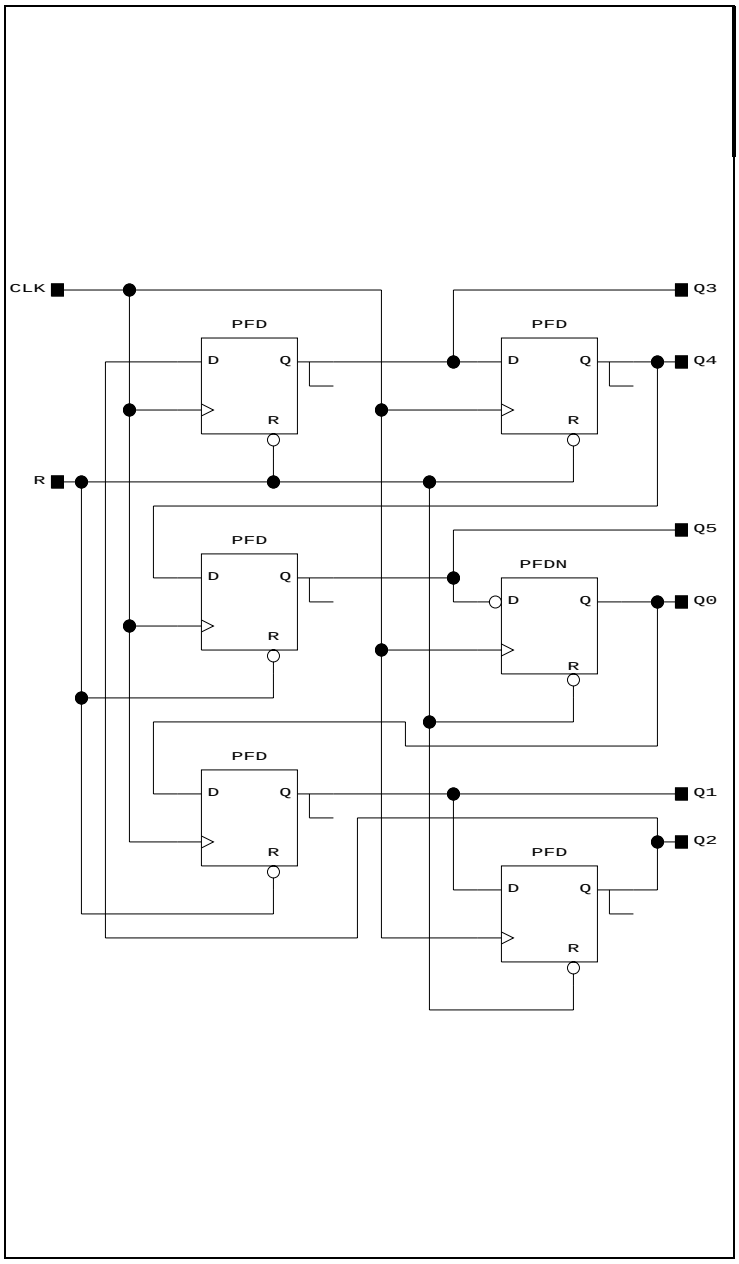
Switching Speeds for -2ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
R → Q5.BUS	-	-	-	1.90	2.20	2.50
CLK → Q5.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q5	-	-	-	1.56	1.82	2.06
CLK → Q5	1.58	1.81	2.04	1.96	2.22	2.46
R → Q4.BUS	-	-	-	1.90	2.20	2.50
CLK → Q4.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q4	-	-	-	1.48	1.71	1.93
CLK → Q4	1.49	1.71	1.92	1.88	2.11	2.33
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.48	1.71	1.93
CLK → Q3	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

Switching Speeds for -4ns Parts

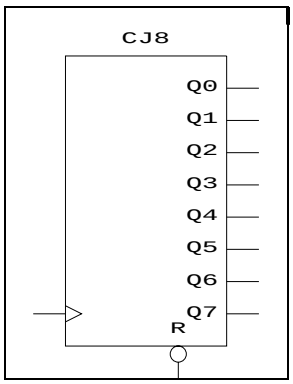
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
R → Q5.BUS	-	-	-	3.40	3.90	4.80
CLK → Q5.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q5	-	-	-	2.56	2.92	3.31
CLK → Q5	2.54	2.88	3.24	3.16	3.52	3.91
R → Q4.BUS	-	-	-	3.40	3.90	4.80
CLK → Q4.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q4	-	-	-	2.48	2.81	3.15
CLK → Q4	2.47	2.79	3.12	3.08	3.41	3.75
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.48	2.81	3.15
CLK → Q3	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

Schematic



CJ8 - 8-Bit Johnson Counter

Symbol



Rectangular Area: 2x4 cells

Number of Cells: 8

Truth Table

Input		Output							
R	**CLK**	**Q7**	**Q6**	**Q5**	**Q4**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	0	0	0	0	0	0	0	0
1	r	q6	q5	q4	q3	q2	q1	q0	q7'

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q7.BUS	-	-	-	1.90	2.20	2.50
CLK → Q7.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q7	-	-	-	1.56	1.82	2.06
CLK → Q7	1.58	1.81	2.04	1.96	2.22	2.46
R → Q6.BUS	-	-	-	1.90	2.20	2.50
CLK → Q6.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q6	-	-	-	1.48	1.71	1.93
CLK → Q6	1.49	1.71	1.92	1.88	2.11	2.33
R → Q5.BUS	-	-	-	1.90	2.20	2.50
CLK → Q5.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q5	-	-	-	1.48	1.71	1.93
CLK → Q5	1.49	1.71	1.92	1.88	2.11	2.33
R → Q4.BUS	-	-	-	1.90	2.20	2.50
CLK → Q4.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q4	-	-	-	1.48	1.71	1.93
CLK → Q4	1.49	1.71	1.92	1.88	2.11	2.33
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.48	1.71	1.93
CLK → Q3	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33

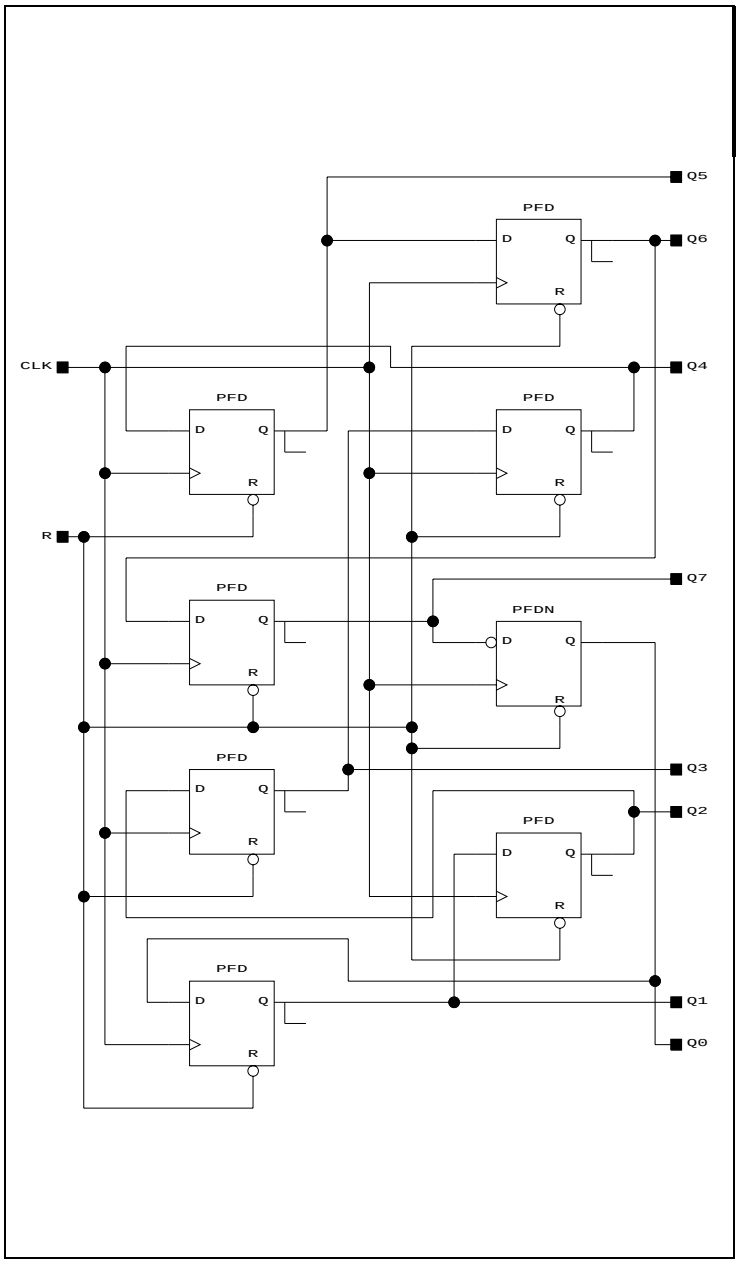
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

Switching Speeds for -4ns Parts

Pin	Rise			Fall		
	Min	Typ	Max	Min	Typ	Max
R → Q7.BUS	-	-	-	3.40	3.90	4.80
CLK → Q7.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q7	-	-	-	2.56	2.92	3.31
CLK → Q7	2.54	2.88	3.24	3.16	3.52	3.91
R → Q6.BUS	-	-	-	3.40	3.90	4.80
CLK → Q6.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q6	-	-	-	2.48	2.81	3.15
CLK → Q6	2.47	2.79	3.12	3.08	3.41	3.75
R → Q5.BUS	-	-	-	3.40	3.90	4.80
CLK → Q5.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q5	-	-	-	2.48	2.81	3.15
CLK → Q5	2.47	2.79	3.12	3.08	3.41	3.75
R → Q4.BUS	-	-	-	3.40	3.90	4.80
CLK → Q4.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q4	-	-	-	2.48	2.81	3.15
CLK → Q4	2.47	2.79	3.12	3.08	3.41	3.75
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.48	2.81	3.15
CLK → Q3	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75

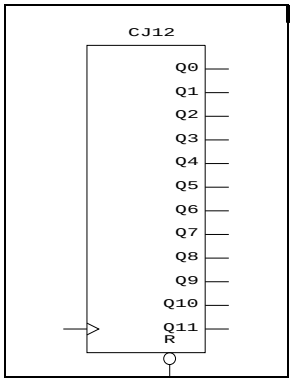
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

Schematic



CJ12 - 12-Bit Johnson Counter

Symbol



Rectangular Area: 2x6 cells

Number of Cells: 12

Truth Table

Input		Output							
R	**CLK**	**Q11**	**Q10**	**Q9**	**Q8...Q3**		**Q2**	**Q1**	**Q0**
0	x	0	0	0	0	0	0	0	0
1	r	q10	q9	q8	q7...q2		q1	q0	q11'

Switching Speeds for -2ns Parts

Pin	Rise			Fall		
	Min	Typ	Max	Min	Typ	Max
R → Q11.BUS	-	-	-	1.90	2.20	2.50
CLK → Q11.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q11	-	-	-	1.56	1.82	2.06
CLK → Q11	1.58	1.81	2.04	1.96	2.22	2.46
R → Q10.BUS	-	-	-	1.90	2.20	2.50
CLK → Q10.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q10	-	-	-	1.48	1.71	1.93
CLK → Q10	1.49	1.71	1.92	1.88	2.11	2.33
R → Q9.BUS	-	-	-	1.90	2.20	2.50
CLK → Q9.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q9	-	-	-	1.48	1.71	1.93
CLK → Q9	1.49	1.71	1.92	1.88	2.11	2.33
R → Q8.BUS	-	-	-	1.90	2.20	2.50
CLK → Q8.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q8	-	-	-	1.48	1.71	1.93
CLK → Q8	1.49	1.71	1.92	1.88	2.11	2.33
R → Q7.BUS	-	-	-	1.90	2.20	2.50
CLK → Q7.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q7	-	-	-	1.48	1.71	1.93
CLK → Q7	1.49	1.71	1.92	1.88	2.11	2.33
R → Q6.BUS	-	-	-	1.90	2.20	2.50
CLK → Q6.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q6	-	-	-	1.48	1.71	1.93
CLK → Q6	1.49	1.71	1.92	1.88	2.11	2.33

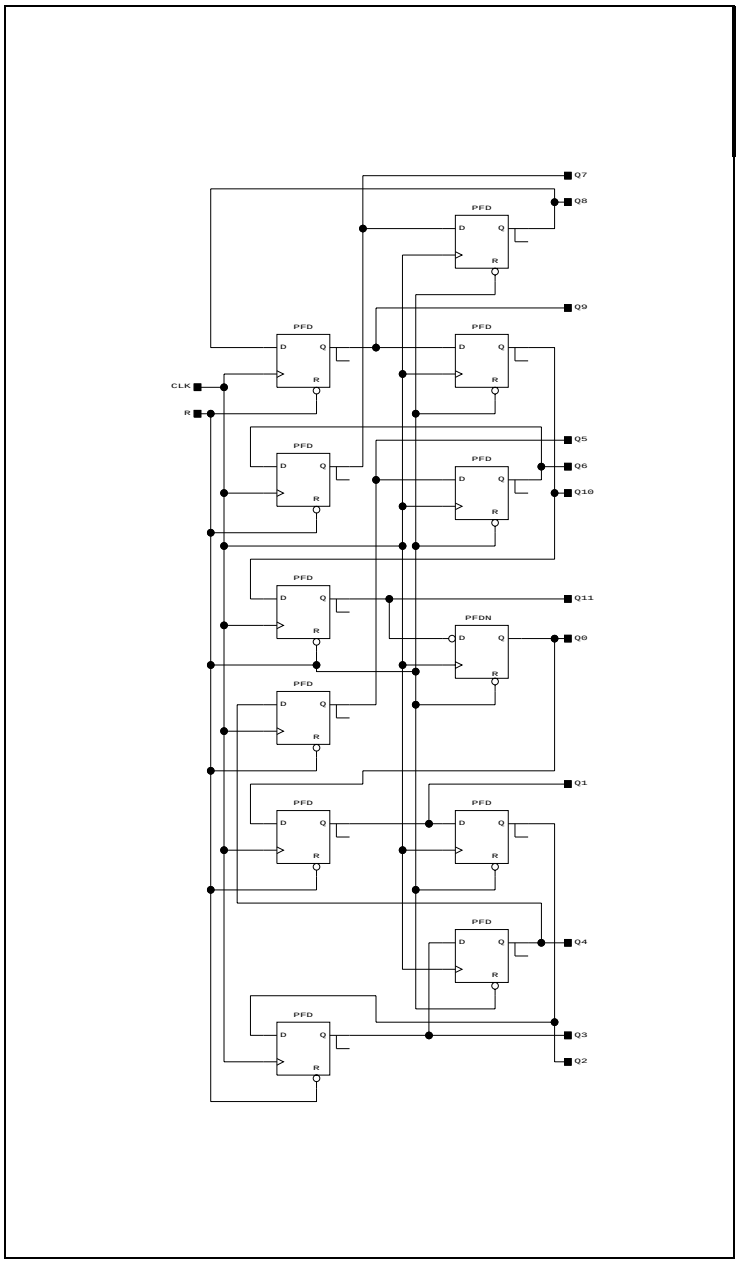
R → Q5.BUS	-	-	-	1.90	2.20	2.50
CLK → Q5.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q5	-	-	-	1.48	1.71	1.93
CLK → Q5	1.49	1.71	1.92	1.88	2.11	2.33
R → Q4.BUS	-	-	-	1.90	2.20	2.50
CLK → Q4.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q4	-	-	-	1.48	1.71	1.93
CLK → Q4	1.49	1.71	1.92	1.88	2.11	2.33
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.48	1.71	1.93
CLK → Q3	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q11.BUS	-	-	-	3.40	3.90	4.80
CLK → Q11.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q11	-	-	-	2.56	2.92	3.31
CLK → Q11	2.54	2.88	3.24	3.16	3.52	3.91
R → Q10.BUS	-	-	-	3.40	3.90	4.80
CLK → Q10.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q10	-	-	-	2.48	2.81	3.15
CLK → Q10	2.47	2.79	3.12	3.08	3.41	3.75
R → Q9.BUS	-	-	-	3.40	3.90	4.80
CLK → Q9.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q9	-	-	-	2.48	2.81	3.15
CLK → Q9	2.47	2.79	3.12	3.08	3.41	3.75
R → Q8.BUS	-	-	-	3.40	3.90	4.80
CLK → Q8.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q8	-	-	-	2.48	2.81	3.15
CLK → Q8	2.47	2.79	3.12	3.08	3.41	3.75
R → Q7.BUS	-	-	-	3.40	3.90	4.80
CLK → Q7.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q7	-	-	-	2.48	2.81	3.15
CLK → Q7	2.47	2.79	3.12	3.08	3.41	3.75
R → Q6.BUS	-	-	-	3.40	3.90	4.80
CLK → Q6.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q6	-	-	-	2.48	2.81	3.15
CLK → Q6	2.47	2.79	3.12	3.08	3.41	3.75

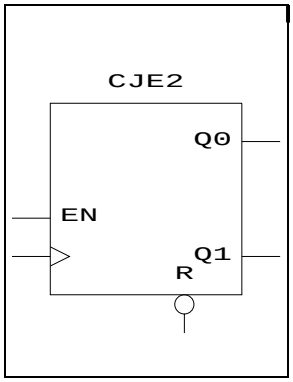
R → Q5.BUS	-	-	-	3.40	3.90	4.80
CLK → Q5.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q5	-	-	-	2.48	2.81	3.15
CLK → Q5	2.47	2.79	3.12	3.08	3.41	3.75
R → Q4.BUS	-	-	-	3.40	3.90	4.80
CLK → Q4.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q4	-	-	-	2.48	2.81	3.15
CLK → Q4	2.47	2.79	3.12	3.08	3.41	3.75
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.48	2.81	3.15
CLK → Q3	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

Schematic



CJE2 - 2-Bit Johnson Counter with Enable

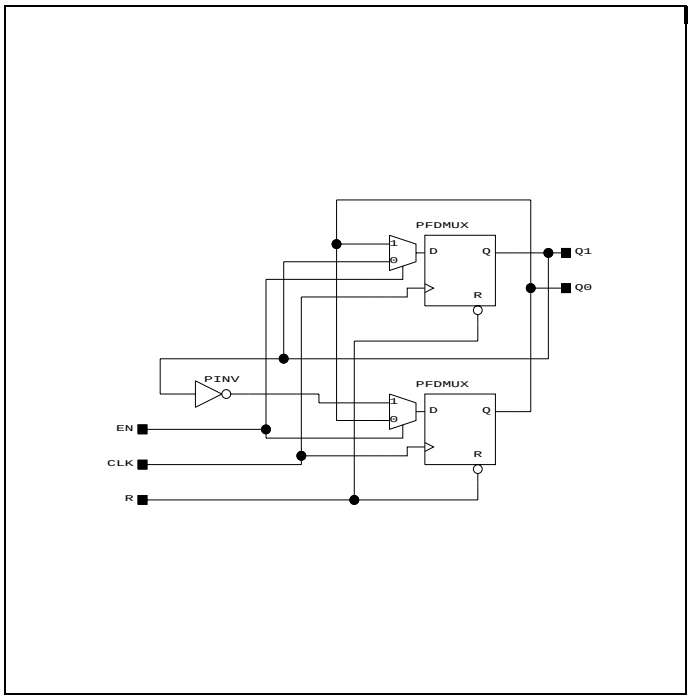
Symbol



Rectangular Area: 3x2 cells

Number of Cells: 6

Schematic



Truth Table

Input			Output	
R	EN	CLK	Q1	Q0
0	x	x	0	0
1	0	x	q1	q0
1	1	r	q0	q1'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q1	-	-	-	1.56	1.82	2.06
CLK → Q1	1.58	1.81	2.04	1.96	2.22	2.46
R → Q0	-	-	-	1.56	1.82	2.06
CLK → Q0	1.58	1.81	2.04	1.96	2.22	2.46

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
EN	3.80	4.00	4.30	0.00	0.00	0.00

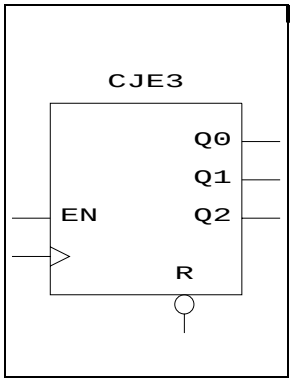
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q1	-	-	-	2.56	2.92	3.31
CLK → Q1	2.54	2.88	3.24	3.16	3.52	3.91
R → Q0	-	-	-	2.56	2.92	3.31
CLK → Q0	2.54	2.88	3.24	3.16	3.52	3.91

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
EN	6.10	6.40	6.70	0.00	0.00	0.00

CJE3 - 3-Bit Johnson Counter with Enable

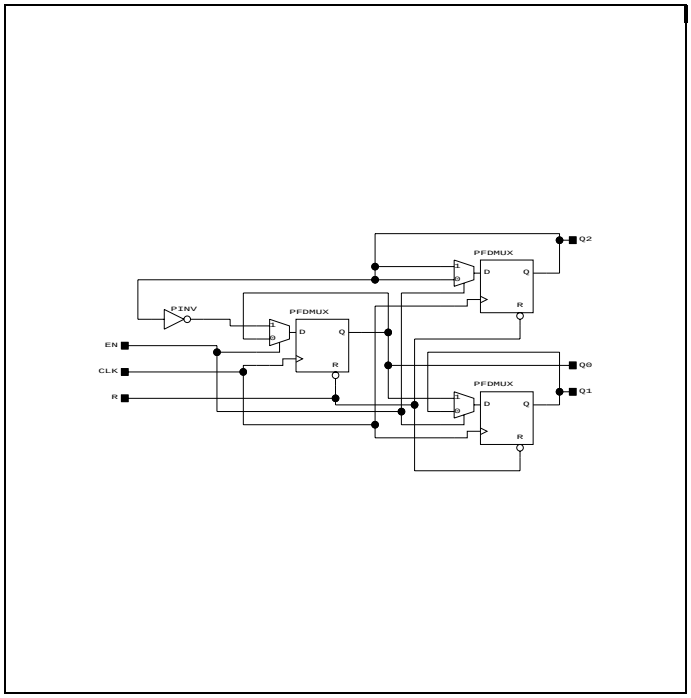
Symbol



Rectangular Area: 4x2 cells

Number of Cells: 7

Schematic



Truth Table

Input			Output		
R	EN	CLK	Q2	Q1	Q0
0	x	x	0	0	0
1	0	x	q2	q1	q0
1	1	r	q1	q0	q2'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q2	-	-	-	1.56	1.82	2.06
CLK → Q2	1.58	1.81	2.04	1.96	2.22	2.46
R → Q1	-	-	-	1.56	1.82	2.06
CLK → Q1	1.58	1.81	2.04	1.96	2.22	2.46
R → Q0	-	-	-	1.56	1.82	2.06
CLK → Q0	1.58	1.81	2.04	1.96	2.22	2.46

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
EN	3.80	4.00	4.30	0.00	0.00	0.00

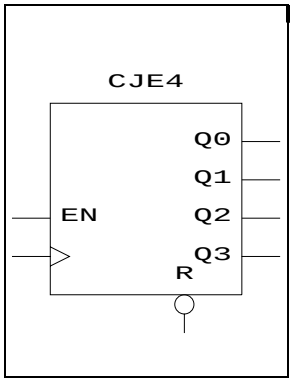
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q2	-	-	-	2.56	2.92	3.31
CLK → Q2	2.54	2.88	3.24	3.16	3.52	3.91
R → Q1	-	-	-	2.56	2.92	3.31
CLK → Q1	2.54	2.88	3.24	3.16	3.52	3.91
R → Q0	-	-	-	2.56	2.92	3.31
CLK → Q0	2.54	2.88	3.24	3.16	3.52	3.91

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
EN	6.10	6.40	6.70	0.00	0.00	0.00

CJE4 - 4-Bit Johnson Counter with Enable

Symbol



Rectangular Area: 4x3 cells

Number of Cells: 10

Truth Table

Input			Output			
R	**EN**	**CLK**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	x	0	0	0	0
1	0	x	q3	q2	q1	q0
1	1	r	q2	q1	q0	q3'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q3	-	-	-	1.56	1.82	2.06
CLK → Q3	1.58	1.81	2.04	1.96	2.22	2.46
R → Q2	-	-	-	1.56	1.82	2.06
CLK → Q2	1.58	1.81	2.04	1.96	2.22	2.46
R → Q1	-	-	-	1.56	1.82	2.06
CLK → Q1	1.58	1.81	2.04	1.96	2.22	2.46
R → Q0	-	-	-	1.56	1.82	2.06
CLK → Q0	1.58	1.81	2.04	1.96	2.22	2.46

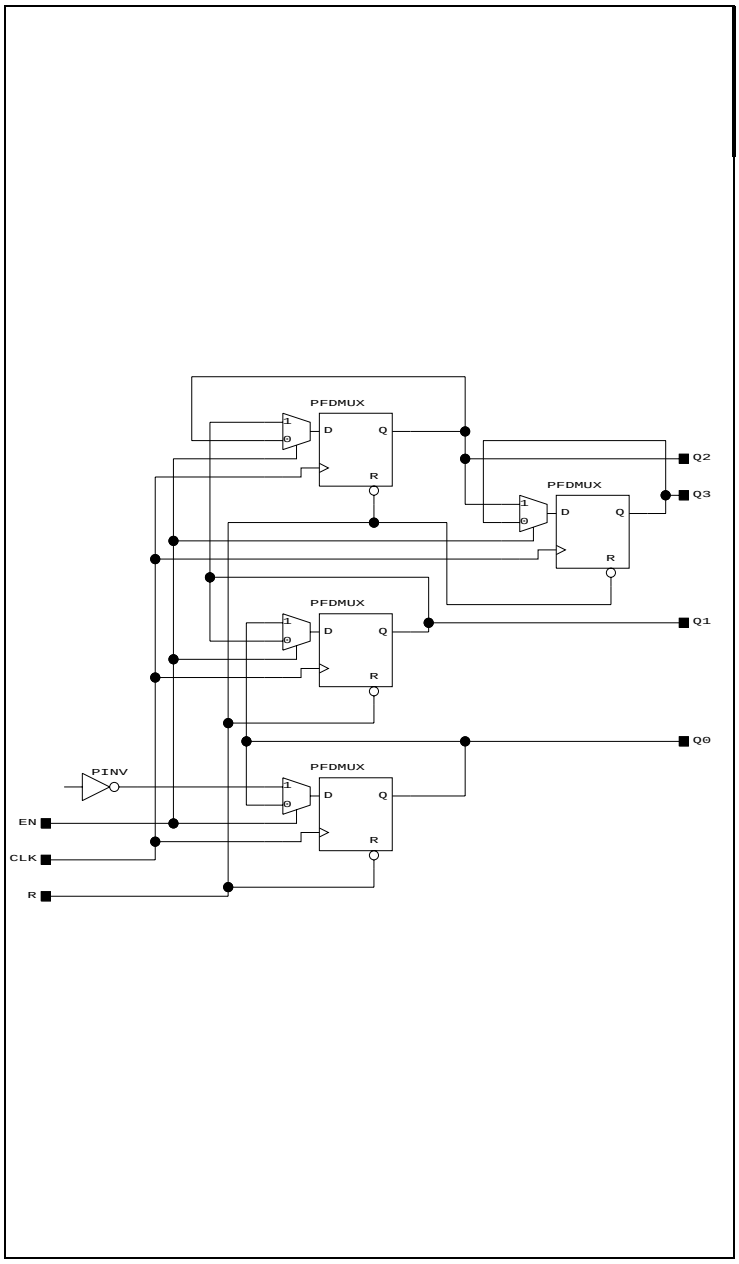
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
EN	3.80	4.00	4.30	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q3	-	-	-	2.56	2.92	3.31
CLK → Q3	2.54	2.88	3.24	3.16	3.52	3.91
R → Q2	-	-	-	2.56	2.92	3.31
CLK → Q2	2.54	2.88	3.24	3.16	3.52	3.91
R → Q1	-	-	-	2.56	2.92	3.31
CLK → Q1	2.54	2.88	3.24	3.16	3.52	3.91
R → Q0	-	-	-	2.56	2.92	3.31
CLK → Q0	2.54	2.88	3.24	3.16	3.52	3.91

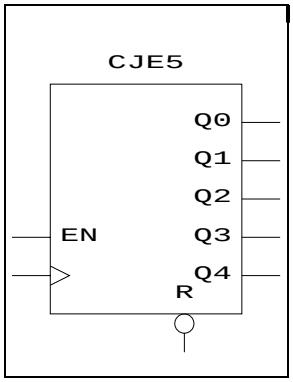
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
EN	6.10	6.40	6.70	0.00	0.00	0.00

Schematic



CJE5 - 5-Bit Johnson Counter with Enable

Symbol



Rectangular Area: 4x3 cells

Number of Cells: 11

Truth Table

Input			Output				
R	**EN**	**CLK**	**Q4**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	x	0	0	0	0	0
1	0	x	q4	q3	q2	q1	q0
1	1	r	q3	q2	q1	q0	q4'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q4	-	-	-	1.56	1.82	2.06
CLK → Q4	1.58	1.81	2.04	1.96	2.22	2.46
R → Q3	-	-	-	1.56	1.82	2.06
CLK → Q3	1.58	1.81	2.04	1.96	2.22	2.46
R → Q2	-	-	-	1.56	1.82	2.06
CLK → Q2	1.58	1.81	2.04	1.96	2.22	2.46
R → Q1	-	-	-	1.56	1.82	2.06
CLK → Q1	1.58	1.81	2.04	1.96	2.22	2.46
R → Q0	-	-	-	1.56	1.82	2.06
CLK → Q0	1.58	1.81	2.04	1.96	2.22	2.46

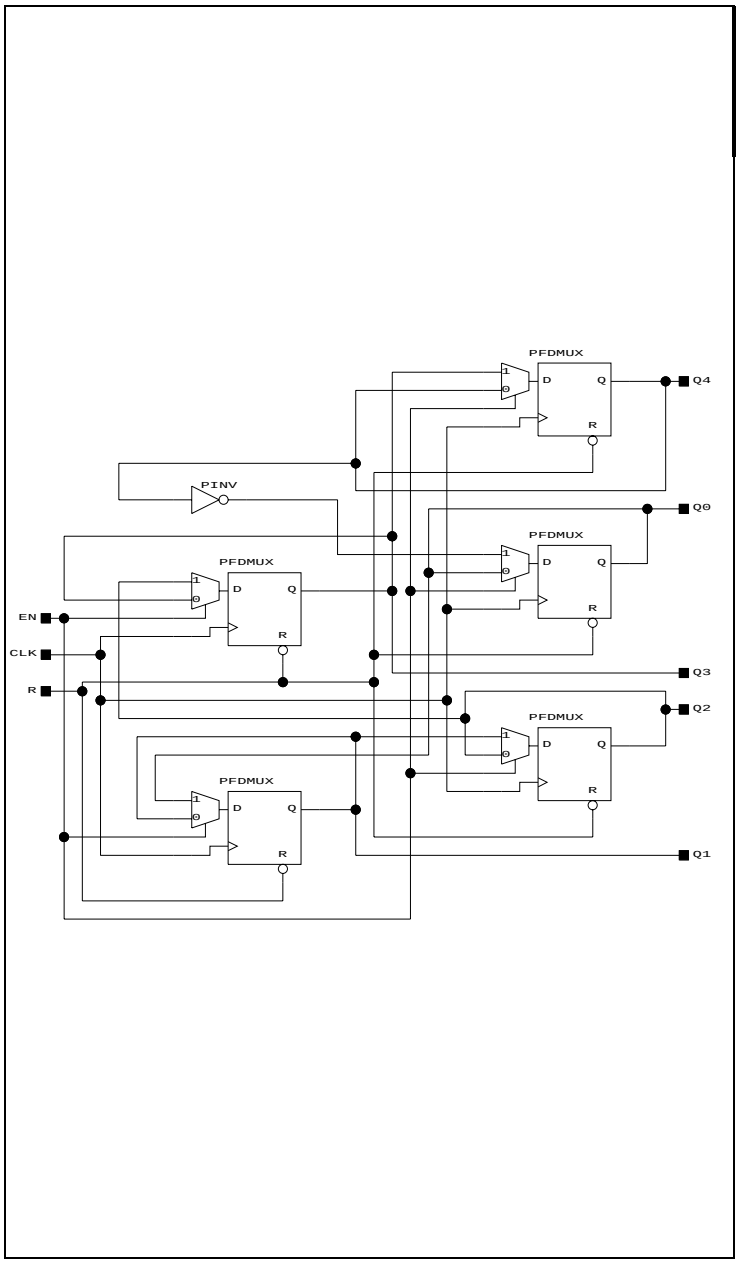
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
EN	3.80	4.00	4.30	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q4	-	-	-	2.56	2.92	3.31
CLK → Q4	2.54	2.88	3.24	3.16	3.52	3.91
R → Q3	-	-	-	2.56	2.92	3.31
CLK → Q3	2.54	2.88	3.24	3.16	3.52	3.91
R → Q2	-	-	-	2.56	2.92	3.31
CLK → Q2	2.54	2.88	3.24	3.16	3.52	3.91
R → Q1	-	-	-	2.56	2.92	3.31
CLK → Q1	2.54	2.88	3.24	3.16	3.52	3.91
R → Q0	-	-	-	2.56	2.92	3.31
CLK → Q0	2.54	2.88	3.24	3.16	3.52	3.91

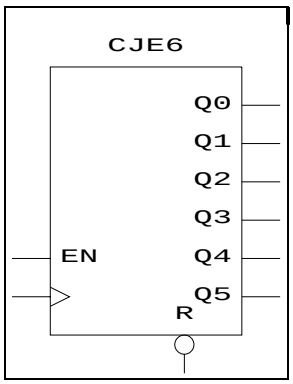
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
EN	6.10	6.40	6.70	0.00	0.00	0.00

Schematic


PFDMUX
PFDMUX
PFDMUX
PFDMUX
PFDMUX
PINV
EN
CLK
R
Q4
Q0
Q3
Q2
Q1
D
Q
R
1
0

CJE6 - 6-Bit Johnson Counter with Enable

Symbol



Rectangular Area: 4x4 cells

Number of Cells: 14

Truth Table

Input			Output					
R	**EN**	**CLK**	**Q5**	**Q4**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	x	0	0	0	0	0	0
1	0	x	q5	q4	q3	q2	q1	q0
1	1	r	q4	q3	q2	q1	q0	q5'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q5	-	-	-	1.56	1.82	2.06
CLK → Q5	1.58	1.81	2.04	1.96	2.22	2.46
R → Q4	-	-	-	1.56	1.82	2.06
CLK → Q4	1.58	1.81	2.04	1.96	2.22	2.46
R → Q3	-	-	-	1.56	1.82	2.06
CLK → Q3	1.58	1.81	2.04	1.96	2.22	2.46
R → Q2	-	-	-	1.56	1.82	2.06
CLK → Q2	1.58	1.81	2.04	1.96	2.22	2.46
R → Q1	-	-	-	1.56	1.82	2.06
CLK → Q1	1.58	1.81	2.04	1.96	2.22	2.46
R → Q0	-	-	-	1.56	1.82	2.06
CLK → Q0	1.58	1.81	2.04	1.96	2.22	2.46

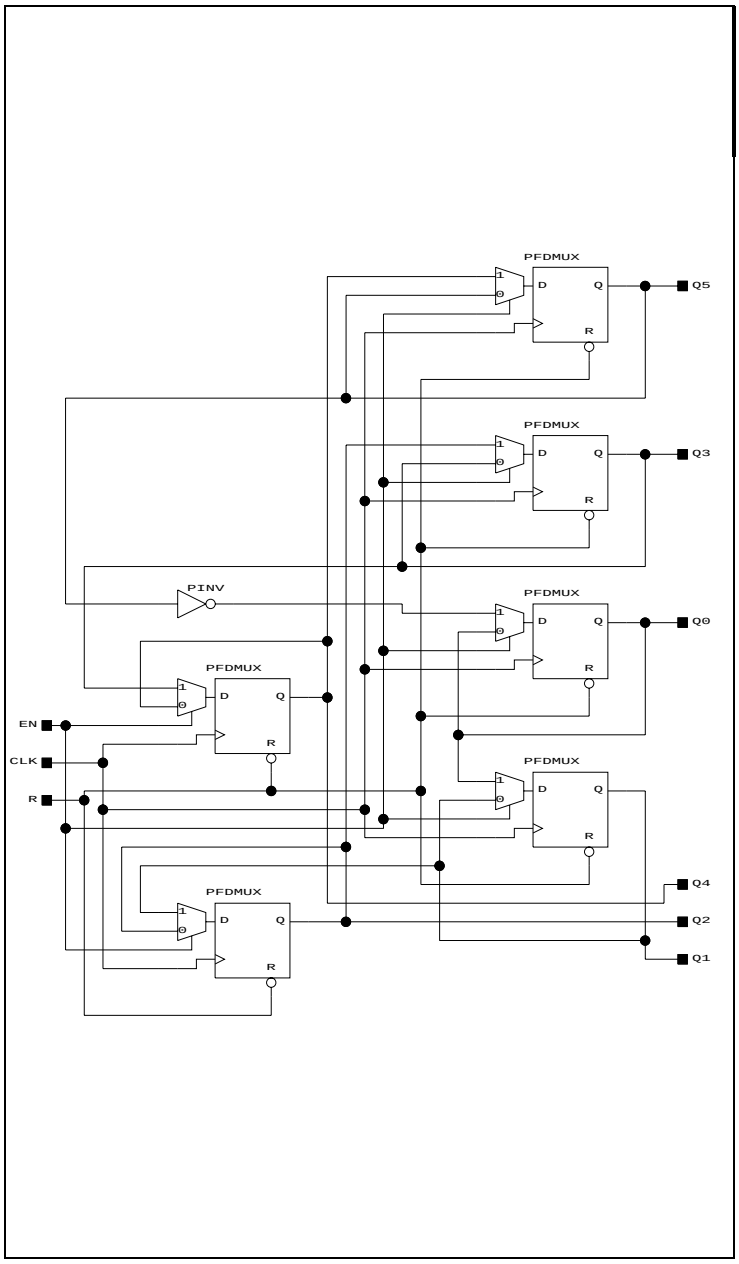
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
EN	3.80	4.00	4.30	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q5	-	-	-	2.56	2.92	3.31
CLK → Q5	2.54	2.88	3.24	3.16	3.52	3.91
R → Q4	-	-	-	2.56	2.92	3.31
CLK → Q4	2.54	2.88	3.24	3.16	3.52	3.91
R → Q3	-	-	-	2.56	2.92	3.31
CLK → Q3	2.54	2.88	3.24	3.16	3.52	3.91
R → Q2	-	-	-	2.56	2.92	3.31
CLK → Q2	2.54	2.88	3.24	3.16	3.52	3.91
R → Q1	-	-	-	2.56	2.92	3.31
CLK → Q1	2.54	2.88	3.24	3.16	3.52	3.91
R → Q0	-	-	-	2.56	2.92	3.31
CLK → Q0	2.54	2.88	3.24	3.16	3.52	3.91

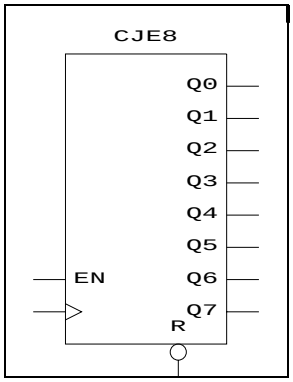
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
EN	6.10	6.40	6.70	0.00	0.00	0.00

Schematic


PFDMUX
PFDMUX
PFDMUX
PFDMUX
PFDMUX
PFDMUX
PINV
EN
CLK
R
Q5
Q3
Q0
Q4
Q2
Q1

CJE8 - 8-Bit Johnson Counter with Enable

Symbol



Rectangular Area: 4x5 cells

Number of Cells: 18

Truth Table

Input			Output					
R	**EN**	**CLK**	**Q7**	**Q6**	**Q5**	**Q4 ...Q2**	**Q1**	**Q0**
0	x	x	0	0	0	0...0	0	0
1	0	x	q7	q6	q5	q4...q2	q1	q0
1	1	r	q6	q5	q4	q3...q1	q0	q7'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q7	-	-	-	1.56	1.82	2.06
CLK → Q7	1.58	1.81	2.04	1.96	2.22	2.46
R → Q6	-	-	-	1.56	1.82	2.06
CLK → Q6	1.58	1.81	2.04	1.96	2.22	2.46
R → Q5	-	-	-	1.56	1.82	2.06
CLK → Q5	1.58	1.81	2.04	1.96	2.22	2.46
R → Q4	-	-	-	1.56	1.82	2.06
CLK → Q4	1.58	1.81	2.04	1.96	2.22	2.46
R → Q3	-	-	-	1.56	1.82	2.06
CLK → Q3	1.58	1.81	2.04	1.96	2.22	2.46
R → Q2	-	-	-	1.56	1.82	2.06
CLK → Q2	1.58	1.81	2.04	1.96	2.22	2.46
R → Q1	-	-	-	1.56	1.82	2.06
CLK → Q1	1.58	1.81	2.04	1.96	2.22	2.46
R → Q0	-	-	-	1.56	1.82	2.06
CLK → Q0	1.58	1.81	2.04	1.96	2.22	2.46

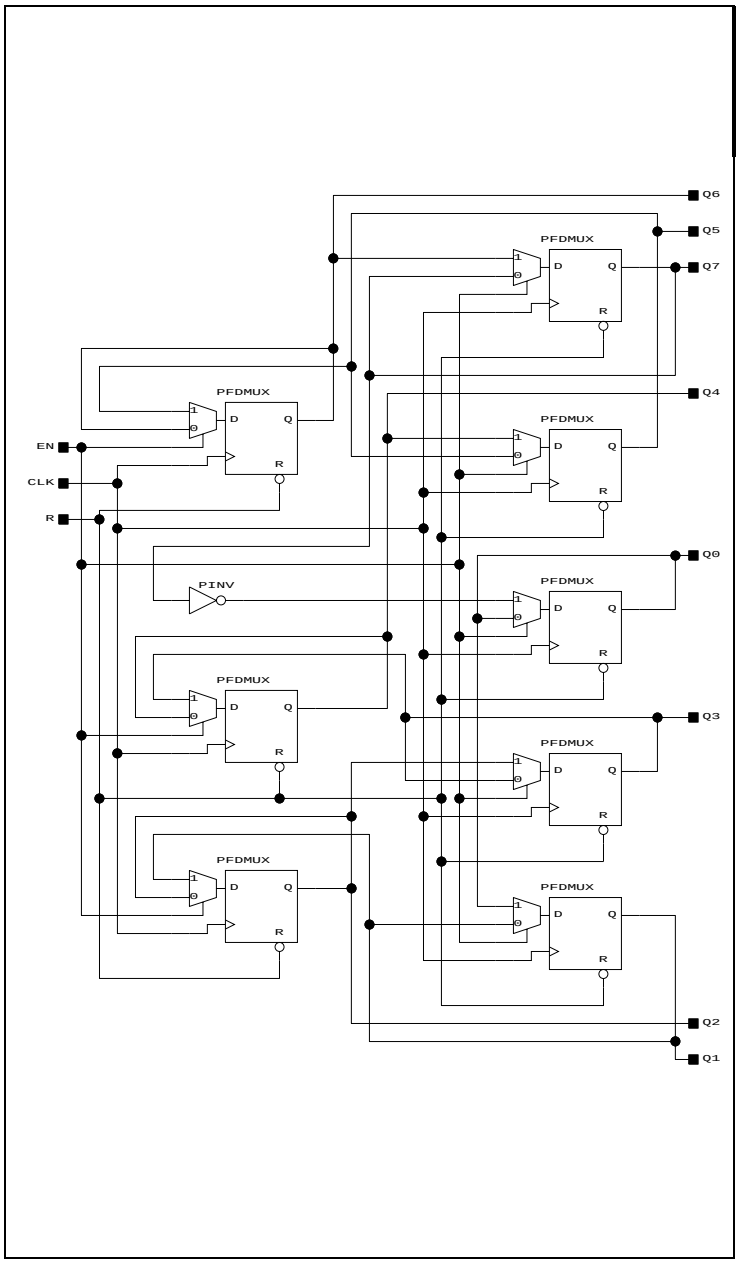
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
EN	3.80	4.00	4.30	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q7	-	-	-	2.56	2.92	3.31
CLK → Q7	2.54	2.88	3.24	3.16	3.52	3.91
R → Q6	-	-	-	2.56	2.92	3.31
CLK → Q6	2.54	2.88	3.24	3.16	3.52	3.91
R → Q5	-	-	-	2.56	2.92	3.31
CLK → Q5	2.54	2.88	3.24	3.16	3.52	3.91
R → Q4	-	-	-	2.56	2.92	3.31
CLK → Q4	2.54	2.88	3.24	3.16	3.52	3.91
R → Q3	-	-	-	2.56	2.92	3.31
CLK → Q3	2.54	2.88	3.24	3.16	3.52	3.91
R → Q2	-	-	-	2.56	2.92	3.31
CLK → Q2	2.54	2.88	3.24	3.16	3.52	3.91
R → Q1	-	-	-	2.56	2.92	3.31
CLK → Q1	2.54	2.88	3.24	3.16	3.52	3.91
R → Q0	-	-	-	2.56	2.92	3.31
CLK → Q0	2.54	2.88	3.24	3.16	3.52	3.91

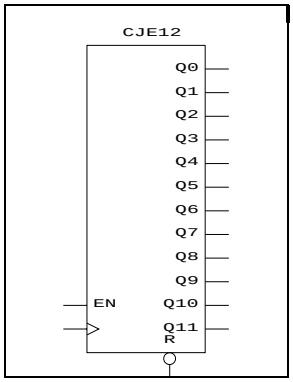
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
EN	6.10	6.40	6.70	0.00	0.00	0.00

Schematic



CJE12 - 12-Bit Johnson Counter with Enable

Symbol



Rectangular Area: 4x7 cells

Number of Cells: 26

Truth Table

Input			Output					
R	**EN**	**CLK**	**Q11**	**Q10**	**Q9**	**Q8...Q2**	**Q1**	**Q0**
0	x	x	0	0	0	0...0	0	0
1	0	x	q11	q10	q9	q8...q2	q1	q0
1	1	r	q10	q9	q8	q7...q1	q0	q11'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q11	-	-	-	1.56	1.82	2.06
CLK → Q11	1.58	1.81	2.04	1.96	2.22	2.46
R → Q10	-	-	-	1.56	1.82	2.06
CLK → Q10	1.58	1.81	2.04	1.96	2.22	2.46
R → Q9	-	-	-	1.56	1.82	2.06
CLK → Q9	1.58	1.81	2.04	1.96	2.22	2.46
R → Q8	-	-	-	1.56	1.82	2.06
CLK → Q8	1.58	1.81	2.04	1.96	2.22	2.46
R → Q7	-	-	-	1.56	1.82	2.06
CLK → Q7	1.58	1.81	2.04	1.96	2.22	2.46
R → Q6	-	-	-	1.56	1.82	2.06
CLK → Q6	1.58	1.81	2.04	1.96	2.22	2.46
R → Q5	-	-	-	1.56	1.82	2.06
CLK → Q5	1.58	1.81	2.04	1.96	2.22	2.46
R → Q4	-	-	-	1.56	1.82	2.06
CLK → Q4	1.58	1.81	2.04	1.96	2.22	2.46
R → Q3	-	-	-	1.56	1.82	2.06
CLK → Q3	1.58	1.81	2.04	1.96	2.22	2.46
R → Q2	-	-	-	1.56	1.82	2.06
CLK → Q2	1.58	1.81	2.04	1.96	2.22	2.46
R →Q1	-	-	-	1.56	1.82	2.06
CLK → Q1	1.58	1.81	2.04	1.96	2.22	2.46
R → Q0	-	-	-	1.56	1.82	2.06
CLK → Q0	1.58	1.81	2.04	1.96	2.22	2.46

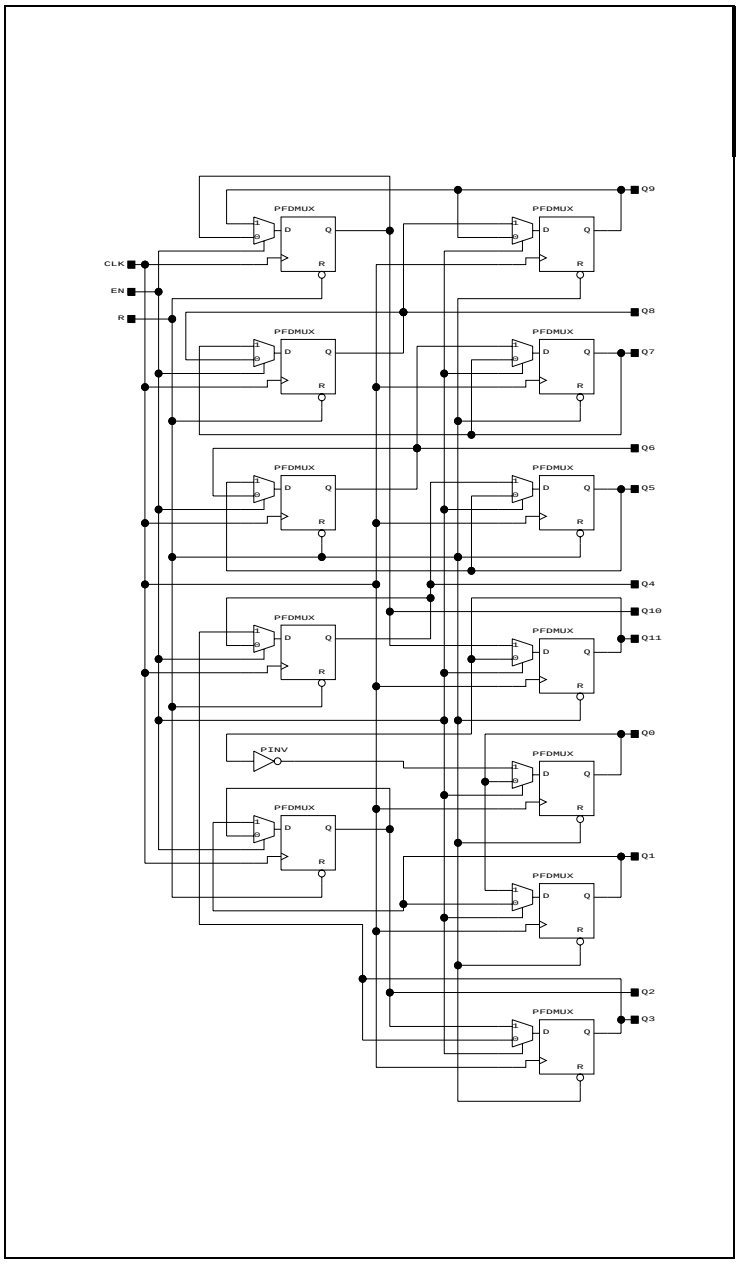
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
EN	3.80	4.00	4.30	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q11	-	-	-	2.56	2.92	3.31
CLK → Q11	2.54	2.88	3.24	3.16	3.52	3.91
R → Q10	-	-	-	2.56	2.92	3.31
CLK → Q10	2.54	2.88	3.24	3.16	3.52	3.91
R → Q9	-	-	-	2.56	2.92	3.31
CLK → Q9	2.54	2.88	3.24	3.16	3.52	3.91
R → Q8	-	-	-	2.56	2.92	3.31
CLK → Q8	2.54	2.88	3.24	3.16	3.52	3.91
R → Q7	-	-	-	2.56	2.92	3.31
CLK → Q7	2.54	2.88	3.24	3.16	3.52	3.91
R → Q6	-	-	-	2.56	2.92	3.31
CLK → Q6	2.54	2.88	3.24	3.16	3.52	3.91
R → Q5	-	-	-	2.56	2.92	3.31
CLK → Q5	2.54	2.88	3.24	3.16	3.52	3.91
R → Q4	-	-	-	2.56	2.92	3.31
CLK → Q4	2.54	2.88	3.24	3.16	3.52	3.91
R → Q3	-	-	-	2.56	2.92	3.31
CLK → Q3	2.54	2.88	3.24	3.16	3.52	3.91
R → Q2	-	-	-	2.56	2.92	3.31
CLK → Q2	2.54	2.88	3.24	3.16	3.52	3.91
R → Q1	-	-	-	2.56	2.92	3.31
CLK → Q1	2.54	2.88	3.24	3.16	3.52	3.91
R → Q0	-	-	-	2.56	2.92	3.31
CLK → Q0	2.54	2.88	3.24	3.16	3.52	3.91

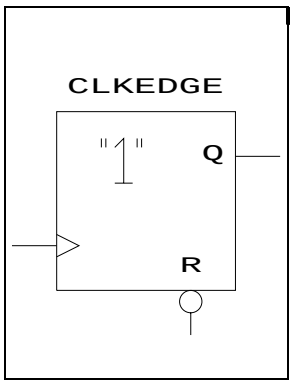
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
EN	6.10	6.40	6.70	0.00	0.00	0.00

Schematic



CLKEDGE - Clock Edge Detect

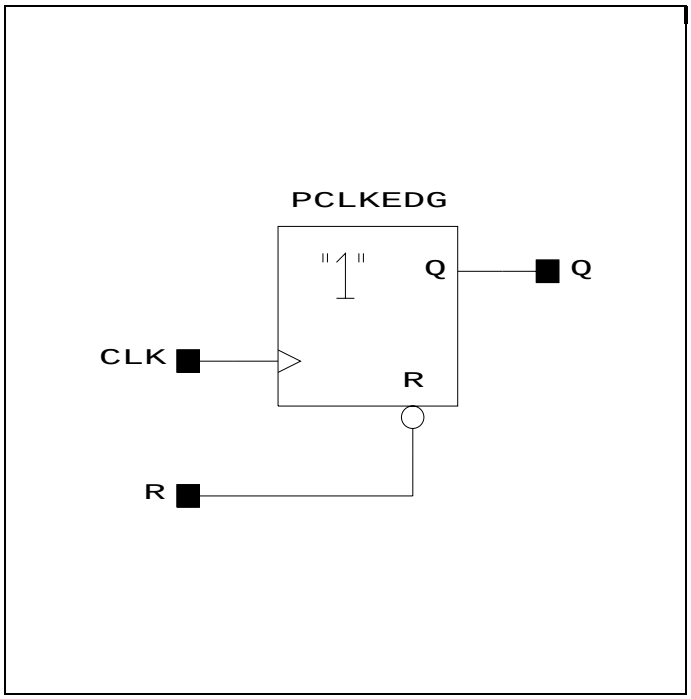
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input R	CLK	Output Q
0	x	0
1	r	1

Switching Speeds for -2ns Parts

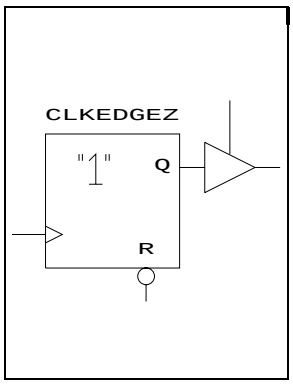
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20
R → Q	0.00	0.00	0.00	1.40	1.60	1.80
CLK → Q.BUS	1.80	2.10	2.40	1.80	2.00	2.20
R → Q.BUS	0.40	0.50	0.60	1.40	1.60	1.80

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60
R → Q	0.00	0.00	0.00	2.40	2.70	3.00
CLK → Q.BUS	3.10	3.60	4.40	3.00	3.30	3.60
R → Q.BUS	0.70	0.90	1.40	2.40	2.70	3.00

CLKEDGEZ - Clock Edge Detect Q=1 on Rise (Z)

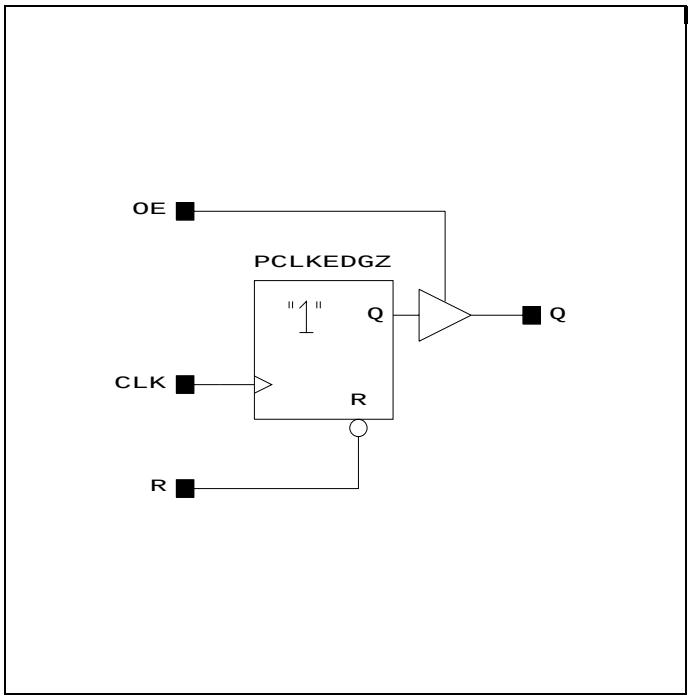
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input R	CLK	OE	Output Q
0	x	1	0
1	x	0	z
1	x	1	0
1	r	1	1

Switching Speeds for -2ns Parts

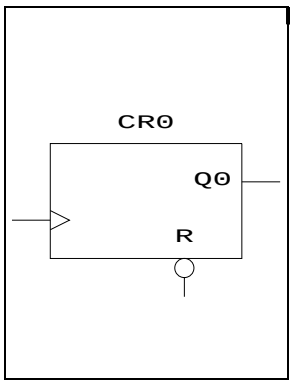
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	2.00	2.30	2.60	2.30	2.60	2.90
OE → Q	1.30	1.40	1.50	1.20	1.30	1.40
R → Q	0.60	0.70	0.80	1.90	2.20	2.50

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	3.50	3.90	4.30	3.90	4.30	4.70
OE → Q	1.90	2.10	2.30	1.80	2.00	2.20
R → Q	1.10	1.20	1.30	3.30	3.70	4.10

CR0 - 0-Bit Ripple-Carry Counter

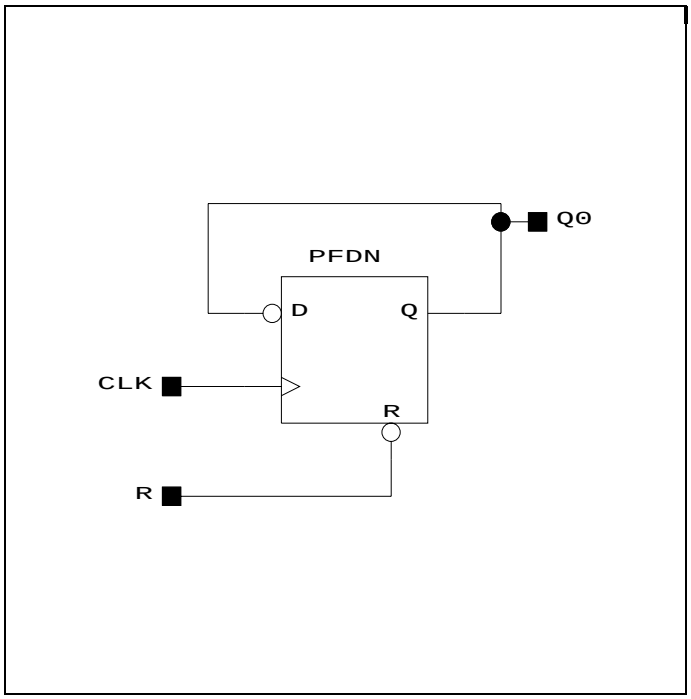
Symbol



Rectangular Area: 2x1 cells

Number of Cells: 2

Schematic



Truth Table

Input R	CLK	Output Q0
0	x	0
1	x	q0
1	r	q0'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max

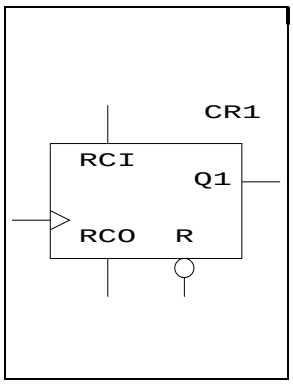
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max

CR1 - 1-Bit Ripple-Carry Counter

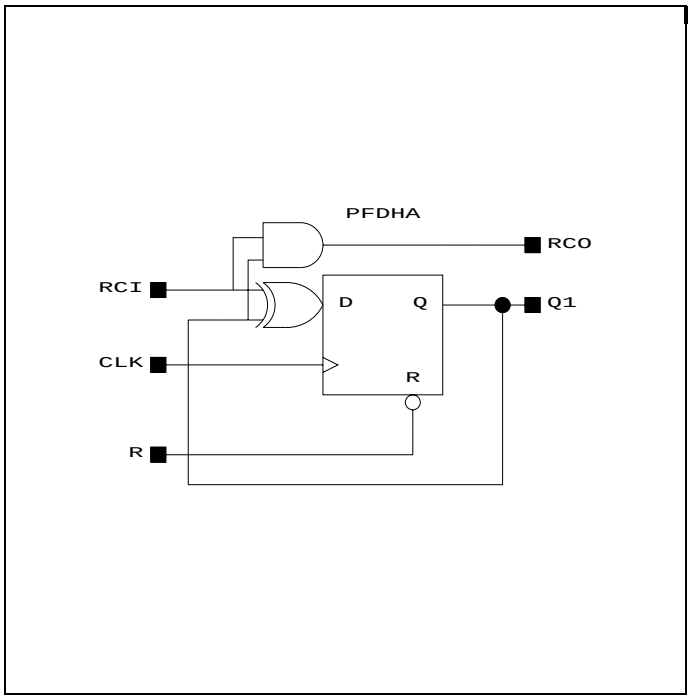
Symbol



Rectangular Area: 2x1 cells

Number of Cells: 2

Schematic



Truth Table

Input			Output	
R	CLK	RCI	Q1	RCO
0	x	x	0	0
1	r	0	q1	0
1	r	1	q1'	q1
1	x	1	q1	q1

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
RCI → RCO	0.60	1.20	1.90	0.80	1.50	2.20
R → RCO	-	-	-	2.75	3.99	5.32
CLK → RCO	2.57	3.69	5.01	3.15	4.39	5.72

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RCI	2.10	2.10	2.10	0.00	0.00	0.00

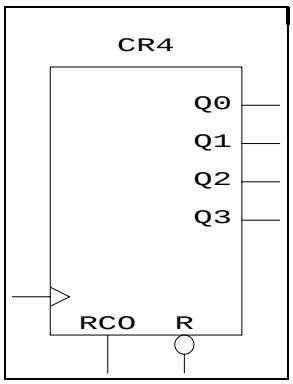
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
RCI → RCO	1.70	2.10	2.90	1.80	2.30	3.00
R → RCO	-	-	-	5.35	6.40	7.89
CLK → RCO	5.24	6.28	7.85	5.95	7.00	8.49

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
RCI	3.50	3.50	3.50	0.00	0.00	0.00

CR4 - 4-Bit Ripple-Carry Counter

Symbol



Rectangular Area: 2x4cells

Number of Cells: 8

Truth Table

Input		Output				
R	**CLK**	**Q3**	**Q2**	**Q1**	**Q0**	**RCO**
0	x	x	0	0	0	0
1	x	q3	q2	q1	q0	0
1	r	present state + 1				q3*q2*q1*q0
1	x	1	1	1	1	1

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → RCO	-	-	-	2.75	5.59	9.96
CLK → RCO	2.57	4.98	9.01	3.15	5.99	10.36
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.48	1.71	1.93
CLK → Q3	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.56	1.82	2.06
CLK → Q0	1.58	1.81	2.04	1.96	2.22	2.46

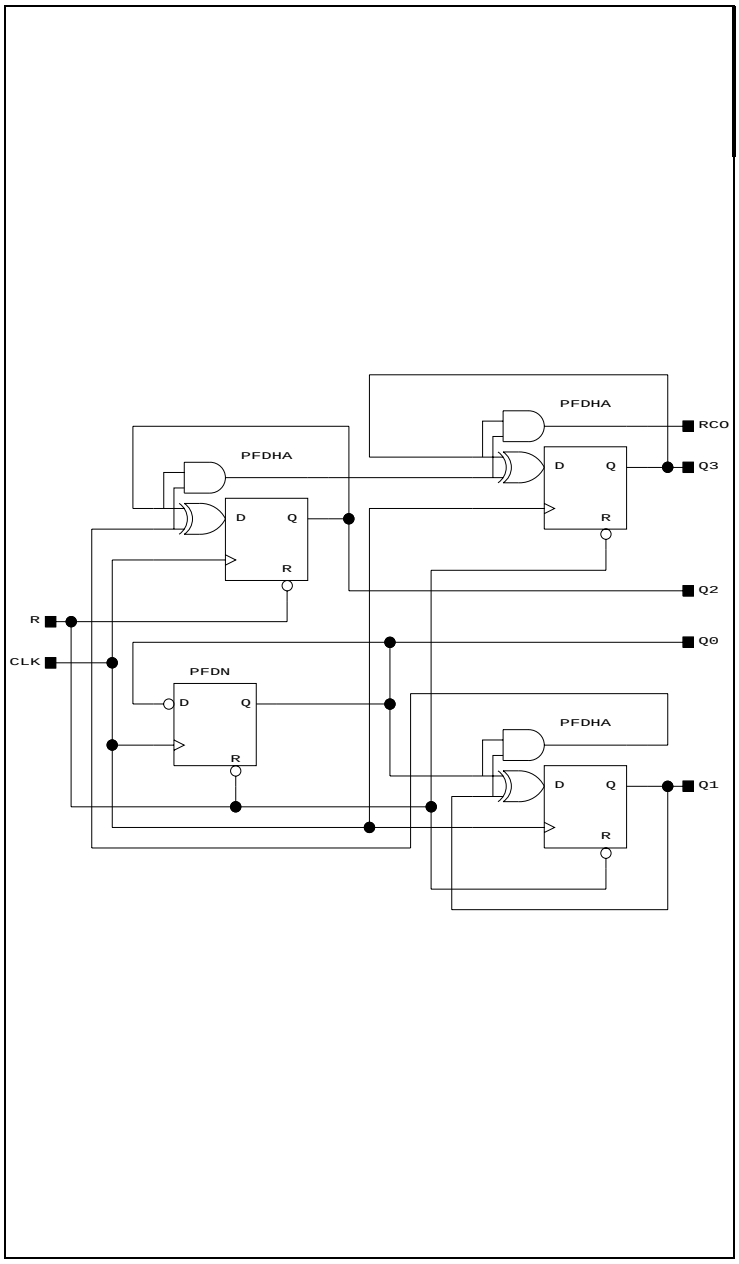
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → RCO	-	-	-	5.35	8.81	14.20
CLK → RCO	5.24	8.47	13.89	5.95	9.41	14.80
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.48	2.81	3.15
CLK → Q3	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.56	2.92	3.31
CLK → Q0	2.54	2.88	3.24	3.16	3.52	3.91

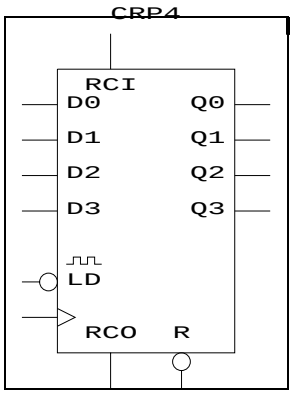
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max

Schematic



CRP4 - 4-Bit Ripple-Carry Counter w/ Parallel Load

Symbol



Rectangular Area: 2x4cells

Number of Cells: 8

Truth Table

Input					Output	
R	**RCI**	**CLK**	**LD**	**D3...D0**	**Q3...Q0**	**RCO**
0	x	x	x	x...x	0...0	0
1	0	x	x	x...x	q3...q0	0
1	0	r	0	d3...d0	d3...d0	0
1	1	x	1	x...x	present state	q3*q2*q1*q0
1	1	r	0	d3...d0	d3...d0+1	q3*q2*q1*q0

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.48	1.71	1.93
CLK → Q3	1.49	1.71	1.92	1.88	2.11	2.33
D0 → RCO	3.51	6.75	10.29	4.24	7.80	11.35
D1 → RCO	2.83	5.46	8.29	3.35	6.19	9.03
D2 → RCO	2.15	4.17	6.29	2.46	4.59	6.71
D3 → RCO	1.47	2.88	4.29	1.57	2.98	4.39
LD → RCO	1.67	5.12	11.09	1.87	5.99	12.45
RCI → RCO	2.64	5.07	7.90	3.47	6.32	9.16
R → RCO	-	-	-	3.15	7.20	13.38
CLK → RCO	2.96	6.33	12.01	3.55	7.60	13.78

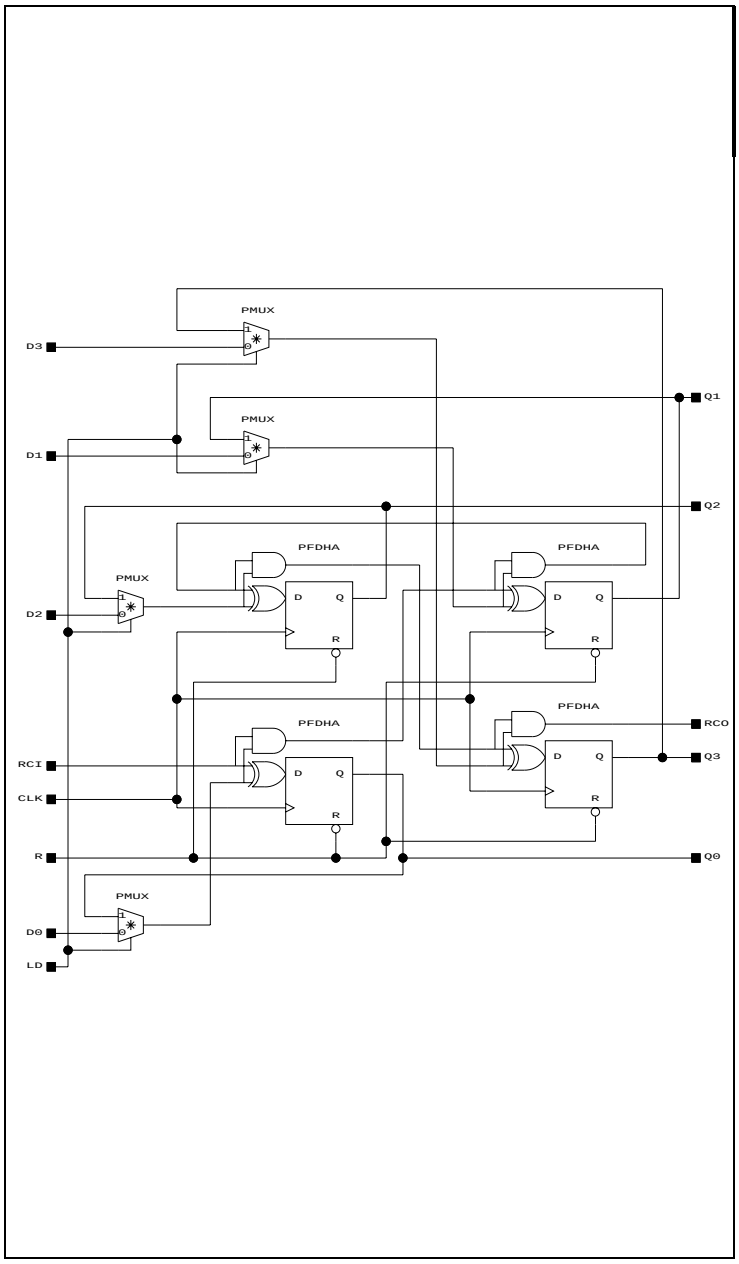
Pin	Setup			Hold		
	Min	Typ	Max	Min	Typ	Max
D0	5.54	8.40	11.25	0.77	0.77	0.77
D1	4.65	6.79	8.93	0.77	0.77	0.77
D2	3.76	5.18	6.61	0.77	0.77	0.77
D3	2.97	3.78	4.49	0.77	0.77	0.77
LD	5.84	8.99	12.35	1.07	1.07	1.07
RCI	4.77	6.91	9.06	0.00	0.00	0.00

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R -> Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.48	2.81	3.15
CLK → Q3	2.47	2.79	3.12	3.08	3.41	3.75
D0 → RCO	8.99	11.06	15.17	9.51	12.11	15.88
D1 → RCO	7.22	8.87	12.15	7.62	9.70	12.73
D2 → RCO	5.44	6.68	9.13	5.74	7.29	9.58
D3 → RCO	3.67	4.49	6.11	3.86	4.88	6.42
LD → RCO	4.67	8.88	16.67	5.36	10.29	18.28
RCI → RCO	7.02	8.67	11.96	7.44	9.53	12.46
R → RCO	-	-	-	6.84	11.91	19.94
CLK → RCO	6.04	10.57	18.29	7.44	12.51	20.54

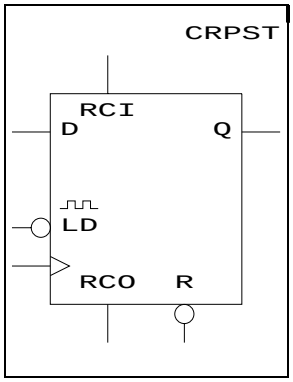
Pin	Setup			Hold		
	Min	Typ	Max	Min	Typ	Max
D0	11.21	13.31	16.38	1.97	1.97	1.97
D1	9.32	10.90	13.23	1.97	1.97	1.97
D2	7.44	8.49	10.08	1.97	1.97	1.97
D3	5.56	6.08	6.92	1.97	1.97	1.97
LD	12.71	15.11	18.78	2.97	2.97	2.97
RCI	9.14	10.73	12.96	0.00	0.00	0.00

Schematic


PMUX
D3
PMUX
D1
PMUX
D2
PMUX
D0
LD
PFDHA
PFDHA
PFDHA
PFDHA
D
Q
R
RCI
CLK
R
Q1
Q2
RCO
Q3
Q0

CRPST - Bit Stage Ripple-Carry Counter w/ Parallel Load

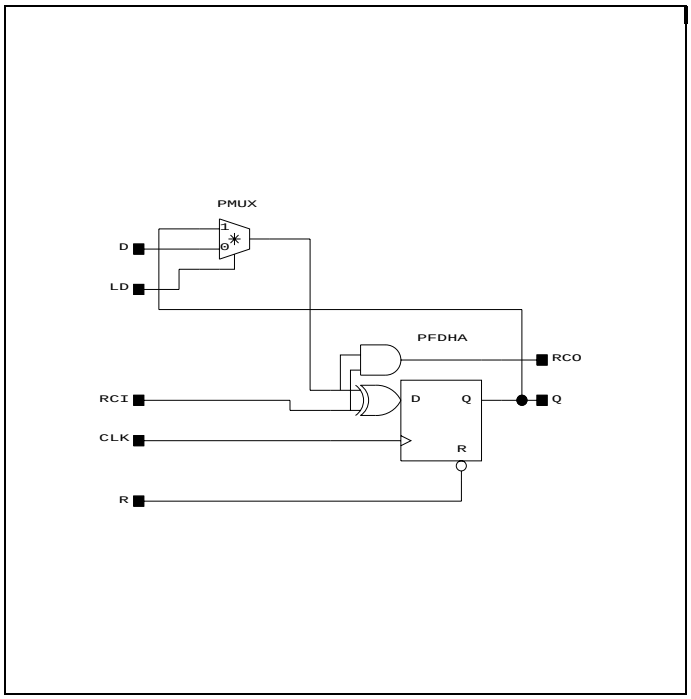
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input					Output	
R	CLK	LD	RCI	D	Q	RCO
0	x	x	x	x	0	0
1	x	x	x	x	q	rco
1	r	0	x	d	d	rci*d
1	r	1	0	x	q	0
1	r	1	1	x	q'	q'
1	x	1	1	x	q	q

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
RCI → RCO	0.60	1.20	1.90	0.80	1.50	2.20
D → RCO	1.47	2.88	4.29	1.57	2.98	4.39
LD → RCO	1.67	3.18	5.09	1.87	3.58	5.49
R → RCO	-	-	-	3.15	4.79	6.42
CLK → RCO	2.96	4.39	6.01	3.55	5.19	6.82
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.48	1.71	1.93
CLK → Q	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RCI	2.10	2.10	2.10	0.00	0.00	0.00
D	2.97	3.78	4.49	0.77	0.77	0.77
LD	3.17	4.18	5.39	1.07	1.07	1.07

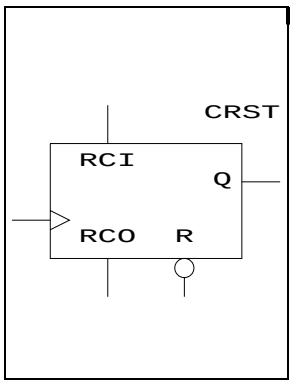
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
RCI → RCO	1.70	2.10	2.90	1.80	2.30	3.00
D → RCO	3.67	4.49	6.11	3.86	4.88	6.42
LD → RCO	4.67	5.59	7.61	5.36	6.68	8.82
R → RCO	-	-	-	6.84	8.29	10.48
CLK → RCO	6.04	7.28	9.23	7.44	8.89	11.08
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.48	2.81	3.15
CLK → Q	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RCI	3.50	3.50	3.50	0.00	0.00	0.00
D	5.56	6.08	6.92	1.97	1.97	1.97
LD	7.06	7.88	9.32	2.97	2.97	2.97

CRST - Bit Stage Ripple-Carry Counter

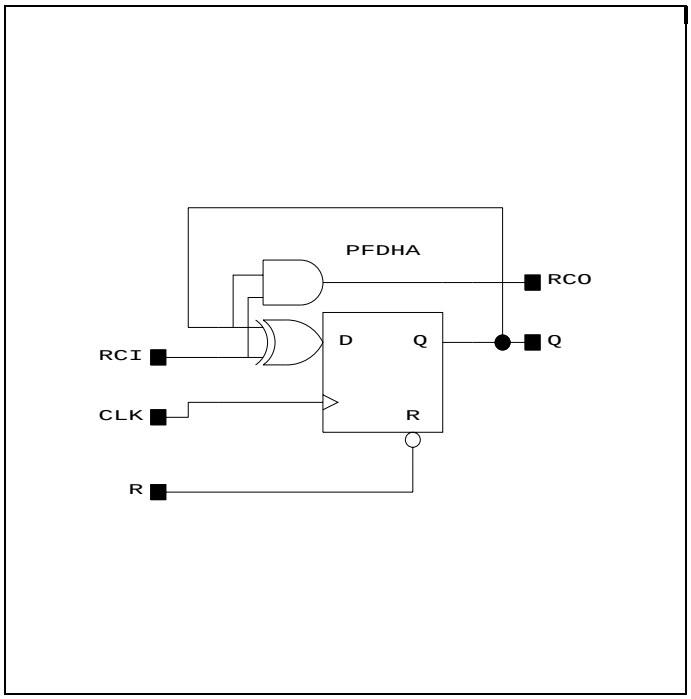
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input			Output	
R	CLK	RCI	Q	RCO
0	x	x	0	0
1	x	0	q	0
1	r	1	q'	q*rci

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.48	1.71	1.93
CLK → Q	1.49	1.71	1.92	1.88	2.11	2.33
RCI → RCO	0.60	1.20	1.90	0.80	1.50	2.20
R → RCO	-	-	-	2.75	3.99	5.32
CLK → RCO	2.57	3.69	5.02	3.15	4.39	5.72

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RCI	2.10	2.10	2.10	0.00	0.00	0.00

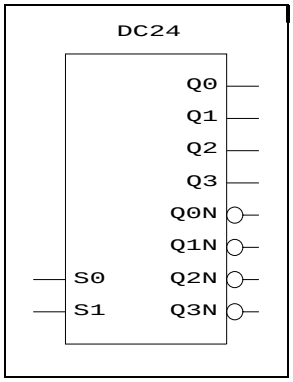
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.48	2.81	3.15
CLK → Q	2.47	2.79	3.12	3.08	3.41	3.75
RCI → RCO	1.70	2.10	2.90	1.80	2.30	3.00
R → RCO	-	-	-	5.35	6.40	7.99
CLK → RCO	5.24	6.28	7.84	5.95	7.00	8.59

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
RCI	3.50	3.50	3.50	0.00	0.00	0.00

DC24 - 2-4 Decoder Active High/Low

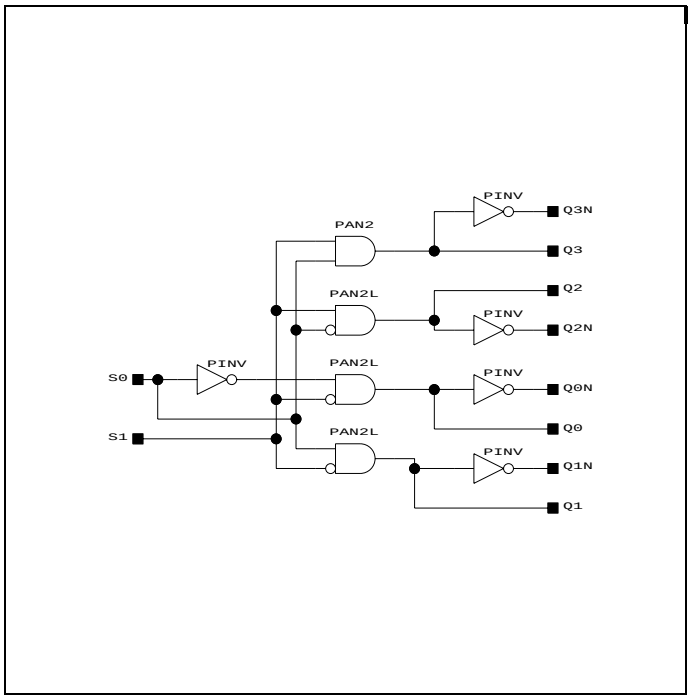
Symbol



Rectangular Area: 2x5cells

Number of Cells: 9

Schematic



Truth Table

Input		Output							
S1	S0	Q3	Q2	Q1	Q0	Q3N	Q2N	Q1N	Q0N
0	0	0	0	0	1	1	1	1	0
0	1	0	0	1	0	1	1	0	1
1	0	0	1	0	0	1	0	1	1
1	1	1	0	0	0	0	1	1	1

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S1 → Q0	0.88	1.19	1.59	0.97	1.38	1.89
S0 → Q0	1.26	1.97	2.78	1.44	2.16	2.98
S1 → Q0N.BUS	2.17	3.48	4.79	2.08	3.18	4.39
S0 → Q0N.BUS	2.64	4.26	5.88	2.46	3.97	5.58
S1 → Q0N	1.77	2.98	4.19	1.58	2.59	3.69
S0 → Q0N	2.24	3.76	5.28	1.96	3.37	4.88
S1 → Q1	0.88	1.19	1.59	0.97	1.38	1.89
S0 → Q1	1.04	1.65	2.47	1.11	1.74	2.57
S1 → Q2	0.96	1.57	2.38	1.04	1.66	2.48
S0 → Q2	0.88	1.19	1.59	0.97	1.38	1.89
S1 → Q3	0.78	1.29	2.00	0.99	1.61	2.32
S0 → Q3	1.34	2.16	3.28	1.53	2.46	3.60
S1 → Q1N.BUS	2.17	3.48	4.79	2.08	3.18	4.39
S0 → Q1N.BUS	2.31	3.84	5.47	2.24	3.65	5.27
S1 → Q1N	1.77	2.98	4.19	1.58	2.59	3.69
S0 → Q1N	1.91	3.34	4.87	1.74	3.05	4.57

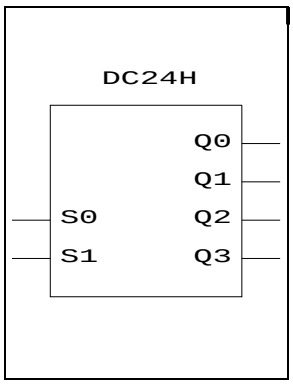
S1 → Q2N.BUS	2.24	3.76	5.38	2.16	3.57	5.18
S0 → Q2N.BUS	2.17	3.48	4.79	2.08	3.18	4.39
S1 → Q2N	1.84	3.26	4.78	1.66	2.97	4.48
S0 → Q2N	1.77	2.98	4.19	1.58	2.59	3.69
S1 → Q3N.BUS	2.19	3.70	5.22	1.98	3.29	4.80
S0 → Q3N.BUS	2.73	4.56	6.50	2.54	4.16	6.08
S1 → Q3N	1.79	3.20	4.62	1.48	2.69	4.10
S0 → Q3N	2.33	4.07	5.90	2.04	3.56	5.38

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
S1 → Q0	1.57	1.99	2.53	1.77	2.09	2.63
S0 → Q0	2.64	3.28	4.25	2.84	3.38	4.26
S1 → Q0N.BUS	4.37	5.29	7.13	4.57	5.69	7.63
S0 → Q0N.BUS	5.44	6.58	8.76	5.64	6.98	9.35
S1 → Q0N	3.67	4.39	5.73	3.57	4.49	5.83
S0 → Q0N	4.74	5.68	7.36	4.64	5.78	7.55
S1 → Q1	1.57	1.99	2.53	1.77	2.09	2.63
S0 → Q1	2.22	2.87	3.80	2.52	3.07	4.10
S1 → Q2	2.14	2.78	3.66	2.44	2.98	3.96
S0 → Q2	1.57	1.99	2.53	1.77	2.09	2.63
S1 → Q3	1.77	2.19	2.92	2.18	2.71	3.45
S0 → Q3	2.92	3.67	4.88	3.22	4.09	5.42
S1 → Q1N.BUS	4.37	5.29	7.13	4.57	5.69	7.63
S0 → Q1N.BUS	5.12	6.27	8.60	5.22	6.57	8.90
S1 → Q1N	3.67	4.39	5.73	3.57	4.49	5.83
S0 → Q1N	4.42	5.37	7.20	4.22	5.37	7.10
S1 → Q2N.BUS	5.04	6.18	8.46	5.14	6.48	8.76
S0 → Q2N.BUS	4.37	5.29	7.13	4.57	5.69	7.63
S1 → Q2N	4.34	5.28	7.06	4.14	5.28	6.96
S0 → Q2N	3.67	4.39	5.73	3.57	4.49	5.83
S1 → Q3N.BUS	4.78	5.91	7.95	4.77	5.89	8.02
S0 → Q3N.BUS	5.82	7.29	9.92	5.92	7.37	9.98
S1 → Q3N	4.08	5.01	6.55	3.77	4.69	6.22
S0 → Q3N	5.12	6.39	8.52	4.92	6.17	8.18

DC24H - 2-4 Decoder Active High

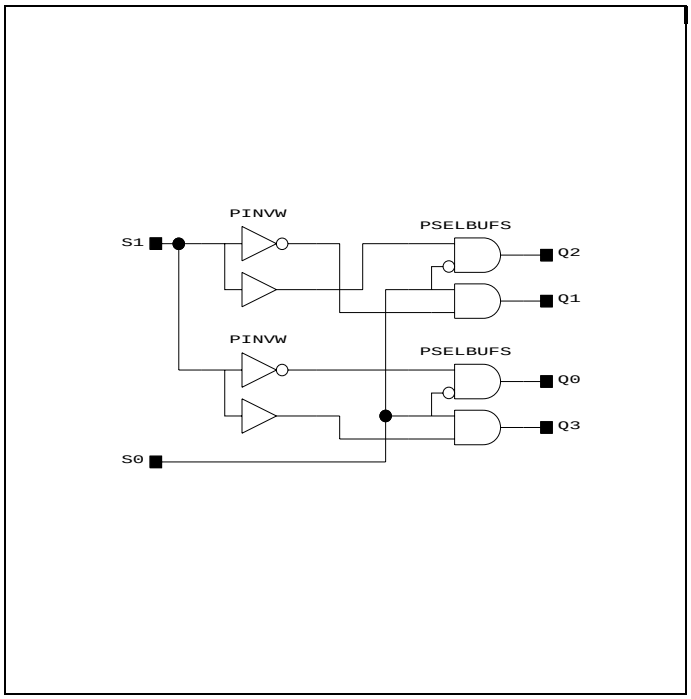
Symbol



Rectangular Area: 2x2cells

Number of Cells: 4

Schematic



Truth Table

Input		Output			
S1	S0	Q3	Q2	Q1	Q0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Switching Speeds for -2ns Parts

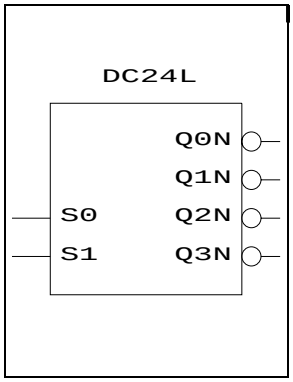
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
S0 → Q0	0.80	1.10	1.50	0.90	1.30	1.80
S1 → Q0	1.18	1.88	2.69	1.37	2.08	2.89
S0 → Q1	0.40	0.70	1.10	0.50	0.80	1.20
S1 → Q1	1.18	1.88	2.69	1.37	2.08	2.89
S0 → Q2	0.80	1.10	1.50	0.90	1.30	1.80
S1 → Q2	0.88	1.48	2.29	0.97	1.58	2.39
S0 → Q3	0.40	0.70	1.10	0.50	0.80	1.20
S1 → Q3	0.88	1.49	2.30	0.97	1.68	2.39

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S0 → Q0	1.50	1.80	2.40	1.60	2.00	2.50
S1 → Q0	2.57	3.09	4.12	2.67	3.29	4.13
S0 → Q1	1.00	1.30	1.70	1.40	1.60	2.10
S1 → Q1	2.67	3.29	4.23	2.77	3.29	4.33
S0 → Q2	1.50	1.80	2.40	1.60	2.00	2.50
S1 → Q2	2.07	2.59	3.53	2.27	2.89	3.83
S0 → Q3	1.00	1.30	1.70	1.40	1.60	2.10
S1 → Q3	2.07	2.69	3.52	2.37	2.89	3.93

DC24L - 2-4 Decoder Active Low

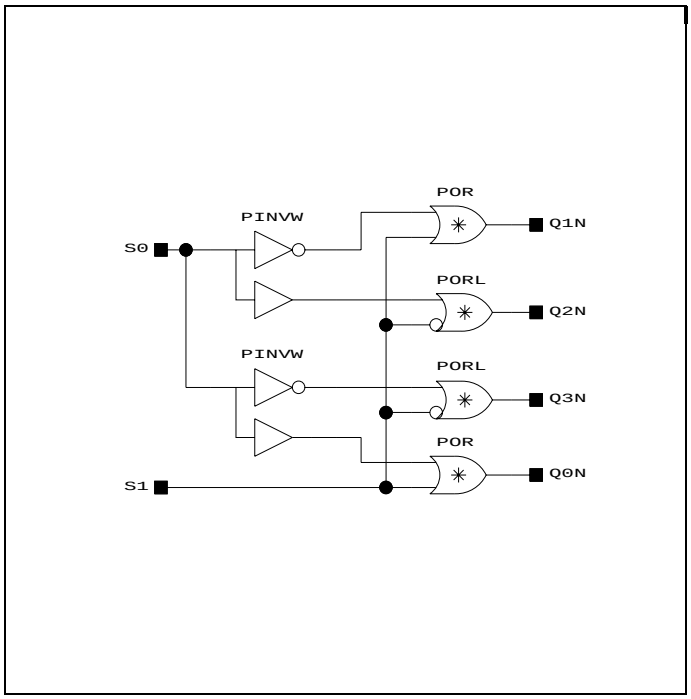
Symbol



Rectangular Area: 1x6cells

Number of Cells: 6

Schematic



Truth Table

Input		Output			
S1	S0	Q3N	Q2N	Q1N	Q0N
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	1

Switching Speeds for -2ns Parts

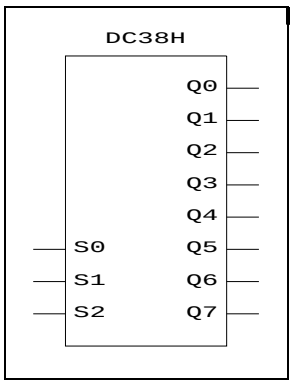
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S1 → Q3N	0.80	1.40	2.10	0.90	1.60	2.30
S0 → Q3N	1.58	2.59	3.69	1.77	2.88	3.99
S1 → Q2N	0.80	1.40	2.10	0.90	1.60	2.30
S0 → Q2N	1.28	2.19	3.30	1.37	2.48	3.49
S1 → Q1N	0.80	1.40	2.10	0.90	1.60	2.30
S0 → Q1N	1.58	2.59	3.69	1.77	2.88	3.99
S1 → Q0N	0.80	1.40	2.10	0.90	1.60	2.30
S0 → Q0N	1.28	2.18	3.29	1.37	2.38	3.49

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S1 → Q3N	1.80	2.30	3.10	2.90	3.50	4.60
S0 → Q3N	3.47	4.29	5.63	4.27	5.19	6.83
S1 → Q2N	1.80	2.30	3.10	2.90	3.50	4.60
S0 → Q2N	2.87	3.69	4.92	3.87	4.79	6.43
S1 → Q1N	1.80	2.30	3.10	2.90	3.50	4.60
S0 → Q1N	3.37	4.19	5.52	4.27	5.19	6.73
S1 → Q0N	1.80	2.30	3.10	2.90	3.50	4.60
S0 → Q0N	2.87	3.69	4.93	3.87	4.79	6.43

DC38H - 3-8 Decoder Active High

Symbol



Rectangular Area: 3x8cells

Number of Cells: 20

Truth Table

Input			Output							
S2	**S1**	**S0**	**Q7**	**Q6**	**Q5**	**Q4**	**Q3**	**Q2**	**Q1**	**Q0**
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

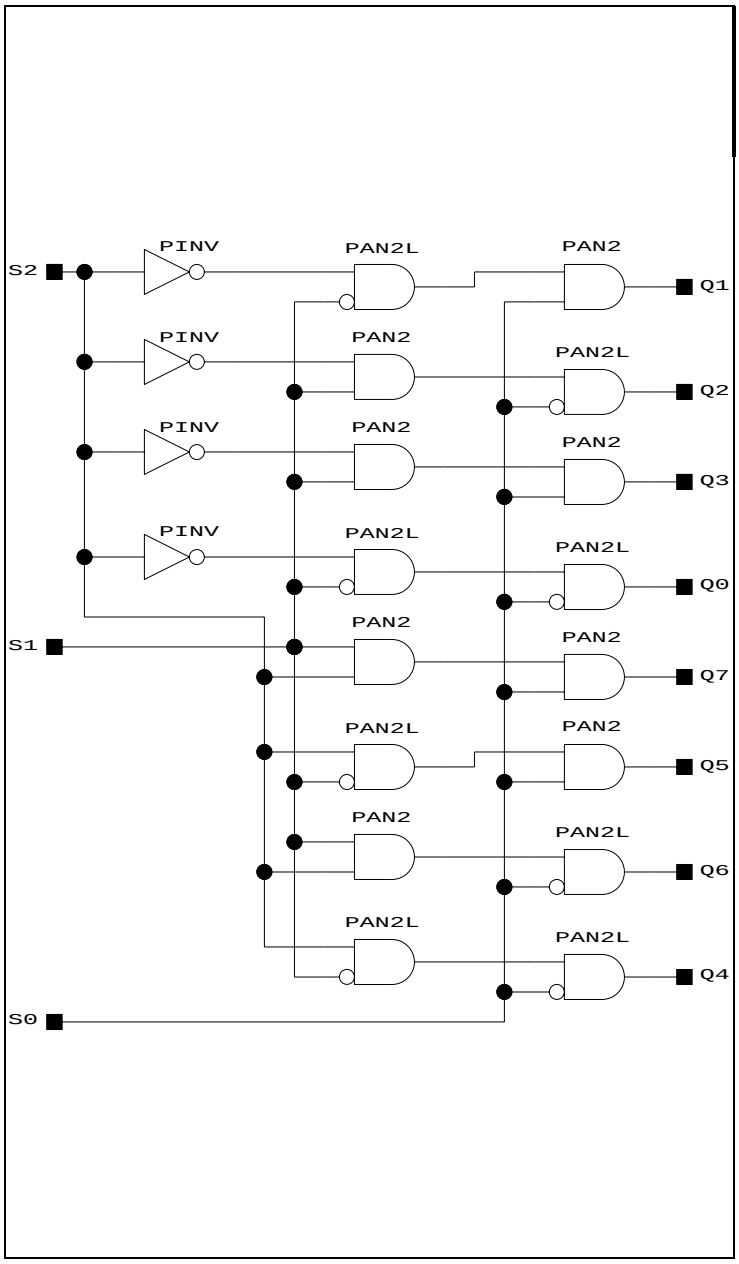
Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S2 → Q0	1.66	2.67	3.88	1.84	2.86	4.08
S1 → Q0	1.28	1.88	2.69	1.37	2.08	2.99
S0 → Q0	0.80	1.10	1.50	0.90	1.30	1.80
S2 → Q1	1.96	3.17	4.68	2.24	3.56	5.08
S1 → Q1	1.58	2.39	3.49	1.77	2.78	3.99
S0 → Q1	0.70	1.20	1.90	0.90	1.50	2.20
S2 → Q2	1.96	3.18	4.69	2.26	3.59	5.11
S1 → Q2	1.18	1.99	3.10	1.39	2.31	3.42
S0 → Q2	0.80	1.10	1.50	0.90	1.30	1.80
S2 → Q3	2.26	3.68	5.49	2.66	4.28	6.11
S1 → Q3	1.48	2.49	3.90	1.79	3.01	4.42
S0 → Q3	0.70	1.20	1.90	0.90	1.50	2.20
S2 → Q4	0.88	1.48	2.29	0.87	1.48	2.29
S1 → Q4	1.28	1.88	2.69	1.37	2.08	2.99
S0 → Q4	0.80	1.10	1.50	0.90	1.30	1.80
S2 → Q5	1.18	1.99	3.09	1.27	2.18	3.29
S1 → Q5	1.58	2.39	3.49	1.77	2.78	3.99
S0 → Q5	0.70	1.20	1.90	0.90	1.50	2.20
S2 → Q6	1.18	1.99	3.10	1.29	2.20	3.32
S1 → Q6	1.18	1.99	3.10	1.39	2.31	3.42
S0 → Q6	0.80	1.10	1.50	0.90	1.30	1.80
S2 → Q7	1.48	2.49	3.90	1.69	2.90	4.32
S1 → Q7	1.48	2.49	3.90	1.79	3.01	4.42
S0 → Q7	0.70	1.20	1.90	0.90	1.50	2.20

Switching Speeds for -4ns Parts

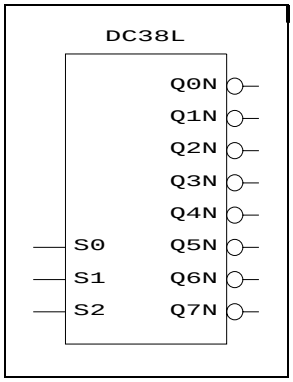
Pin	Rise			Fall		
	Min	Typ	Max	Min	Typ	Max
S2 → Q0	3.64	4.48	5.94	3.74	4.58	5.86
S1 → Q0	2.57	3.19	4.22	2.67	3.29	4.23
S0 → Q0	1.50	1.90	2.40	1.70	2.00	2.50
S2 → Q1	4.34	5.28	7.04	4.44	5.58	7.16
S1 → Q1	3.27	3.99	5.32	3.37	4.29	5.53
S0 → Q1	1.70	2.10	2.80	2.10	2.60	3.30
S2 → Q2	4.34	5.38	7.04	4.55	5.60	7.19
S1 → Q2	2.77	3.49	4.62	3.18	3.91	5.05
S0 → Q2	1.50	1.90	2.40	1.70	2.00	2.50
S2 → Q3	5.04	6.18	8.14	5.25	6.60	8.49
S1 → Q3	3.47	4.29	5.72	3.88	4.91	6.35
S0 → Q3	1.70	2.10	2.80	2.10	2.60	3.30
S2 → Q4	2.07	2.59	3.52	1.97	2.49	3.33
S1 → Q4	2.57	3.19	4.22	2.67	3.29	4.23
S0 → Q4	1.50	1.90	2.40	1.70	2.00	2.50
S2 → Q5	2.77	3.39	4.62	2.67	3.49	4.63
S1 → Q5	3.27	3.99	5.32	3.37	4.29	5.53
S0 → Q5	1.70	2.10	2.80	2.10	2.60	3.30
S2 → Q6	2.77	3.49	4.62	2.78	3.51	4.65
S1 → Q6	2.77	3.49	4.62	3.18	3.91	5.05
S0 → Q6	1.50	1.90	2.40	1.70	2.00	2.50
S2 → Q7	3.47	4.29	5.72	3.48	4.51	5.95
S1 → Q7	3.47	4.29	5.72	3.88	4.91	6.35
S0 → Q7	1.70	2.10	2.80	2.10	2.60	3.30

Schematic



DC38L - 3-8 Decoder Active Low

Symbol



Rectangular Area: 4x8cells

Number of Cells: 24

Truth Table

Input			Output							
S2	S1	S0	Q7N	Q6N	Q5N	Q4N	Q3N	Q2N	Q1N	Q0N
0	0	0	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	1	0	1
0	1	0	1	1	1	1	1	0	1	1
0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	1	1	0	1	1	1	1
1	0	1	1	1	0	1	1	1	1	1
1	1	0	1	0	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
S1 → Q0N.BUS	2.64	4.26	5.98	2.56	3.97	5.58
S2 → Q0N.BUS	3.11	5.04	7.07	2.94	4.76	6.77
S0 → Q0N.BUS	2.17	3.48	4.79	2.08	3.18	4.39
S1 → Q0N	2.24	3.76	5.38	2.06	3.37	4.88
S2 → Q0N	2.71	4.54	6.47	2.44	4.16	6.07
S0 → Q0N	1.77	2.98	4.19	1.58	2.59	3.69
S1 → Q2N.BUS	2.66	4.48	6.41	2.46	4.07	5.99
S2 → Q2N.BUS	3.53	5.76	8.10	3.24	5.26	7.58
S0 → Q2N.BUS	2.17	3.48	4.79	2.08	3.18	4.39
S1 → Q2N	2.26	3.99	5.81	1.96	3.47	5.29
S2 → Q2N	3.13	5.26	7.50	2.74	4.66	6.88
S0 → Q2N	1.77	2.98	4.19	1.58	2.59	3.69
S1 → Q4N.BUS	2.64	4.26	5.98	2.56	3.97	5.58
S2 → Q4N.BUS	2.14	3.66	5.28	2.16	3.57	5.18
S0 → Q4N.BUS	2.17	3.48	4.79	2.08	3.18	4.39
S1 → Q4N	2.24	3.76	5.38	2.06	3.37	4.88
S2 → Q4N	1.74	3.16	4.68	1.66	2.97	4.48
S0 → Q4N	1.77	2.98	4.19	1.58	2.59	3.69
S1 → Q6N.BUS	2.66	4.48	6.41	2.46	4.07	5.99
S2 → Q6N.BUS	2.56	4.38	6.31	2.46	4.07	5.99
S0 → Q6N.BUS	2.17	3.48	4.79	2.08	3.18	4.39
S1 → Q6N	2.26	3.99	5.81	1.96	3.47	5.29
S2 → Q6N	2.16	3.88	5.71	1.96	3.47	5.29
S0 → Q6N	1.77	2.98	4.19	1.58	2.59	3.69
S1 → Q1N	1.77	2.78	3.99	1.68	2.59	3.69
S2 → Q1N	2.24	3.56	5.08	2.06	3.37	4.88
S0 → Q1N	0.80	1.40	2.10	0.90	1.50	2.20
S1 → Q3N	1.79	3.01	4.42	1.58	2.69	4.10

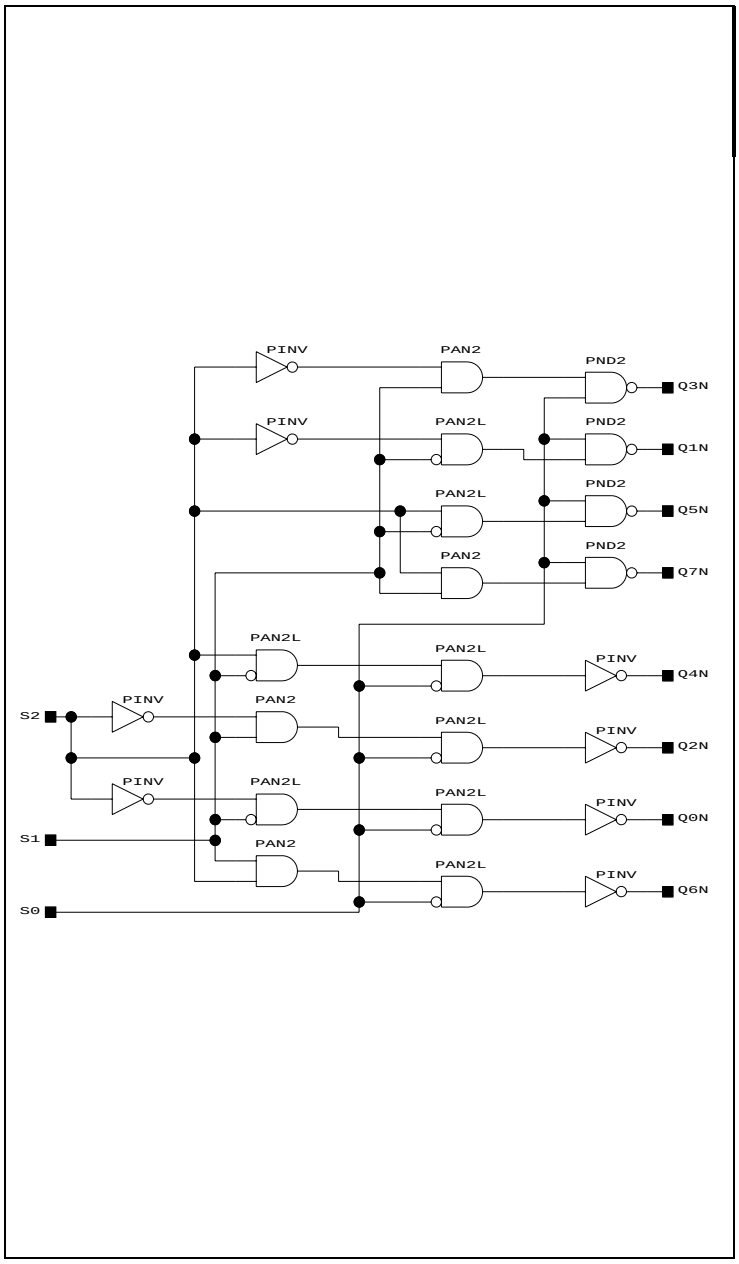
S2 → Q3N	2.66	4.28	6.11	2.36	3.88	5.69
S0 → Q3N	0.80	1.40	2.10	0.90	1.50	2.20
S1 → Q5N	1.77	2.78	3.99	1.68	2.59	3.69
S2 → Q5N	1.27	2.18	3.29	1.28	2.18	3.29
S0 → Q5N	0.80	1.40	2.10	0.90	1.50	2.20
S1 → Q7N	1.79	3.01	4.42	1.58	2.69	4.10
S2 → Q7N	1.69	2.90	4.32	1.58	2.69	4.10
S0 → Q7N	0.80	1.40	2.10	0.90	1.50	2.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
S1 → Q0N.BUS	5.24	6.58	8.86	5.64	6.88	9.44
S2 → Q0N.BUS	6.32	7.87	10.50	6.72	8.17	11.16
S0 → Q0N.BUS	4.27	5.29	7.13	4.57	5.59	7.62
S1 → Q0N	4.54	5.68	7.46	4.64	5.68	7.64
S2 → Q0N	5.62	6.97	9.10	5.72	6.97	9.36
S0 → Q0N	3.57	4.39	5.73	3.57	4.39	5.82
S1 → Q2N.BUS	5.75	7.20	9.69	5.84	7.18	9.84
S2 → Q2N.BUS	7.12	8.89	11.82	7.42	9.07	12.26
S0 → Q2N.BUS	4.27	5.29	7.13	4.57	5.59	7.62
S1 → Q2N	5.05	6.30	8.29	4.84	5.98	8.04
S2 → Q2N	6.42	7.99	10.42	6.42	7.87	10.46
S0 → Q2N	3.57	4.39	5.73	3.57	4.39	5.82
S1 → Q4N.BUS	5.24	6.58	8.86	5.64	6.88	9.44
S2 → Q4N.BUS	4.54	5.78	7.96	5.14	6.28	8.74
S0 → Q4N.BUS	4.27	5.29	7.13	4.57	5.59	7.62
S1 → Q4N	4.54	5.68	7.46	4.64	5.68	7.64
S2 → Q4N	3.84	4.88	6.56	4.14	5.08	6.94
S0 → Q4N	3.57	4.39	5.73	3.57	4.39	5.82
S1 → Q6N.BUS	5.75	7.20	9.69	5.84	7.18	9.84
S2 → Q6N.BUS	5.35	6.80	9.29	5.84	7.18	9.84
S0 → Q6N.BUS	4.27	5.29	7.13	4.57	5.59	7.62
S1 → Q6N	5.05	6.30	8.29	4.84	5.98	8.04
S2 → Q6N	4.65	5.90	7.89	4.84	5.98	8.04
S0 → Q6N	3.57	4.39	5.73	3.57	4.39	5.82
S1 → Q1N	3.47	4.29	5.63	3.37	4.09	5.52
S2 → Q1N	4.54	5.58	7.26	4.44	5.38	7.24
S0 → Q1N	2.20	2.60	3.40	1.80	2.20	3.00
S1 → Q3N	3.98	4.91	6.45	3.57	4.39	5.92

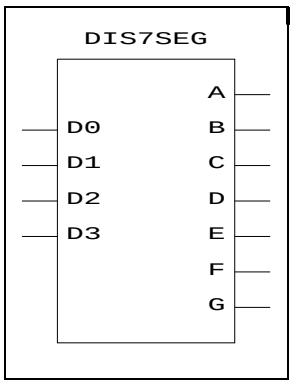
S2 → Q3N	5.35	6.60	8.59	5.14	6.28	8.34
S0 → Q3N	2.20	2.60	3.40	1.80	2.20	3.00
S1 → Q5N	3.47	4.29	5.63	3.37	4.09	5.52
S2 → Q5N	2.77	3.49	4.73	2.87	3.49	4.82
S0 → Q5N	2.20	2.60	3.40	1.80	2.20	3.00
S1 → Q7N	3.98	4.91	6.45	3.57	4.39	5.92
S2 → Q7N	3.58	4.51	6.05	3.57	4.39	5.92
S0 → Q7N	2.20	2.60	3.40	1.80	2.20	3.00

Schematic


PINV
PAN2
PND2
Q3N
PINV
PAN2L
PND2
Q1N
PAN2L
PND2
Q5N
PAN2
PND2
Q7N
PAN2L
PAN2L
PINV
Q4N
S2
PINV
PAN2
PAN2L
PINV
Q2N
PINV
PAN2L
PAN2L
PINV
Q0N
S1
PAN2
PAN2L
PINV
Q6N
S0

DIS7SEG - 7 Segment BCD Display (0 to F)

Symbol



Rectangular Area: 5x26cells

Number of Cells: 84

Truth Table

Input				Output						
D3	D2	D1	D0	A	B	C	D	E	F	G
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	0	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	0	0	1	1
1	0	1	0	0	0	0	1	1	0	1
1	0	1	1	0	0	1	1	0	0	1
1	1	0	0	0	1	0	0	0	1	1
1	1	0	1	1	0	0	1	0	1	1
1	1	1	0	0	0	0	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0

Switching Speeds for -2ns Parts

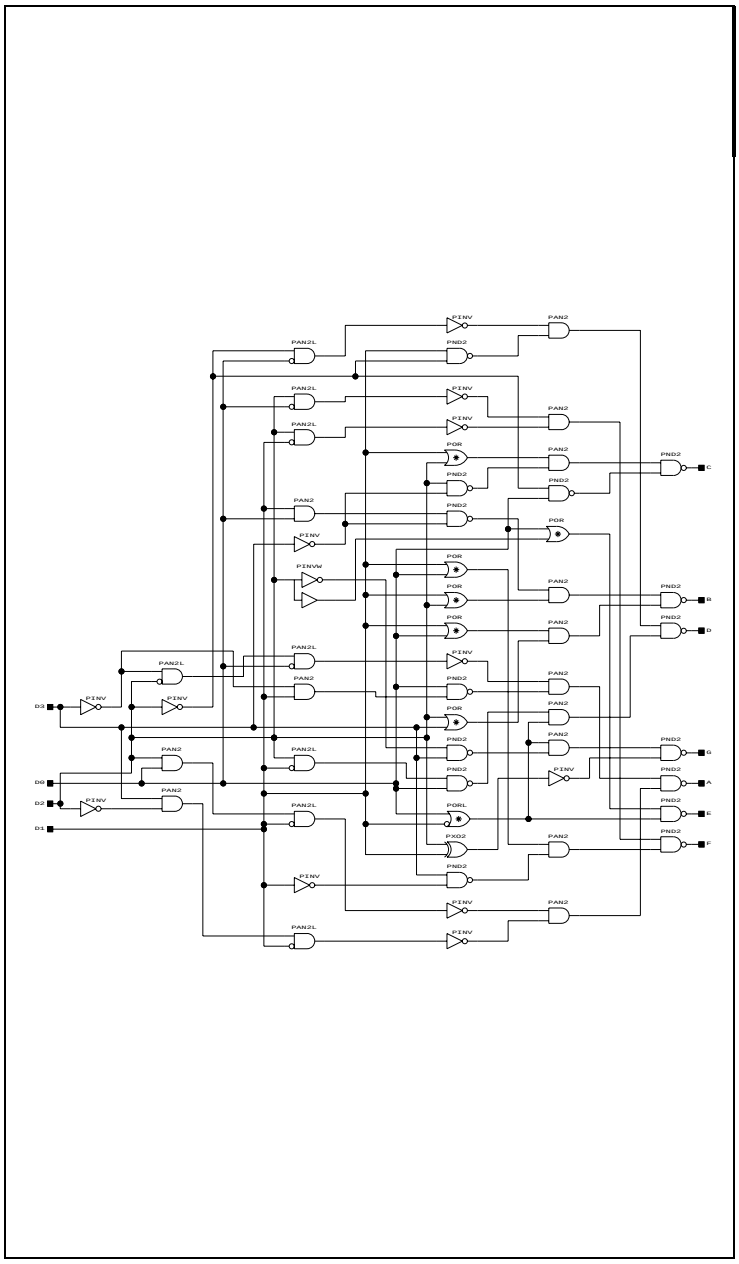
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D1 → G	2.91	5.88	9.47	2.92	5.68	8.85
D0 → G	3.64	6.30	9.37	3.37	5.91	8.85
D3 → G	3.03	5.37	8.00	2.83	5.06	7.59
D2 → G	2.91	5.95	9.59	2.82	5.85	9.28
D1 → F	3.03	6.06	10.20	2.73	5.70	9.68
D0 → F	3.13	5.57	8.30	2.73	5.35	8.38
D3 → F	3.13	5.37	8.01	2.74	4.96	7.48
D2 → F	2.94	5.66	9.10	2.72	5.44	8.67
D1 → E	2.38	4.02	5.96	2.21	3.84	5.66
D0 → E	2.28	4.28	6.97	2.21	4.15	6.69
D2 → E	3.18	5.42	8.16	3.01	5.24	7.88
D1 → D	3.03	6.66	11.85	2.83	6.27	11.23
D0 → D	3.60	7.01	11.75	3.22	6.61	11.23
D2 → D	3.98	7.93	13.31	3.69	7.70	13.07
D1 → C	3.13	5.47	8.10	2.73	4.95	7.48
D0 → C	2.04	3.66	5.59	2.06	3.67	5.58
D3 → C	4.83	8.19	12.06	4.73	7.99	11.75
D2 → C	3.03	6.00	10.38	2.73	5.79	9.97
D1 → B	2.66	5.86	10.48	2.25	5.39	10.06
D0 → B	3.60	6.55	10.29	3.21	6.13	9.96
D3 → B	3.60	6.79	10.78	3.21	6.47	10.65
D2 → B	2.56	5.37	9.19	2.25	4.95	8.68
D1 → A	3.24	6.90	11.87	3.25	6.94	11.96
D0 → A	2.46	6.05	11.47	2.26	5.88	11.35
D3 → A	4.10	7.72	12.66	4.19	7.77	12.55
D2 → A	4.37	8.41	14.25	4.14	8.39	14.24

Switching Speeds for -4ns Parts

	Rise			Fall		

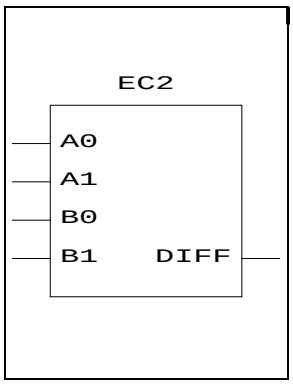
Pin	Min	Typ	Max	Min	Typ	Max
D1 → G	6.81	9.61	14.50	7.31	9.40	13.15
D0 → G	8.33	10.45	14.10	7.73	9.74	13.15
D3 → G	7.22	8.98	12.21	6.92	8.67	11.45
D2 → G	6.81	9.66	14.74	6.91	9.51	13.68
D1 → F	7.22	9.62	13.93	6.52	9.41	14.09
D0 → F	7.22	9.23	12.51	6.52	8.62	11.86
D3 → F	6.52	8.08	10.91	6.91	8.57	11.37
D2 → F	6.72	8.92	12.73	6.62	8.76	12.69
D1 → E	5.88	7.15	9.62	4.89	6.26	8.31
D0 → E	5.48	7.51	11.28	4.89	6.87	9.85
D2 → E	7.78	9.55	13.12	6.89	8.86	11.68
D1 → D	7.12	11.20	17.97	6.92	10.55	16.81
D0 → D	7.49	11.20	17.57	7.98	11.19	16.81
D2 → D	8.56	12.51	19.23	8.55	12.51	19.22
D1 → C	7.62	9.38	12.51	6.52	8.27	11.06
D0 → C	4.54	5.77	7.75	4.64	5.78	7.84
D3 → C	11.10	13.64	18.34	10.50	13.23	17.48
D2 → C	6.32	9.73	15.67	6.52	9.86	15.12
D1 → B	6.54	10.03	16.07	5.44	8.97	14.82
D0 → B	8.46	10.76	14.47	7.59	10.11	14.42
D3 → B	8.69	11.11	15.30	7.59	10.55	15.45
D2 → B	6.14	8.98	13.94	5.44	8.27	12.88
D1 → A	7.22	11.01	17.30	7.52	11.27	17.35
D0 → A	5.44	9.62	16.68	5.34	9.61	16.66
D3 → A	8.86	12.40	18.44	8.96	12.60	18.58
D2 → A	9.16	13.49	20.97	9.15	13.64	20.81

Schematic



EC2 - 2-Bit Equality Comparator

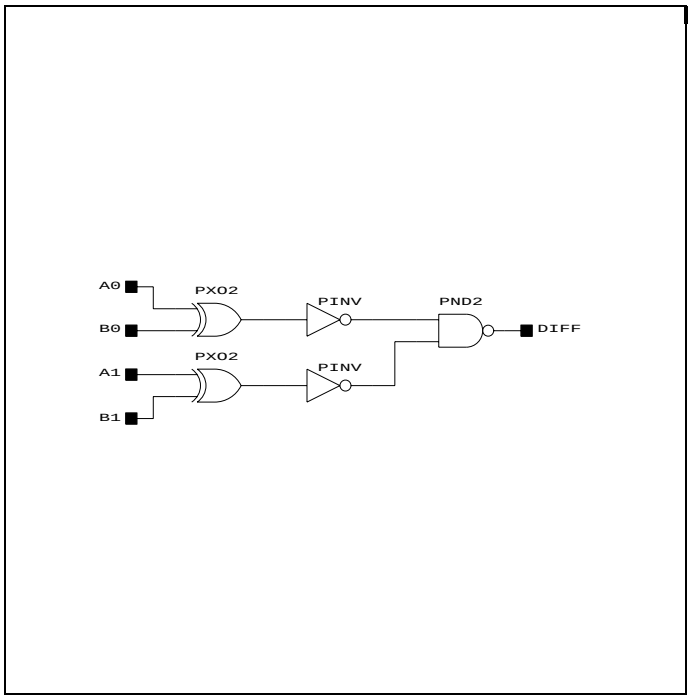
Symbol



Rectangular Area: 3x2cells

Number of Cells: 6

Schematic



Truth Table

Input				Output
A1	A0	B1	B0	DIFF
	a < b, a > b			1
	a = b			0

Switching Speeds for -2ns Parts

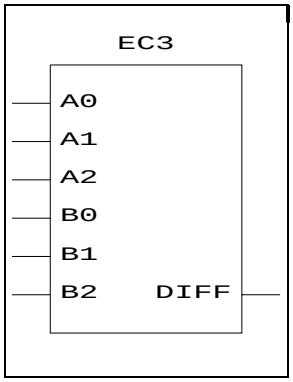
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
B1 → DIFF	2.91	5.14	7.77	2.92	5.45	7.97
A1 → DIFF	2.91	5.14	7.77	2.92	5.45	7.97
B0 → DIFF	2.44	4.36	6.58	2.44	4.66	6.78
A0 → DIFF	2.44	4.36	6.58	2.44	4.66	6.78

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
B1 → DIFF	6.71	8.36	11.26	7.41	9.26	12.36
A1 → DIFF	6.71	8.36	11.26	7.41	9.26	12.36
B0 → DIFF	5.64	7.07	9.53	6.34	7.87	10.53
A0 → DIFF	5.64	7.07	9.53	6.34	7.87	10.53

EC3 - 3-Bit Equality Comparator

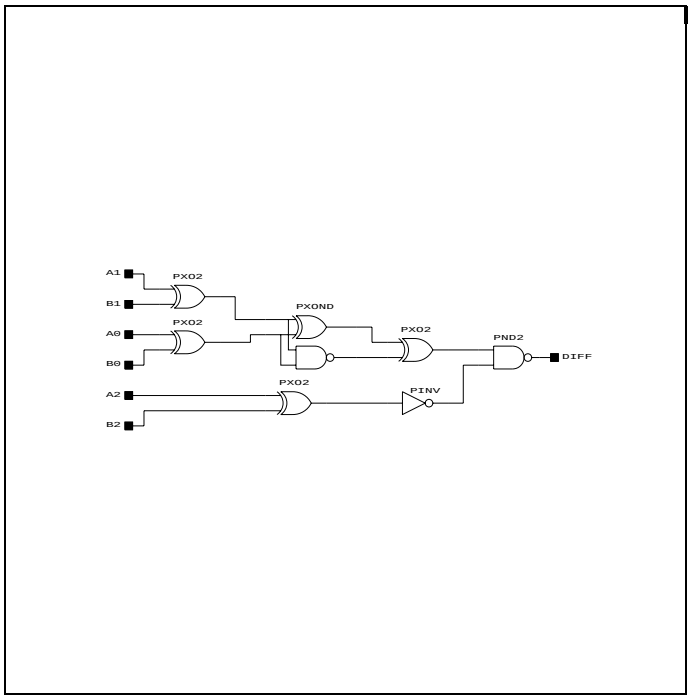
Symbol



Rectangular Area: 3x3cells

Number of Cells: 9

Schematic



Truth Table

Input						Output
A2	A1	A0	B2	B1	B0	DIFF
			a < b, a > b			1
			a = b			0

Switching Speeds for -2ns Parts

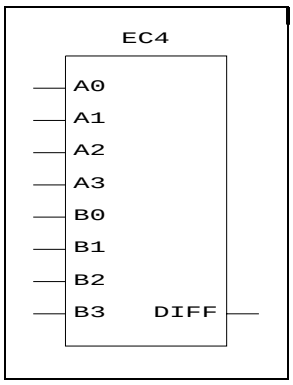
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
B2 → DIFF	2.91	5.14	7.77	2.92	5.45	7.97
A2 → DIFF	2.91	5.14	7.77	2.92	5.45	7.97
B1 → DIFF	3.78	6.82	10.26	3.68	6.72	10.06
A1 → DIFF	3.78	6.82	10.26	3.68	6.72	10.06
B0 → DIFF	3.31	6.04	9.07	3.21	5.94	8.87
A0 → DIFF	3.31	6.04	9.07	3.21	5.94	8.87

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
B2 → DIFF	6.71	8.36	11.26	7.41	9.26	12.36
A2 → DIFF	6.71	8.36	11.26	7.41	9.26	12.36
B1 → DIFF	8.97	12.09	17.59	8.38	11.50	16.58
A1 → DIFF	8.97	12.09	17.59	8.38	11.50	16.58
B0 → DIFF	7.90	10.75	15.86	7.31	10.16	14.85
A0 → DIFF	7.90	10.75	15.86	7.31	10.16	14.85

EC4 - 4-Bit Equality Comparator

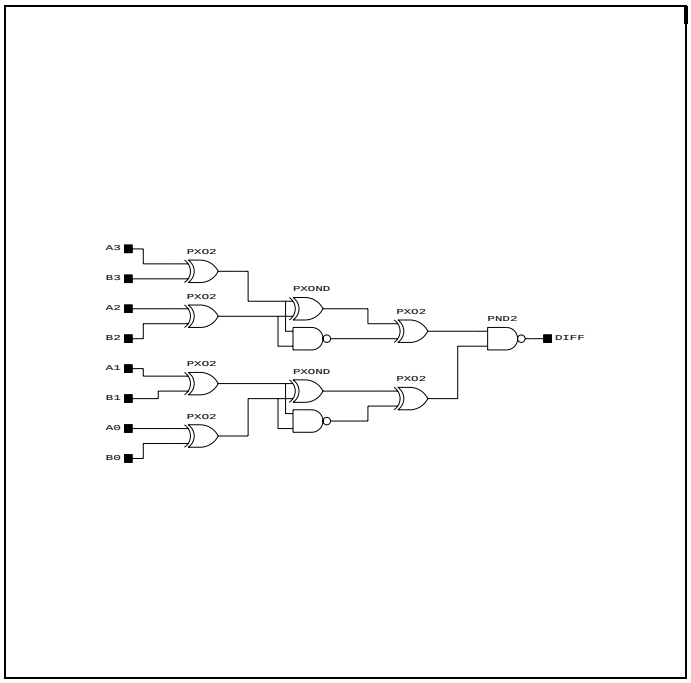
Symbol



Rectangular Area: 3x4cells

Number of Cells: 12

Schematic



Truth Table

Input								Output
A3	A2	A1	A0	B3	B2	B1	B0	DIFF
				a < b, a > b				1
				a = b				0

Switching Speeds for -2ns Parts

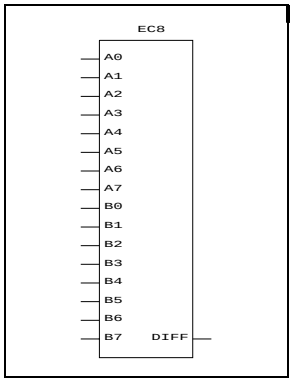
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
B3 → DIFF	3.78	6.82	10.26	3.69	6.72	10.06
A3 → DIFF	3.78	6.82	10.26	3.69	6.72	10.06
B2 → DIFF	4.25	7.60	11.45	4.16	7.51	11.25
A2 → DIFF	4.25	7.60	11.45	4.16	7.51	11.25
B1 → DIFF	3.78	6.82	10.26	3.68	6.72	10.06
A1 → DIFF	3.78	6.82	10.26	3.68	6.72	10.06
B0 → DIFF	3.31	6.04	9.07	3.21	5.94	8.87
A0 → DIFF	3.31	6.04	9.07	3.21	5.94	8.87

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
B3 → DIFF	8.97	12.04	17.59	8.38	11.55	16.68
A3 → DIFF	8.97	12.04	17.59	8.38	11.55	16.68
B2 → DIFF	10.04	13.38	19.33	9.45	12.89	18.42
A2 → DIFF	10.04	13.38	19.33	9.45	12.89	18.42
B1 → DIFF	8.97	12.09	17.59	8.38	11.50	16.58
A1 → DIFF	8.97	12.09	17.59	8.38	11.50	16.58
B0 → DIFF	7.90	10.75	15.86	7.31	10.16	14.85
A0 → DIFF	7.90	10.75	15.86	7.31	10.16	14.85

EC8 - 8-Bit Equality Comparator

Symbol



Rectangular Area: 7x4cells

Number of Cells: 27

Truth Table

Input A7...A0	Input B7...B0	Output DIFF
a < b, a > b		1
a = b		0

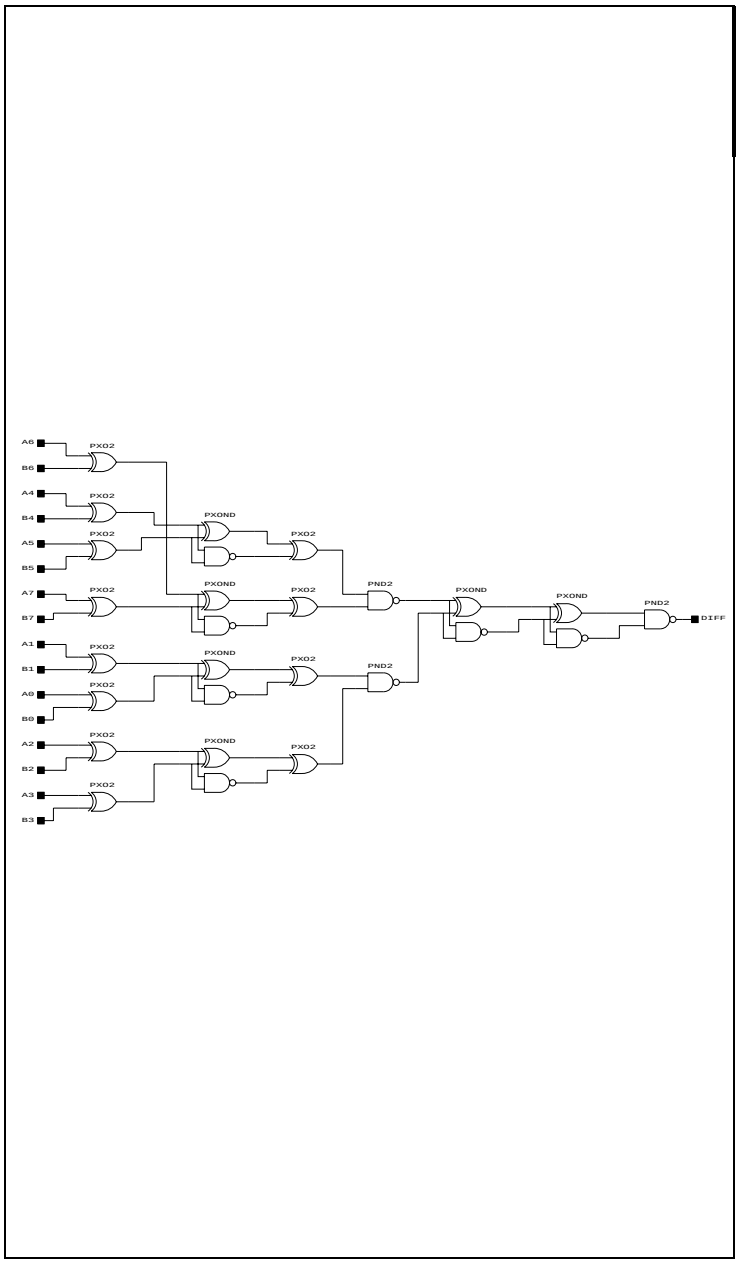
Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A0 → DIFF	6.57	12.10	18.32	6.57	12.06	18.22
B0 → DIFF	6.57	12.10	18.32	6.57	12.06	18.22
A4 → DIFF	5.62	10.53	15.94	5.62	10.48	15.84
B4 → DIFF	5.62	10.53	15.94	5.62	10.48	15.84
A1 → DIFF	7.04	12.89	19.51	7.04	12.83	19.41
B1 → DIFF	7.04	12.89	19.51	7.04	12.83	19.41
A2 → DIFF	6.56	12.10	18.32	6.56	12.05	18.22
B2 → DIFF	6.56	12.10	18.32	6.56	12.05	18.22
A3 → DIFF	6.09	11.32	17.13	6.09	11.27	17.03
B3 → DIFF	6.09	11.32	17.13	6.09	11.27	17.03
A5 → DIFF	6.09	11.32	17.13	6.09	11.27	17.03
B5 → DIFF	6.09	11.32	17.13	6.09	11.27	17.03
A6 → DIFF	6.57	12.11	18.32	6.57	12.05	18.22
B6 → DIFF	6.57	12.11	18.32	6.57	12.05	18.22
A7 → DIFF	6.10	11.32	17.13	6.10	11.27	17.03
B7 → DIFF	6.10	11.32	17.13	6.10	11.27	17.03

Switching Speeds for -4ns Parts

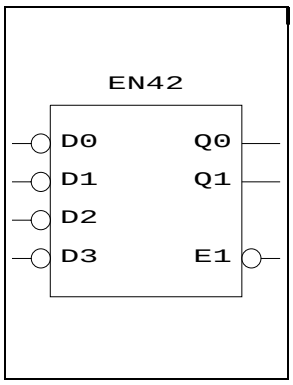
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A0 → DIFF	14.84	20.79	31.09	14.84	20.49	30.08
B0 → DIFF	14.84	20.79	31.09	14.84	20.49	30.08
A4 → DIFF	12.70	18.11	27.52	12.70	17.82	26.51
B4 → DIFF	12.70	18.11	27.52	12.70	17.82	26.51
A1 → DIFF	15.91	22.12	32.82	15.91	21.84	31.81
B1 → DIFF	15.91	22.12	32.82	15.91	21.84	31.81
A2 → DIFF	14.84	20.79	31.09	14.84	20.49	30.08
B2 → DIFF	14.84	20.79	31.09	14.84	20.49	30.08
A3 → DIFF	13.77	19.44	29.36	13.77	19.15	28.35
B3 → DIFF	13.77	19.44	29.36	13.77	19.15	28.35
A5 → DIFF	13.77	19.44	29.26	13.77	19.15	28.25
B5 → DIFF	13.77	19.44	29.26	13.77	19.15	28.25
A6 → DIFF	14.84	20.78	30.99	14.84	20.49	29.98
B6 → DIFF	14.84	20.78	30.99	14.84	20.49	29.98
A7 → DIFF	13.77	19.44	29.26	13.77	19.15	28.25
B7 → DIFF	13.77	19.44	29.26	13.77	19.15	28.25

Schematic



EN42 - 4-to-2 Encoder

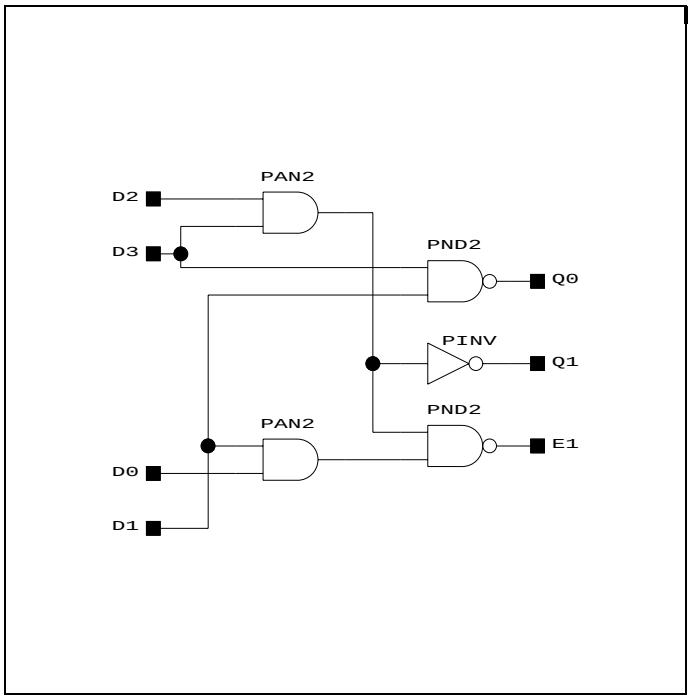
Symbol



Rectangular Area: 2x3cells

Number of Cells: 6

Schematic



Truth Table

Input				Output		
D3	D2	D1	D0	Q1	Q0	E1
1	1	1	1	0	0	0
1	1	1	0	0	0	1
1	1	0	x	0	1	1
1	0	1	x	1	0	1
1	0	0	x	1	1	1
0	x	x	x	1	1	1

Switching Speeds for -2ns Parts

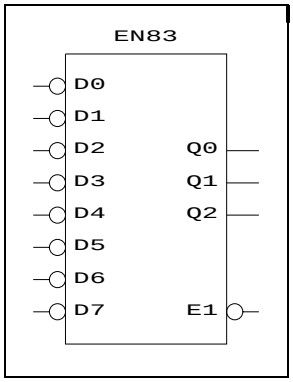
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
D0 → E1	1.69	3.01	4.52	1.38	2.69	4.10
D2 → E1	2.23	3.86	5.80	1.94	3.56	5.38
D3 → E1	2.23	3.86	5.80	1.94	3.56	5.38
D1 → E1	1.69	3.01	4.52	1.38	2.69	4.10
D2 → Q1.BUS	2.63	4.56	6.50	2.44	4.16	6.08
D3 → Q1.BUS	2.63	4.56	6.50	2.44	4.16	6.08
D2 → Q1	2.23	4.07	5.90	1.94	3.56	5.38
D3 → Q1	2.23	4.07	5.90	1.94	3.56	5.38
D3 → Q0	0.80	1.40	2.20	0.70	1.40	2.10
D1 → Q0	0.80	1.40	2.20	0.70	1.40	2.10

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D0 → E1	3.58	4.51	6.05	3.57	4.49	6.02
D2 → E1	4.72	5.89	7.92	4.72	5.97	7.98
D3 → E1	4.72	5.89	7.92	4.72	5.97	7.98
D1 → E1	3.58	4.51	6.05	3.57	4.49	6.02
D2 → Q1.BUS	5.62	6.99	9.52	5.92	7.37	10.08
D3 → Q1.BUS	5.62	6.99	9.52	5.92	7.37	10.08
D2 → Q1	4.92	6.09	8.12	4.92	6.17	8.28
D3 → Q1	4.92	6.09	8.12	4.92	6.17	8.28
D3 → Q0	1.70	2.10	2.90	1.80	2.30	3.00
D1 → Q0	1.70	2.10	2.90	1.80	2.30	3.00

EN83 - 8-to-3 Encoder

Symbol



Rectangular Area: 4x4cells

Number of Cells: 11

Truth Table

Input								Output			
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Q2**	**Q1**	**Q0**	**E1**
1	1	1	1	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	0	0	0	0	1
1	1	1	1	1	1	0	x	0	0	1	1
1	1	1	1	1	0	d1	x	0	1(a)	0(a)	1
1	1	1	1	0	d2	d1	x	0	1(a)	1(a)	1
1	1	1	0	d3	d2	d1	x	1	0(a)	0(a)	1
1	1	0	d4	d3	d2	d1	x	1	0(a)	1(a)	1
1	0	d5	d4	d3	d2	d1	x	1	1(a)	0(a)	1
0	d6	d5	d4	d3	d2	d1	x	1	1(a)	1(a)	1
1	1	1	1	d3	d2	d1	-	0(b)	-	-	-

(a) Q0 = (D7*D5*D3*D1)'; Q1 = (D7*D6*D3*D2)'

(b) Q2 = (D7*D6*D5*D4)'

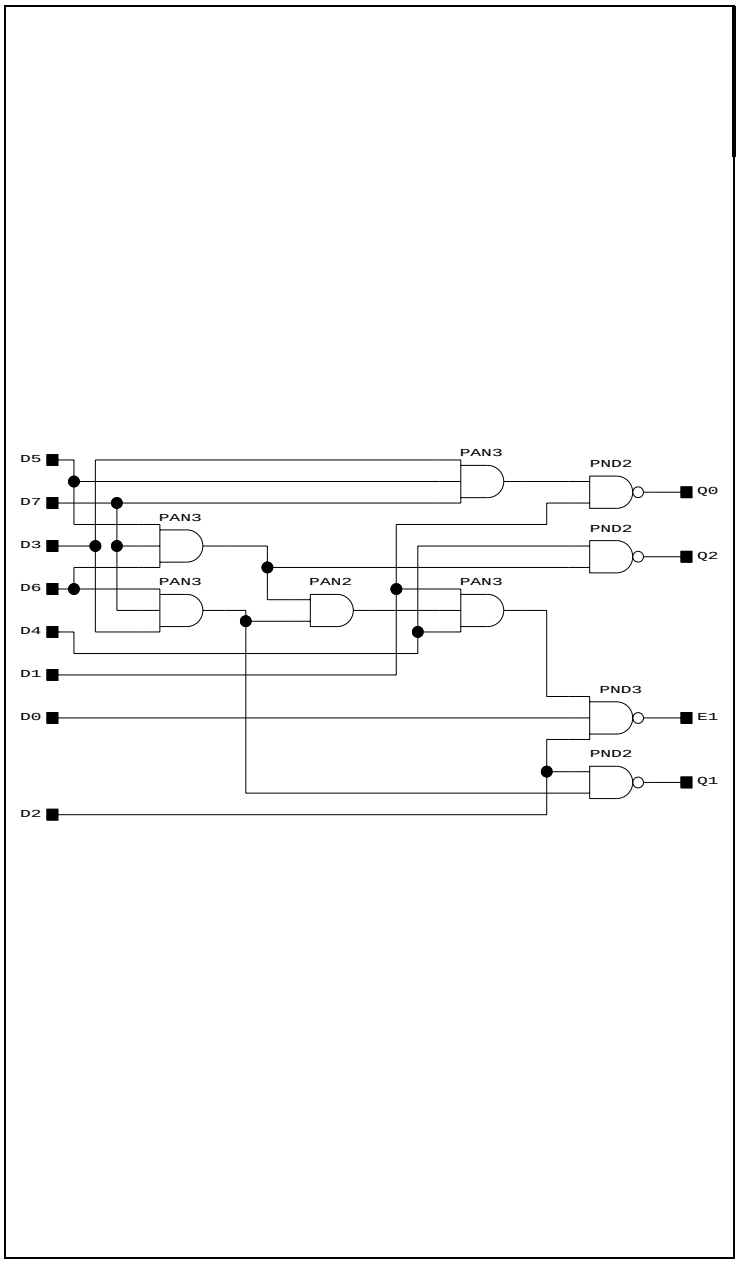
Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D1 → Q0	0.80	1.40	2.20	0.70	1.40	2.10
D7 → Q0	1.79	3.11	4.62	1.38	2.69	4.10
D3 → Q0	1.69	3.01	4.52	1.38	2.69	4.10
D5 → Q0	1.69	3.01	4.52	1.38	2.69	4.10
D2 → Q1	0.80	1.40	2.20	0.70	1.40	2.10
D7 → Q1	2.33	3.97	5.90	1.94	3.56	5.38
D3 → Q1	2.23	3.86	5.80	1.94	3.56	5.38
D6 → Q1	2.23	3.86	5.80	1.94	3.56	5.38
D4 → Q2	0.80	1.40	2.20	0.70	1.40	2.10
D7 → Q2	2.33	3.97	5.90	1.94	3.56	5.38
D6 → Q2	2.23	3.86	5.80	1.94	3.56	5.38
D5 → Q2	2.23	3.86	5.80	1.94	3.56	5.38
D1 → E1	1.79	3.11	4.62	1.38	2.69	4.10
D4 → E1	1.69	3.01	4.52	1.38	2.69	4.10
D2 → E1	0.90	1.50	2.30	0.70	1.40	2.10
D0 → E1	0.80	1.40	2.20	0.70	1.40	2.10
D7 → E1	4.11	7.56	11.73	3.30	6.53	10.58
D3 → E1	4.48	7.86	11.63	3.78	6.93	10.58
D6 → E1	4.01	7.47	11.63	3.30	6.53	10.58
D5 → E1	4.01	7.07	10.44	3.30	6.14	9.38

Switching Speeds for -4ns Parts

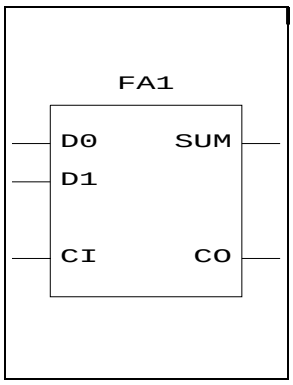
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D1 → Q0	1.70	2.10	2.90	1.80	2.30	3.00
D7 → Q0	3.98	4.91	6.45	3.57	4.49	6.02
D3 → Q0	3.58	4.51	6.05	3.57	4.49	6.02
D5 → Q0	3.58	4.51	6.05	3.57	4.49	6.02
D2 → Q1	1.70	2.10	2.90	1.80	2.30	3.00
D7 → Q1	5.12	6.29	8.32	4.72	5.97	7.98
D3 → Q1	4.72	5.89	7.92	4.72	5.97	7.98
D6 → Q1	4.72	5.89	7.92	4.72	5.97	7.98
D4 → Q2	1.70	2.10	2.90	1.80	2.30	3.00
D7 → Q2	5.02	6.29	8.32	4.72	5.87	7.96
D6 → Q2	4.62	5.89	7.92	4.72	5.87	7.96
D5 → Q2	4.62	5.89	7.92	4.72	5.87	7.96
D1 → E1	3.98	4.91	6.45	3.57	4.49	6.02
D4 → E1	3.58	4.51	6.05	3.57	4.49	6.02
D2 → E1	1.70	2.10	2.90	2.20	2.70	3.40
D0 → E1	1.70	2.10	2.90	1.80	2.30	3.00
D7 → E1	8.79	11.75	16.46	8.26	10.99	15.85
D3 → E1	9.56	12.00	16.06	9.33	11.74	15.85
D6 → E1	8.39	11.36	16.06	8.26	10.99	15.85
D5 → E1	8.39	10.71	14.23	8.26	10.25	14.00

Schematic


D5
D7
D3
D6
D4
D1
D0
D2
PAN3
PAN3
PAN3
PAN2
PAN3
PND2
PND2
PND3
PND2
Q0
Q2
E1
Q1

FA1 - 1-Bit Full Adder

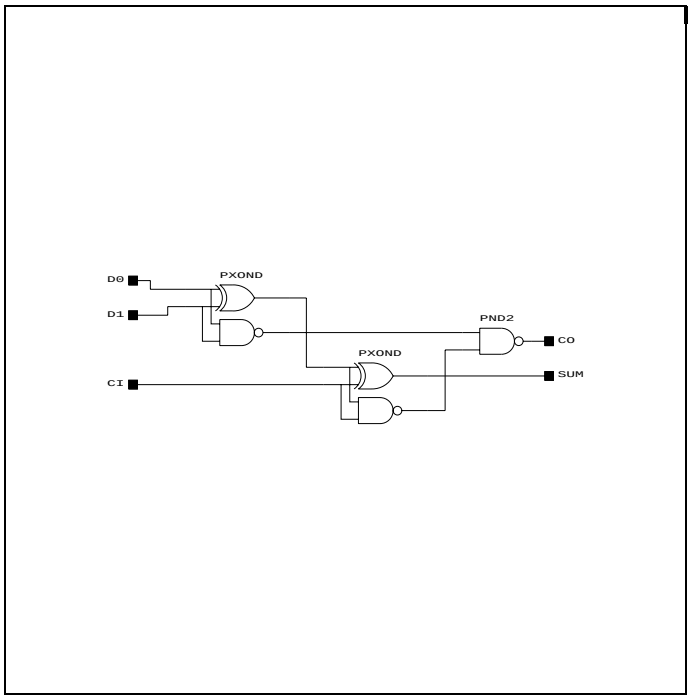
Symbol



Rectangular Area: 2x2cells

Number of Cells: 4

Schematic



Truth Table

Input			Output	
D0	D1	CI	SUM	CO
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Switching Speeds for -2ns Parts

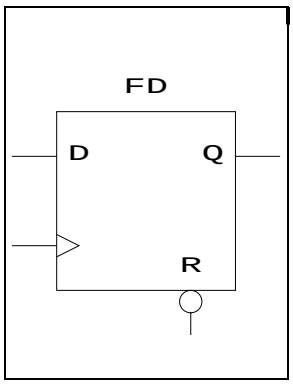
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
D0 → SUM.BUS	2.07	3.48	4.99	2.17	3.68	5.19
D1 → SUM.BUS	2.07	3.48	4.99	2.17	3.68	5.19
CI → SUM.BUS	1.20	1.90	2.70	1.30	2.10	2.90
D0 → SUM	1.67	2.98	4.39	1.67	3.08	4.49
D1 → SUM	1.67	2.98	4.39	1.67	3.08	4.49
CI → SUM	0.80	1.40	2.10	0.80	1.50	2.20
D0 → CO	2.04	4.06	6.69	2.06	4.07	6.68
D1 → CO	2.04	4.06	6.69	2.06	4.07	6.68
CI → CO	1.57	2.88	4.40	1.58	2.88	4.39

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D0 → SUM.BUS	4.37	6.38	8.82	5.37	7.48	10.32
D1 → SUM.BUS	4.37	6.38	8.82	5.37	7.48	10.32
CI → SUM.BUS	2.50	3.20	4.50	3.50	4.30	6.00
D0 → SUM	3.67	5.48	7.42	4.37	6.28	8.52
D1 → SUM	3.67	5.48	7.42	4.37	6.28	8.52
CI → SUM	1.80	2.30	3.10	2.50	3.10	4.20
D0 → CO	4.64	6.71	10.34	4.64	6.78	10.34
D1 → CO	4.64	6.71	10.34	4.64	6.78	10.34
CI → CO	3.56	4.48	6.02	3.56	4.49	6.02

FD - D Flip-Flop Synchronous

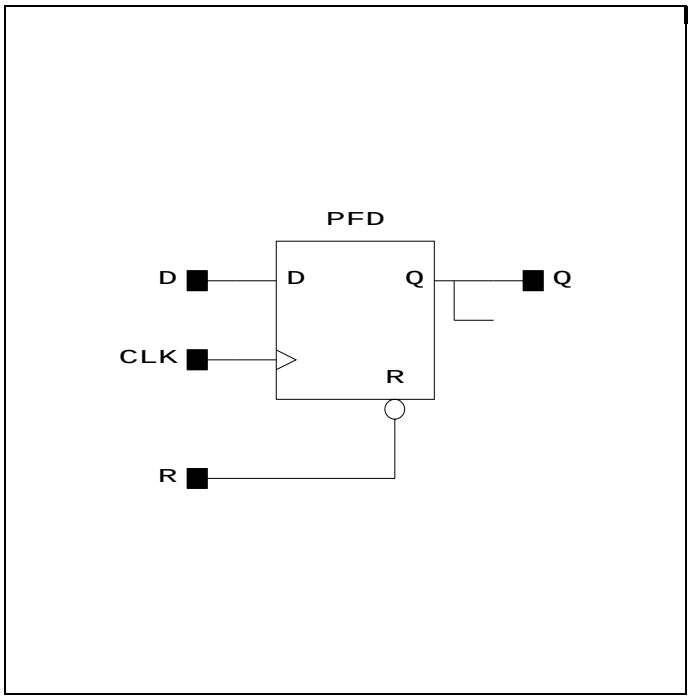
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input			Output
R	CLK	D	Q
0	x	x	0
1	x	x	q
1	r	d	d

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20
R → Q	0.00	0.00	0.00	1.40	1.60	1.80
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q.BUS	0.40	0.50	0.60	1.90	2.20	2.50

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	2.10	2.10	2.10	0.00	0.00	0.00

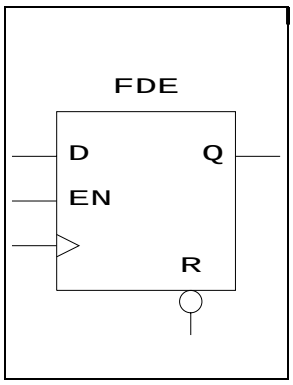
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60
R → Q	0.00	0.00	0.00	2.40	2.70	3.00
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q.BUS	0.70	0.90	1.40	3.40	3.90	4.80

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	3.50	3.50	3.50	0.00	0.00	0.00

FDE - D Flip-Flop Synchronous with Enable

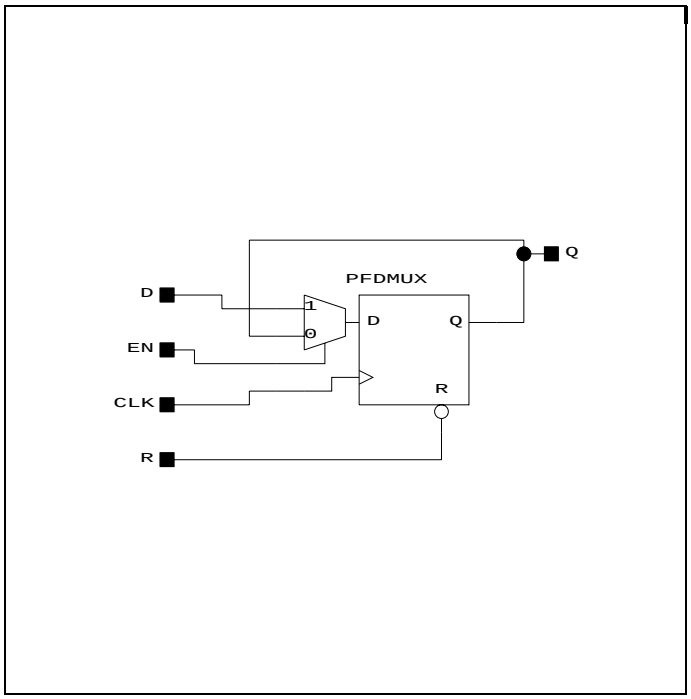
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input				Output
R	EN	CLK	D	Q
0	x	x	x	0
1	0	x	x	q
1	1	r	d	d

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q	-	-	-	1.48	1.71	1.93
CLK → Q	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	3.90	4.10	4.30	0.00	0.00	0.00
EN	3.80	4.00	4.30	0.00	0.00	0.00

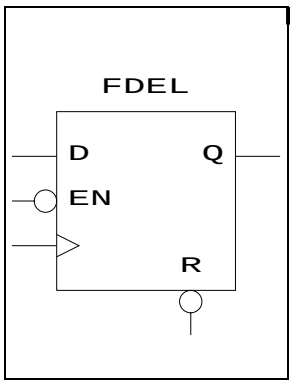
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q	-	-	-	2.48	2.81	3.15
CLK → Q	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	6.30	6.60	6.90	0.00	0.00	0.00
EN	6.10	6.40	6.70	0.00	0.00	0.00

FDEL - D Flip-Flop Synch with Enable Low

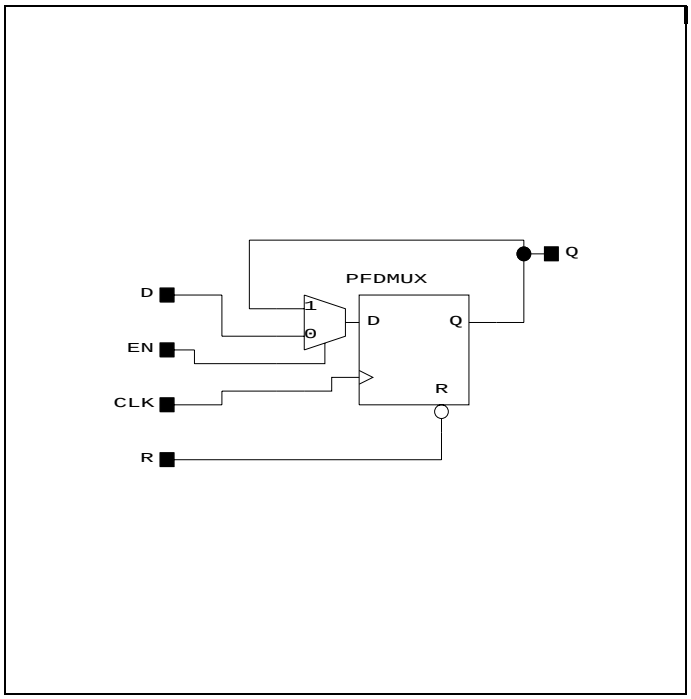
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input R	EN	CLK	D	Output Q
0	x	x	x	0
1	1	x	x	q
1	0	r	d	d

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q	-	-	-	1.48	1.71	1.93
CLK → Q	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	3.90	4.10	4.30	0.00	0.00	0.00
EN	3.80	4.00	4.30	0.00	0.00	0.00

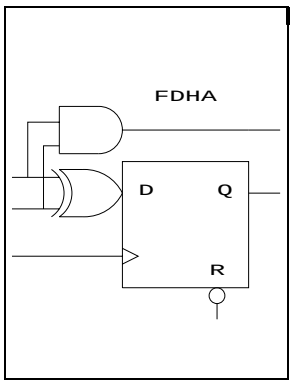
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q	-	-	-	2.48	2.81	3.15
CLK → Q	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	6.30	6.60	6.90	0.00	0.00	0.00
EN	6.10	6.40	6.70	0.00	0.00	0.00

FDHA - D Flip-Flop Half-Adder Sum

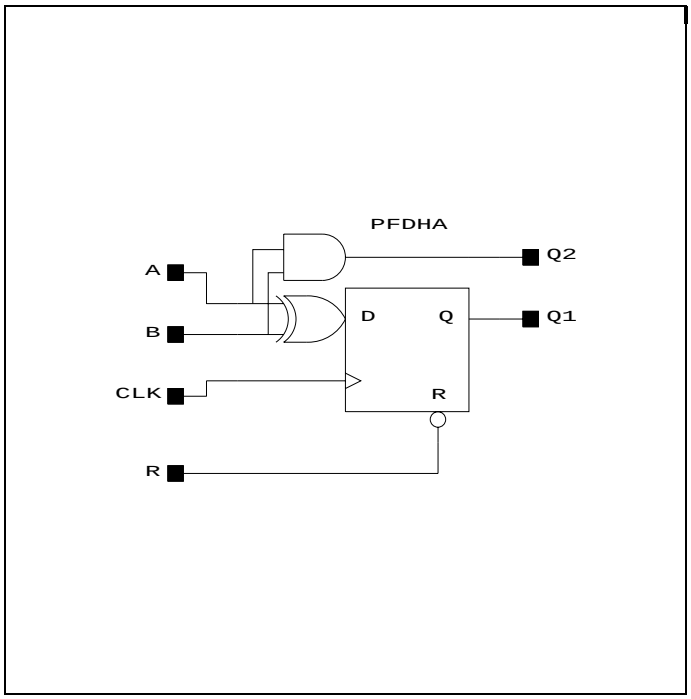
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input				Output	
R	CLK	A	B	Q1	Q2
0	x	x	x	0	x
1	r	0	b	b	0
1	r	1	b	b'	b
1	r	a	0	a	0
1	r	a	1	a'	a

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q1	1.40	1.60	1.80	1.80	2.00	2.20
R → Q1	0.00	0.00	0.00	1.40	1.60	1.80
A → Q2	0.70	1.20	1.90	0.80	1.40	2.10
B → Q2	0.70	1.20	1.90	0.90	1.50	2.20

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
A	2.10	2.10	2.10	0.00	0.00	0.00
B	2.10	2.10	2.10	0.00	0.00	0.00

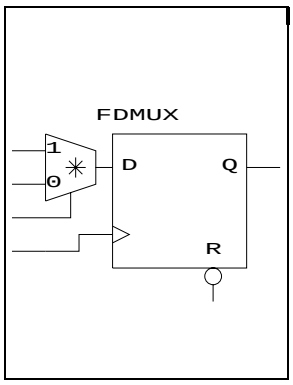
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q1	2.40	2.70	3.00	3.00	3.30	3.60
R → Q1	0.00	0.00	0.00	2.40	2.70	3.00
A → Q2	1.70	2.10	2.80	1.70	2.20	2.90
B → Q2	1.70	2.10	2.80	2.10	2.60	3.30

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
A	3.70	3.70	3.70	0.00	0.00	0.00
B	3.70	3.70	3.70	0.00	0.00	0.00

FDMUX - MUX Feeding D Flip-Flop

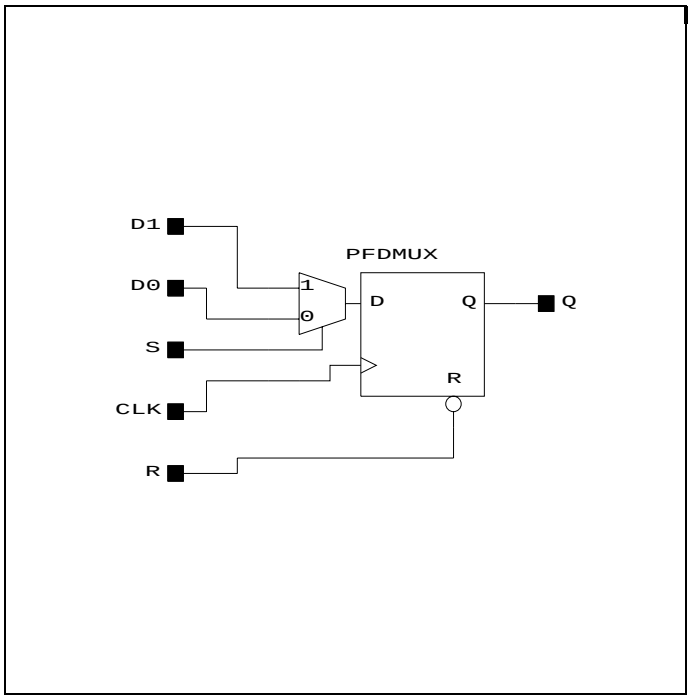
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input					Output
R	CLK	S	D1	D0	Q
0	x	x	x	x	0
1	r	0	x	d0	d0
1	r	1	d1	x	d1

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20
R → Q	0.00	0.00	0.00	1.40	1.60	1.80

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D0	3.90	4.10	4.30	0.00	0.00	0.00
D1	3.90	4.10	4.30	0.00	0.00	0.00
S	3.80	4.00	4.30	0.00	0.00	0.00

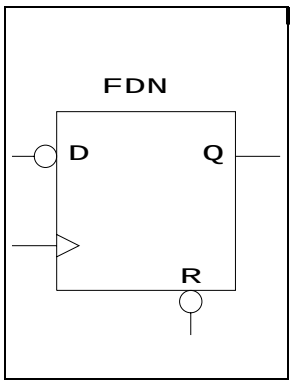
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60
R → Q	0.00	0.00	0.00	2.40	2.70	3.00

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D0	6.30	6.60	6.90	0.00	0.00	0.00
D1	6.30	6.60	6.90	0.00	0.00	0.00
S	6.10	6.40	6.70	0.00	0.00	0.00

FDN - D Flip-Flop Synchronous with QN Out

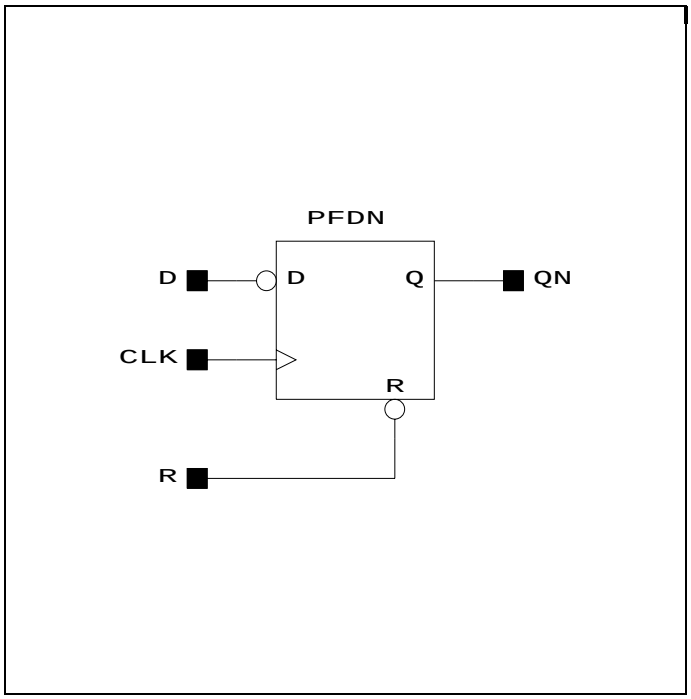
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input R	CLK	D	Output QN
0	x	x	0
1	r	d	d'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → QN	-	-	-	1.40	1.60	1.80
CLK → QN	1.40	1.60	1.80	1.80	2.00	2.20

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	2.10	2.10	2.10	0.00	0.00	0.00

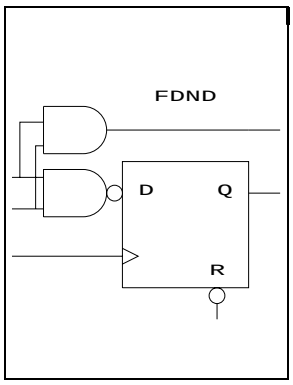
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → QN	-	-	-	2.40	2.70	3.00
CLK → QN	2.40	2.70	3.00	3.00	3.30	3.60

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	3.70	3.70	3.70	0.00	0.00	0.00

FDND - D Flip-Flop 2 Input NAND

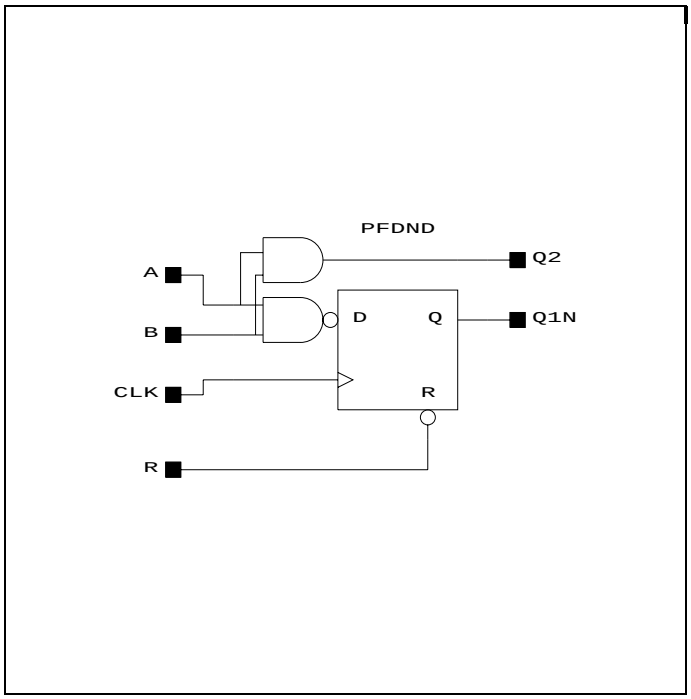
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input				Output	
R	CLK	A	B	Q1N	Q2
0	x	x	x	0	x
1	r	x	0	1	0
1	r	0	x	1	0
1	r	1	1	0	1

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q1N	1.40	1.60	1.80	1.80	2.00	2.20
R → Q1N	0.00	0.00	0.00	1.40	1.60	1.80
A → Q2	0.60	1.20	1.90	0.80	1.50	2.20
B → Q2	0.60	1.20	1.90	0.90	1.60	2.30

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
A	2.10	2.10	2.10	0.00	0.00	0.00
B	2.10	2.10	2.10	0.00	0.00	0.00

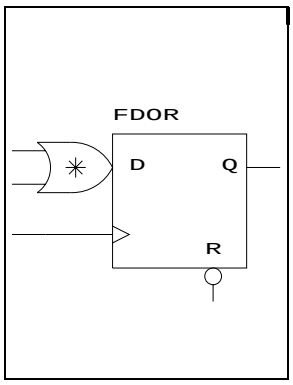
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK -> Q1N	2.40	2.70	3.00	3.00	3.30	3.60
R -> Q1N	0.00	0.00	0.00	2.40	2.70	3.00
A -> Q2	1.70	2.10	2.90	1.80	2.30	3.00
B -> Q2	1.70	2.10	2.90	2.20	2.70	3.40

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
A	3.70	3.70	3.70	0.00	0.00	0.00
B	4.10	4.10	4.10	0.00	0.00	0.00

FDOR - D Flip-Flop 2 Input OR

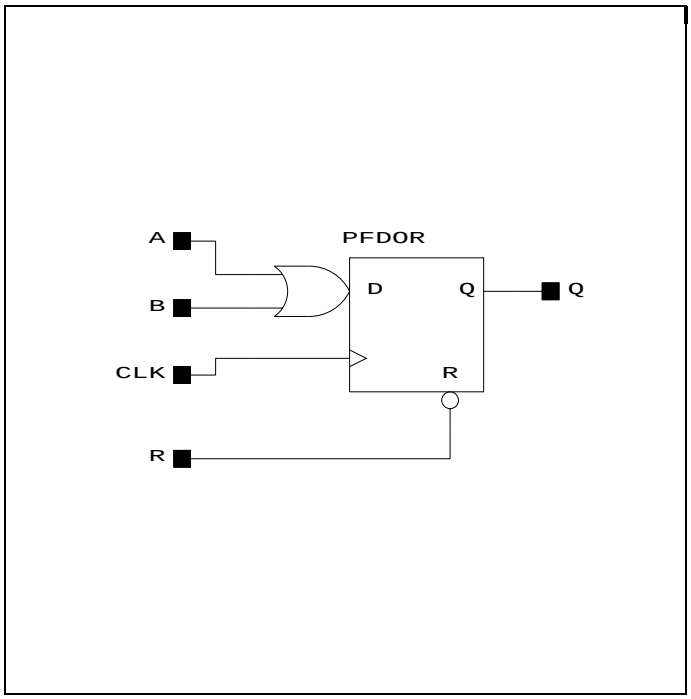
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input				Output
R	CLK	A	B	Q
0	x	x	x	0
1	r	0	b	b
1	r	1	x	1
1	r	a	0	a
1	r	x	1	1

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20
R → Q	0.00	0.00	0.00	1.40	1.60	1.80

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
A	2.10	2.10	2.10	0.00	0.00	0.00
B	2.10	2.10	2.10	0.00	0.00	0.00

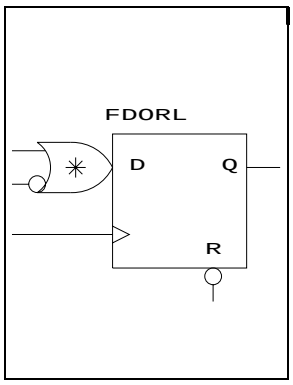
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60
R → Q	0.00	0.00	0.00	2.40	2.70	3.00

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
A	3.70	3.70	3.70	0.00	0.00	0.00
B	3.70	3.70	3.70	0.00	0.00	0.00

FDORL - D Flip-Flop (A + L')

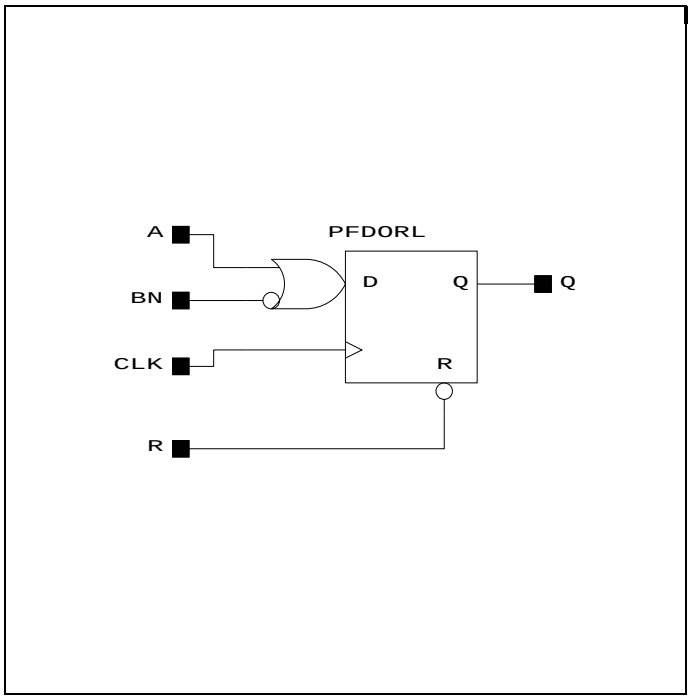
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input R	CLK	A	BN	Output Q
0	x	x	x	0
1	r	0	bn	bn'
1	r	1	x	1
1	r	x	0	1
1	r	a	1	a

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20
R → Q	0.00	0.00	0.00	1.40	1.60	1.80

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
A	2.10	2.10	2.10	0.00	0.00	0.00
BN	2.10	2.10	2.10	0.00	0.00	0.00

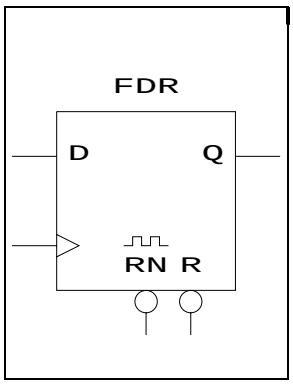
Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60
R → Q	0.00	0.00	0.00	2.40	2.70	3.00

Pin	Setup Min	Setup Typ	Setup Max	Hold Min	Hold Typ	Hold Max
A	3.70	3.70	3.70	0.00	0.00	0.00
BN	3.70	3.70	3.70	0.00	0.00	0.00

FDR - D Flip-Flop Synchronous Reset Low

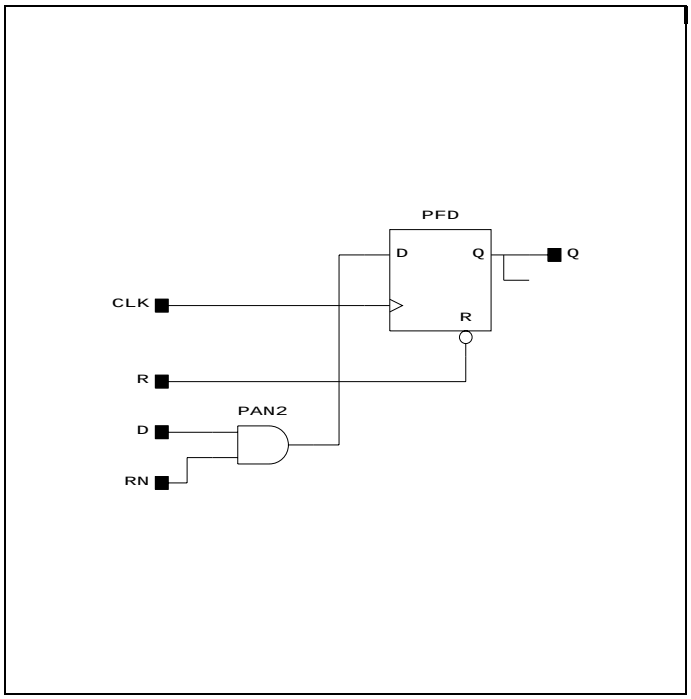
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input				Output
R	CLK	RN	D	Q
0	x	x	x	0
1	r	0	x	0
1	r	1	d	d

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.40	1.60	1.80
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RN	2.67	2.98	3.39	0.48	0.48	0.48
D	2.58	2.89	3.30	0.47	0.47	0.47

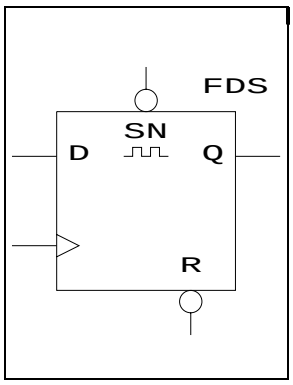
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.40	2.70	3.00
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RN	4.97	5.19	5.73	1.07	1.07	1.07
D	4.57	4.89	5.33	1.07	1.07	1.07

FDS - D Flip-Flop Synchronous Set Low

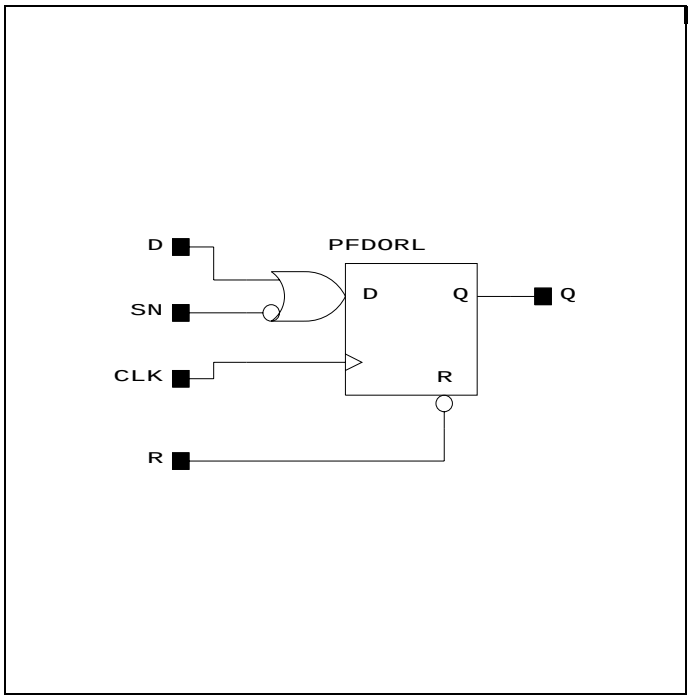
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input				Output
R	CLK	SN	D	Q
0	x	x	x	0
1	r	0	x	1
1	r	1	d	d

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20
R → Q	0.00	0.00	0.00	1.40	1.60	1.80

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	2.10	2.10	2.10	0.00	0.00	0.00
SN	2.10	2.10	2.10	0.00	0.00	0.00

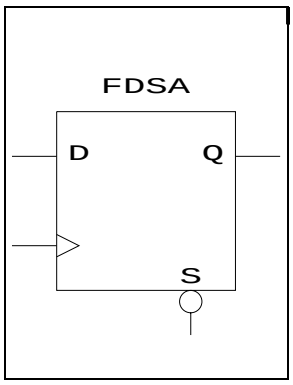
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60
R → Q	0.00	0.00	0.00	2.40	2.70	3.00

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D	3.70	3.70	3.70	0.00	0.00	0.00
SN	3.70	3.70	3.70	0.00	0.00	0.00

FDSA - D Flip-Flop Asynchronous Set Low

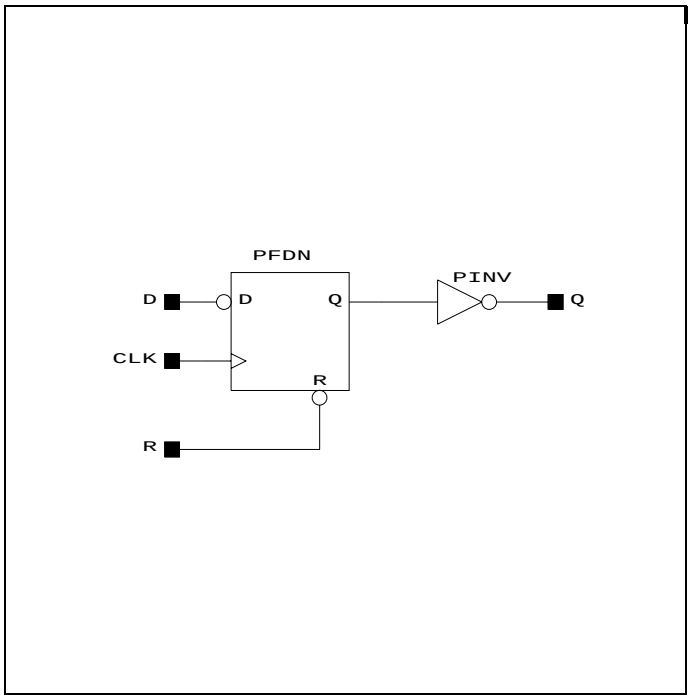
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input			Output
R	CLK	D	Q
0	x	x	1
1	r	d	d

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	2.68	3.81	4.83	-	-	-
CLK → Q.BUS	3.08	4.21	5.23	2.69	3.70	4.72
R → Q	2.28	3.31	4.23	-	-	-
CLK → Q	2.68	3.71	4.63	2.19	3.11	4.02

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	2.10	2.10	2.10	0.00	0.00	0.00

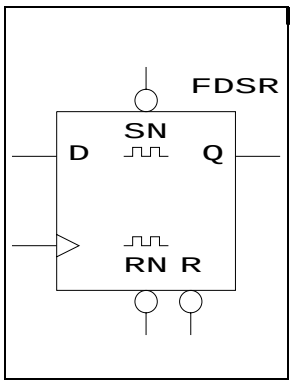
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	5.08	6.01	7.65	-	-	-
CLK → Q.BUS	5.68	6.61	8.25	5.47	6.49	8.22
R → Q	4.38	5.11	6.25	-	-	-
CLK → Q	4.98	5.71	6.85	4.47	5.29	6.42

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	3.50	3.50	3.50	0.00	0.00	0.00

FDSR - D Flip-Flop Synch Set/Reset Low

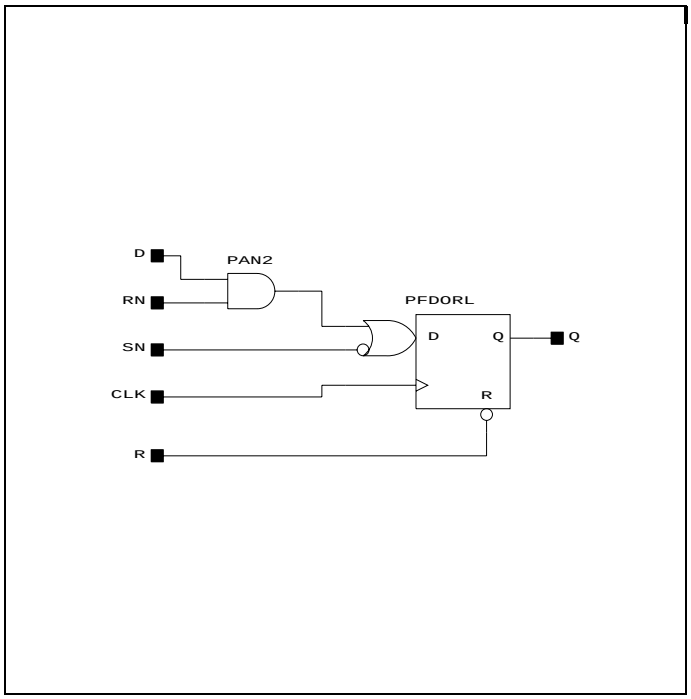
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input					Output
R	CLK	SN	RN	D	Q
0	x	x	x	x	0
1	r	1	0	x	0
1	r	0	x	x	1
1	r	1	1	d	d

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q	-	-	-	1.40	1.60	1.80
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
SN	2.10	2.10	2.10	0.00	0.00	0.00
D	2.58	2.89	3.30	0.47	0.47	0.47
RN	2.67	2.98	3.39	0.48	0.48	0.48

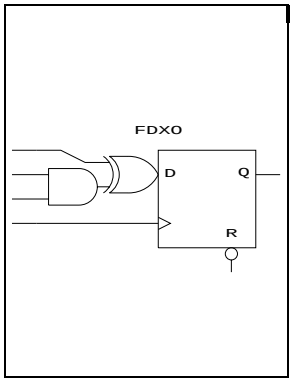
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q	-	-	-	2.40	2.70	3.00
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
SN	3.70	3.70	3.70	0.00	0.00	0.00
D	4.77	5.09	5.53	1.07	1.07	1.07
RN	5.17	5.39	5.93	1.07	1.07	1.07

FDXO - D Flip-Flop with XOR

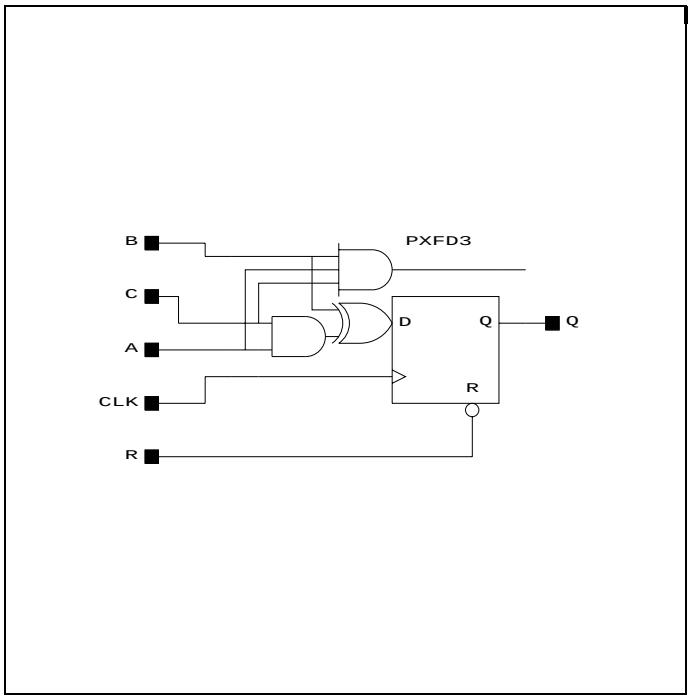
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input					Output
R	CLK	A	B	C	Q
0	x	x	x	x	0
1	r	0	b	x	b
1	r	x	b	0	b
1	r	1	b	1	b'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20
R → Q	0.00	0.00	0.00	1.40	1.60	1.80

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
A	2.10	2.10	2.10	0.00	0.00	0.00
B	2.10	2.10	2.10	0.00	0.00	0.00
C	2.10	2.10	2.10	0.00	0.00	0.00

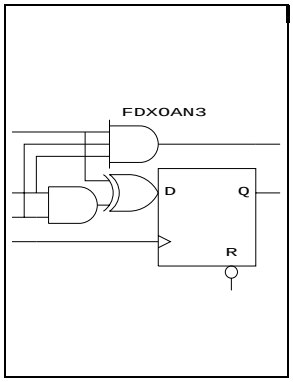
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60
R → Q	0.00	0.00	0.00	2.40	2.70	3.00

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
A	3.70	3.70	3.70	0.00	0.00	0.00
B	3.70	3.70	3.70	0.00	0.00	0.00
C	3.70	3.70	3.70	0.00	0.00	0.00

FDXOAN3 - (A*L) XOR B; B = (A*L) AND B

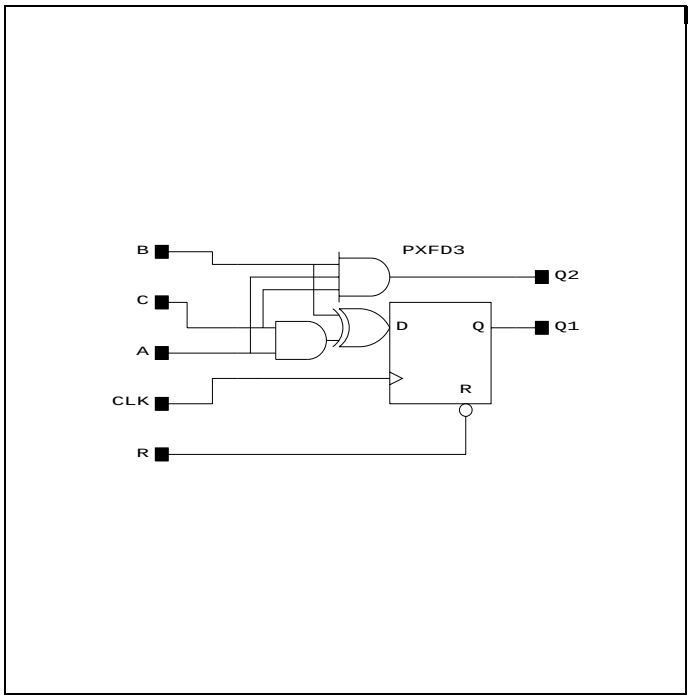
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input					Output	
R	CLK	A	C	B	Q1	Q2
0	x	x	x	x	0	x
x	x	0	x	x	x	0
x	x	x	0	x	x	0
x	x	x	x	0	x	0
1	r	0	x	b	b	x
1	r	x	0	b	b	x
1	r	1	1	b	b'	b

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q1	1.40	1.60	1.80	1.80	2.00	2.20
R → Q1	0.00	0.00	0.00	1.40	1.60	1.80
A → Q2	0.70	1.20	1.90	0.80	1.40	2.10
B → Q2	0.70	1.20	1.90	0.80	1.40	2.10
C → Q2	0.70	1.20	1.90	0.90	1.50	2.20

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
A	2.10	2.10	2.10	0.00	0.00	0.00
B	2.10	2.10	2.10	0.00	0.00	0.00
C	2.10	2.10	2.10	0.00	0.00	0.00

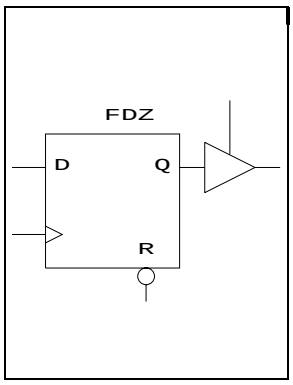
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
CLK → Q1	2.40	2.70	3.00	3.00	3.30	3.60
R → Q1	0.00	0.00	0.00	2.40	2.70	3.00
A → Q2	1.70	2.10	2.80	1.70	2.20	2.90
B → Q2	1.70	2.10	2.80	1.70	2.20	2.90
C → Q2	1.70	2.10	2.80	2.10	2.60	3.30

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
A	3.70	3.70	3.70	0.00	0.00	0.00
B	3.70	3.70	3.70	0.00	0.00	0.00
C	3.70	3.70	3.70	0.00	0.00	0.00

FDZ - D Flip-Flop with Tristate Out

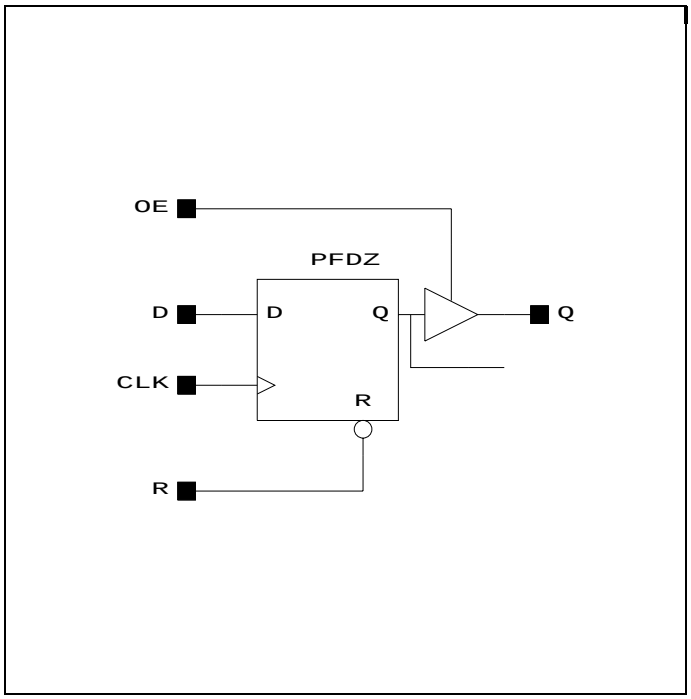
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input R	CLK	OE	D	Output Q
0	x	0	x	0
1	r	0	x	z
1	r	1	d	d

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	2.00	2.30	2.60	2.30	2.60	2.90
OE → Q	1.30	1.40	1.50	1.20	1.30	1.40
R → Q	0.60	0.70	0.80	1.90	2.20	2.50

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	2.10	2.10	2.10	0.00	0.00	0.00

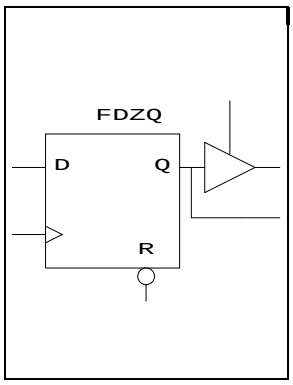
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	3.50	3.90	4.30	3.90	4.30	4.70
OE → Q	1.90	2.10	2.30	1.80	2.00	2.20
R → Q	1.10	1.20	1.30	3.30	3.70	4.10

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	3.70	3.70	3.70	0.00	0.00	0.00

FDZQ - D Flip-Flop with Tristate Out and Q Out

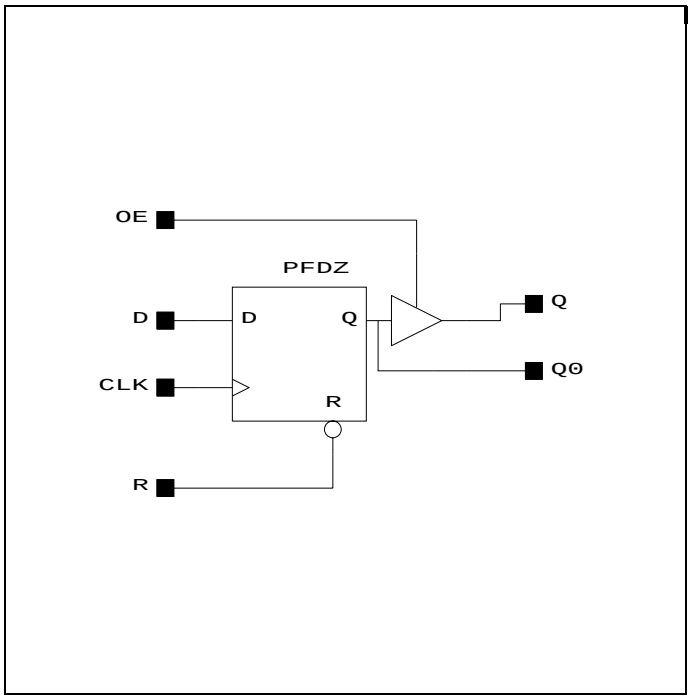
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input				Output	
R	CLK	OE	D	Q0	Q
0	x	x	x	0	0
1	r	0	x	x	z
1	r	1	d	d	d

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q0	1.40	1.60	1.80	1.80	2.00	2.20
R → Q0	0.00	0.00	0.00	1.40	1.60	1.80
CLK → Q	2.00	2.30	2.60	2.30	2.60	2.90
OE → Q	1.30	1.40	1.50	1.20	1.30	1.40
R → Q	0.60	0.70	0.80	1.90	2.20	2.50

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	2.10	2.10	2.10	0.00	0.00	0.00

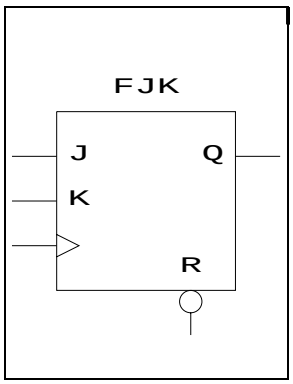
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
CLK → Q0	2.40	2.70	3.00	3.00	3.30	3.60
R → Q0	0.00	0.00	0.00	2.40	2.70	3.00
CLK → Q	3.50	3.90	4.30	3.90	4.30	4.70
OE → Q	1.90	2.10	2.30	1.80	2.00	2.20
R → Q	1.10	1.20	1.30	3.30	3.70	4.10

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D	3.70	3.70	3.70	0.00	0.00	0.00

FJK - JK Flip-Flop Synchronous

Symbol



Rectangular Area: 2x4cells

Number of Cells: 8

Truth Table

Input				Output
R	CLK	J	K	Q
0	x	x	x	0
1	r	0	0	q
1	r	0	1	0
1	r	1	0	1
1	r	1	1	q'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.64	1.93	2.19
CLK → Q	1.67	1.91	2.16	2.04	2.33	2.59

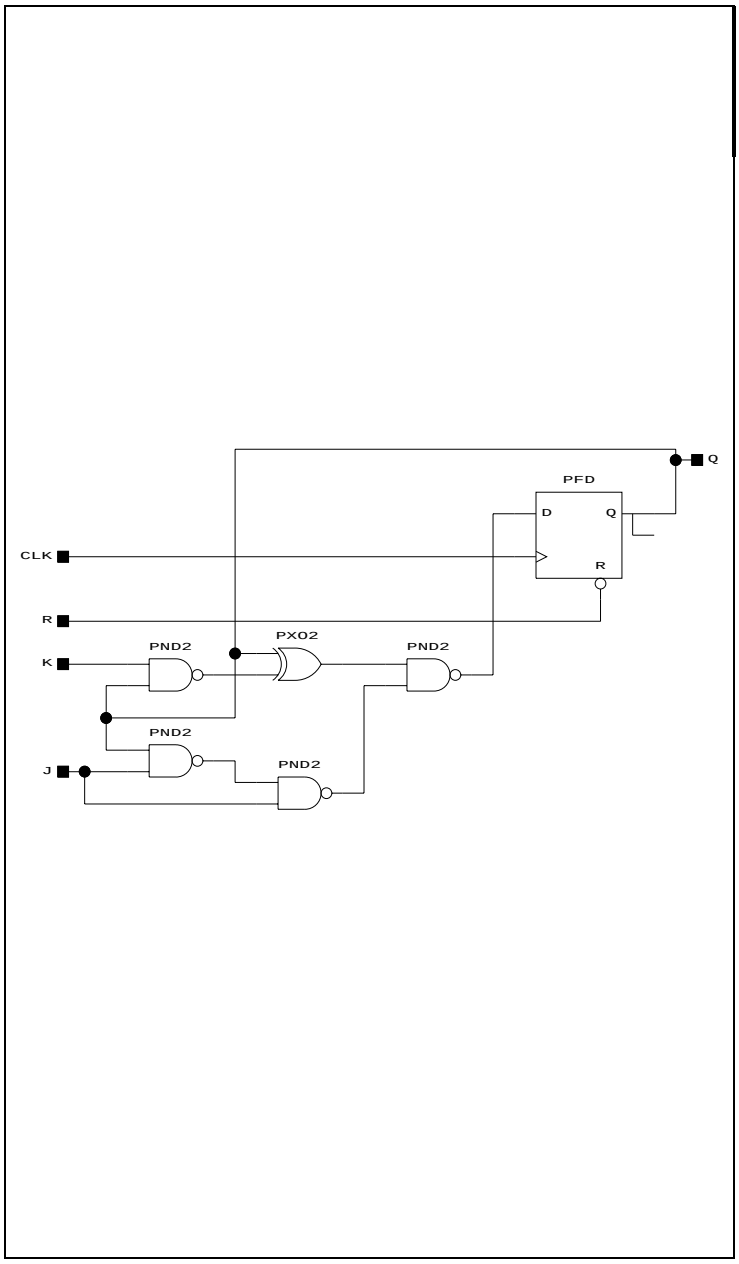
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
K	5.69	8.22	11.35	3.35	3.35	3.35
J	5.11	7.34	10.07	2.12	2.12	2.12

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.64	3.03	3.46
CLK → Q	2.62	2.97	3.36	3.24	3.63	4.06

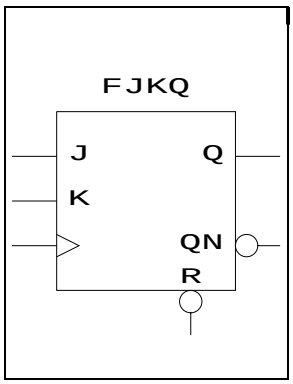
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
K	11.73	13.93	17.53	7.64	7.64	7.64
J	10.06	11.74	14.49	4.70	4.70	4.70

Schematic



FJKQ - JK Flip-Flop Synchronous with Q Low

Symbol



Rectangular Area: 3x4cells

Number of Cells: 10

Truth Table

Input				Output	
R	CLK	J	K	Q	QN
0	x	x	x	0	1
1	r	0	0	q	q'
1	r	0	1	0	1
1	r	1	0	1	0
1	r	1	1	q'	q

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.72	2.04	2.32
CLK → Q	1.76	2.02	2.28	2.12	2.44	2.72
R → QN.BUS	3.39	4.92	6.41	-	-	-
CLK → QN.BUS	3.79	5.32	6.81	3.44	4.81	6.28
R → QN	2.99	4.42	5.81	-	-	-
CLK → QN	3.39	4.82	6.21	2.94	4.21	5.58

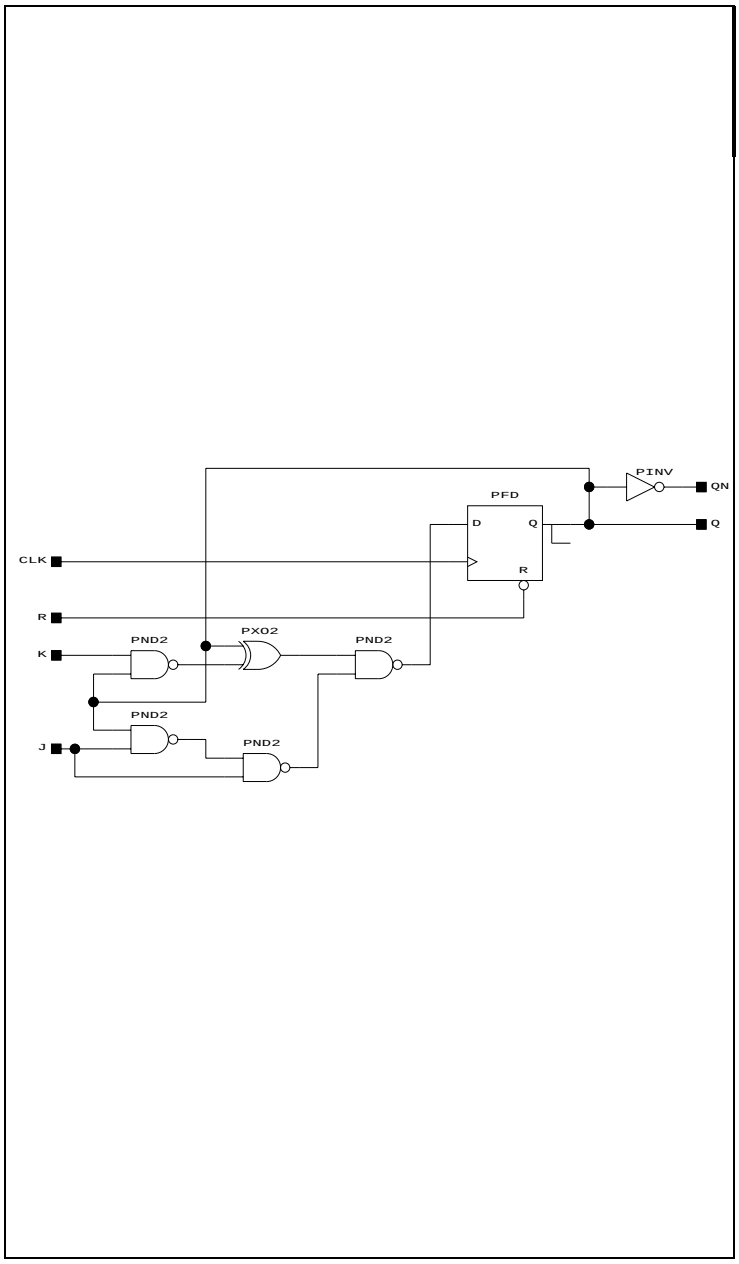
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
J	5.11	7.34	10.07	2.12	2.12	2.12
K	5.69	8.22	11.35	3.35	3.35	3.35

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.72	3.14	3.62
CLK → Q	2.69	3.06	3.48	3.32	3.74	4.22
R → QN.BUS	6.40	7.63	9.95	-	-	-
CLK → QN.BUS	7.00	8.23	10.55	6.76	8.15	10.40
R → QN	5.70	6.73	8.55	-	-	-
CLK → QN	6.30	7.33	9.15	5.76	6.95	8.60

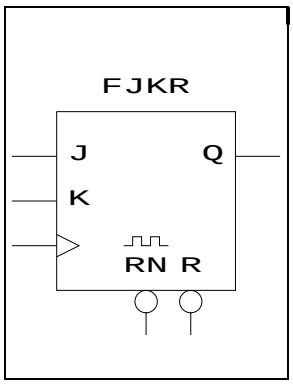
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
J	10.06	11.74	14.49	4.70	4.70	4.70
K	11.73	13.93	17.53	7.64	7.64	7.64

Schematic



FJKR - JK Flip-Flop Synchronous Reset Low

Symbol



Rectangular Area: 3x4cells

Number of Cells: 11

Truth Table

Input					Output
R	CLK	RN	J	K	Q
0	x	x	x	x	0
1	r	0	x	x	0
1	r	1	0	0	q
1	r	1	0	1	0
1	r	1	1	0	1
1	r	1	1	1	q'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.56	1.82	2.06
CLK → Q	1.58	1.81	2.04	1.96	2.22	2.46

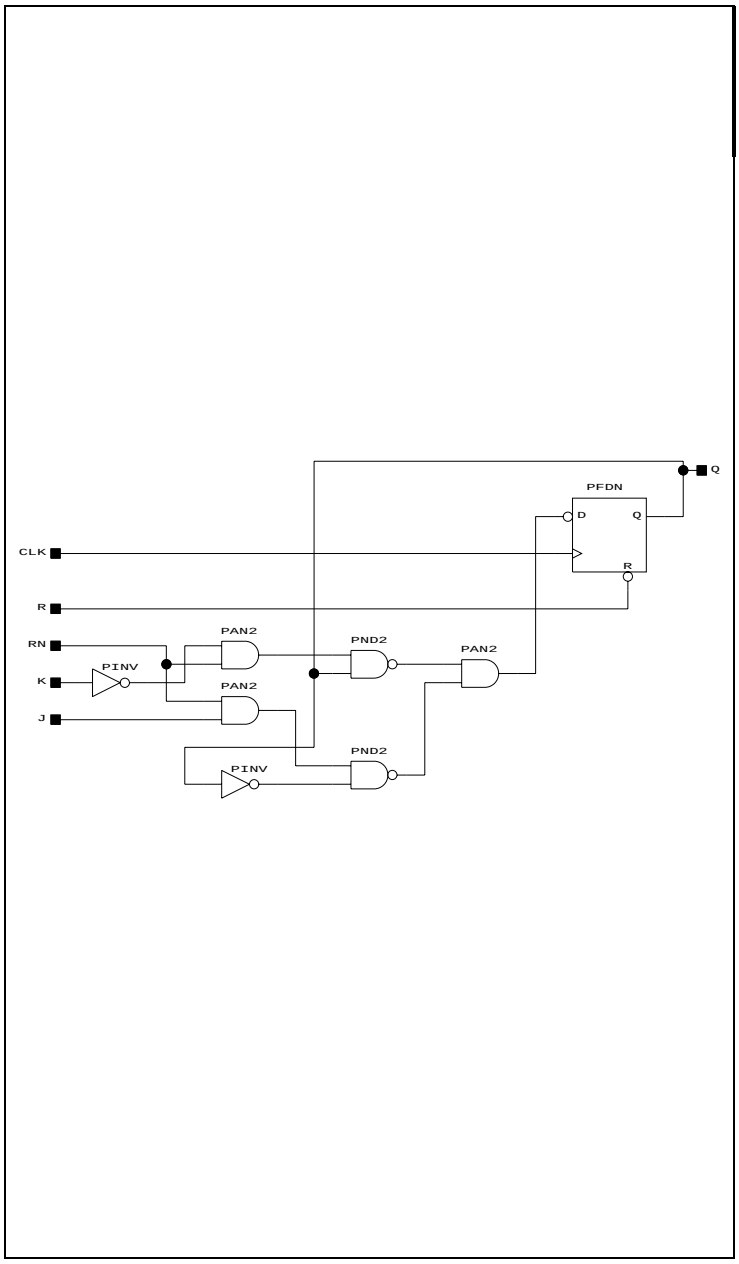
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
K	5.89	8.85	12.22	3.77	3.77	3.77
RN	5.59	8.15	11.20	2.91	2.91	2.91
J	5.59	8.15	11.20	3.37	3.37	3.37

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.56	2.92	3.31
CLK → Q	2.54	2.88	3.24	3.16	3.52	3.91

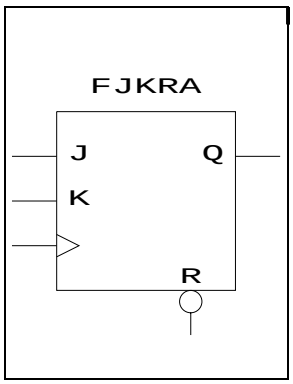
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
K	11.93	14.07	17.79	8.32	8.32	8.32
RN	11.24	13.17	16.51	6.46	6.46	6.46
J	11.24	13.17	16.51	7.63	7.63	7.63

Schematic



FJKRA - JK Flip-Flop Asynchronous Reset Low

Symbol



Rectangular Area: 3x4cells

Number of Cells: 8

Truth Table

Input				Output
R	CLK	J	K	Q
0	x	x	x	0
1	r	0	0	q
1	r	0	1	0
1	r	1	0	1
1	r	1	1	q'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.64	1.93	2.19
CLK → Q	1.67	1.91	2.16	2.04	2.33	2.59

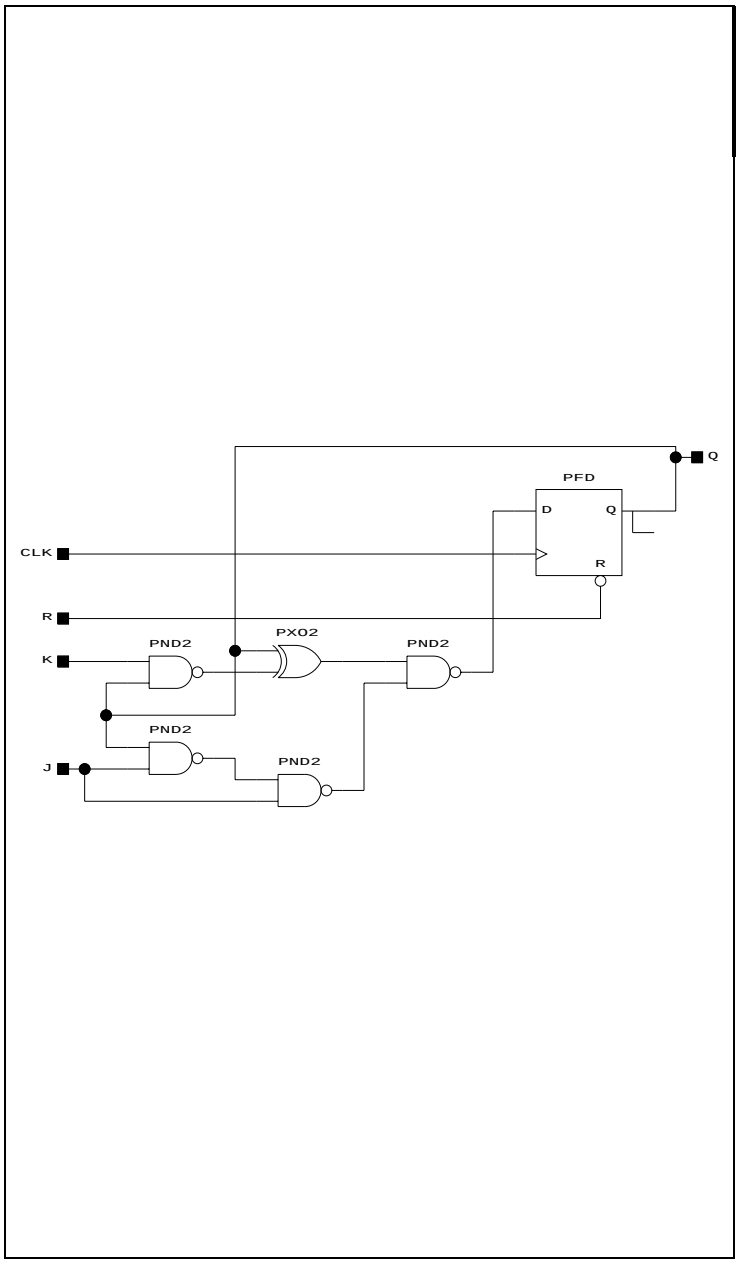
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
K	5.69	8.22	11.35	3.35	3.35	3.35
J	5.11	7.34	10.07	2.12	2.12	2.12

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.64	3.03	3.46
CLK → Q	2.62	2.97	3.36	3.24	3.63	4.06

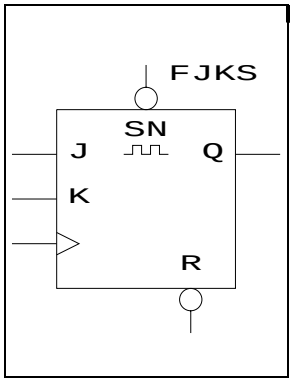
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
K	11.73	13.93	17.53	7.64	7.64	7.64
J	10.06	11.74	14.49	4.70	4.70	4.70

Schematic



FJKS - JK Flip-Flop Synchronous Set Low

Symbol



Rectangular Area: 3x4cells

Number of Cells: 10

Truth Table

Input					Output
R	CLK	SN	J	K	Q
0	x	x	x	x	0
1	r	0	x	x	1
1	r	1	0	0	q
1	r	1	0	1	0
1	r	1	1	0	1
1	r	1	1	1	q'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.56	1.82	2.06
CLK → Q	1.58	1.81	2.04	1.96	2.22	2.46

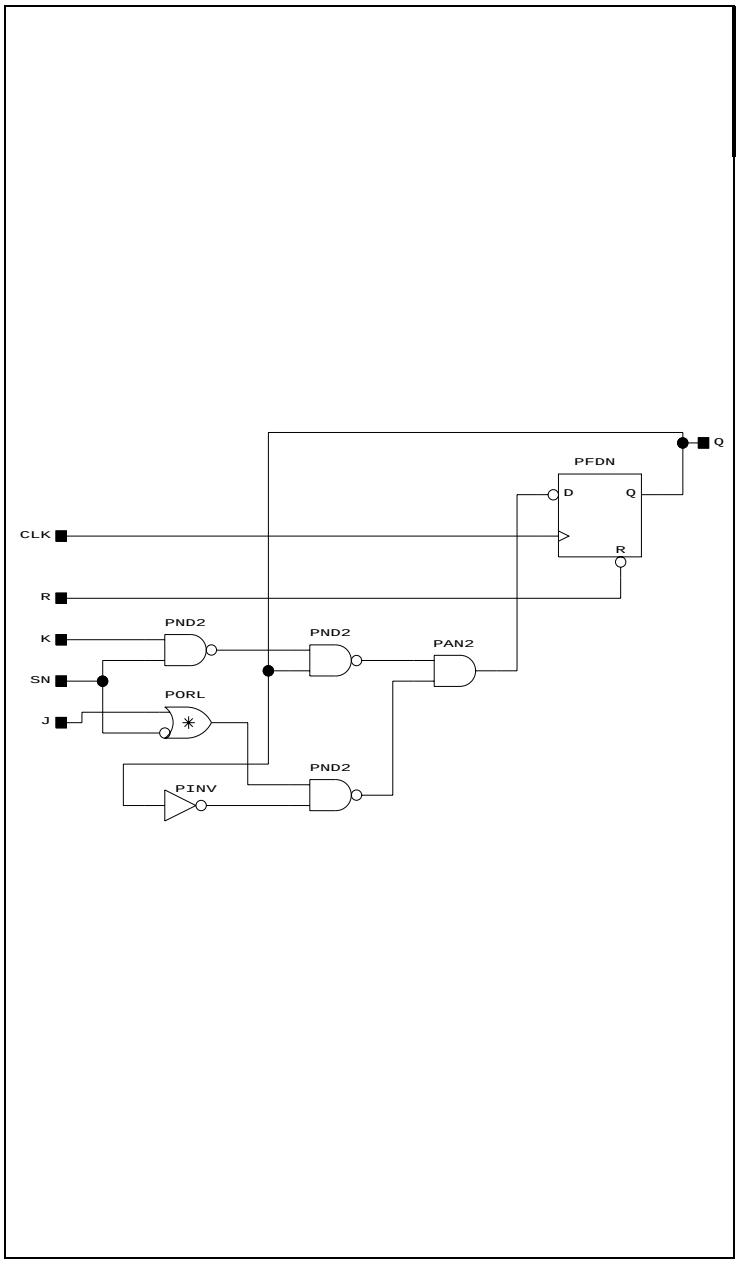
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
K	5.21	7.57	10.22	2.88	2.88	2.88
SN	5.67	8.34	11.31	2.88	2.88	2.88
J	5.66	8.34	11.31	3.47	3.47	3.47

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.56	2.92	3.31
CLK → Q	2.54	2.88	3.24	3.16	3.52	3.91

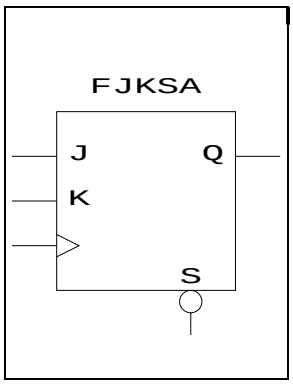
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
K	10.16	11.88	14.77	6.44	6.44	6.44
SN	12.21	14.33	18.04	6.44	6.44	6.44
J	11.81	13.93	17.64	7.84	7.84	7.84

Schematic



FJKSA - JK Flip-Flop Asynchronous Set Low

Symbol



Rectangular Area: 3x4cells

Number of Cells: 10

Truth Table

Input				Output
S	**CLK**	**J**	**K**	**Q**
0	x	x	x	1
1	r	0	0	q
1	r	0	1	1
1	r	1	0	0
1	r	1	1	q'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
S → Q.BUS	2.68	3.81	4.83	-	-	-
CLK → Q.BUS	3.08	4.21	5.23	2.69	3.70	4.72
S → Q	2.35	3.39	4.32	-	-	-
CLK → Q	2.75	3.79	4.72	2.26	3.18	4.11

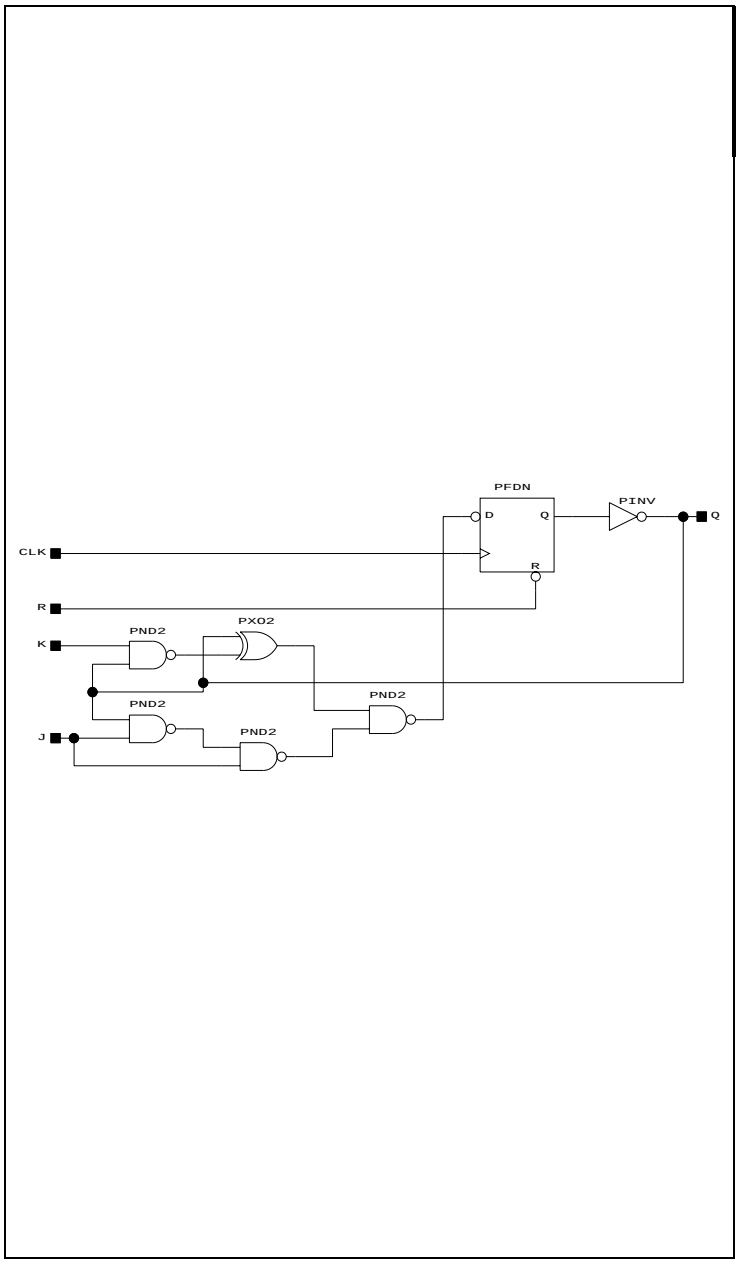
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
J	5.19	7.42	10.16	2.19	2.19	2.19
K	5.77	8.31	11.44	3.42	3.42	3.42

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
S → Q.BUS	5.08	6.01	7.65	-	-	-
CLK → Q.BUS	5.68	6.61	8.25	5.47	6.49	8.22
S → Q	4.45	5.20	6.36	-	-	-
CLK → Q	5.05	5.80	6.96	4.54	5.37	6.54

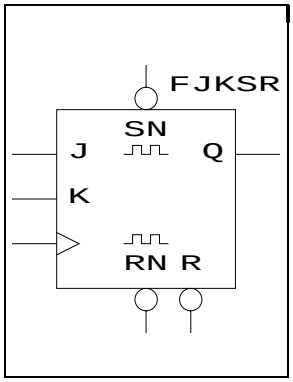
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
J	10.03	11.83	14.63	4.67	4.67	4.67
K	11.81	13.92	17.64	7.61	7.61	7.61

Schematic



FJKSR - JK Flip-Flop Synch Set/Reset Low

Symbol



Rectangular Area: 3x4cells

Number of Cells: 12

Truth Table

Input						Output
R	CLK	RN	SN	J	K	Q
0	x	x	x	x	x	0
1	r	x	0	x	x	1
1	r	0	1	x	x	0
1	r	1	1	0	0	q
1	r	1	1	0	1	0
1	r	1	1	1	0	1
1	r	1	1	1	1	q'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.56	1.82	2.06
CLK → Q	1.58	1.81	2.04	1.96	2.22	2.46

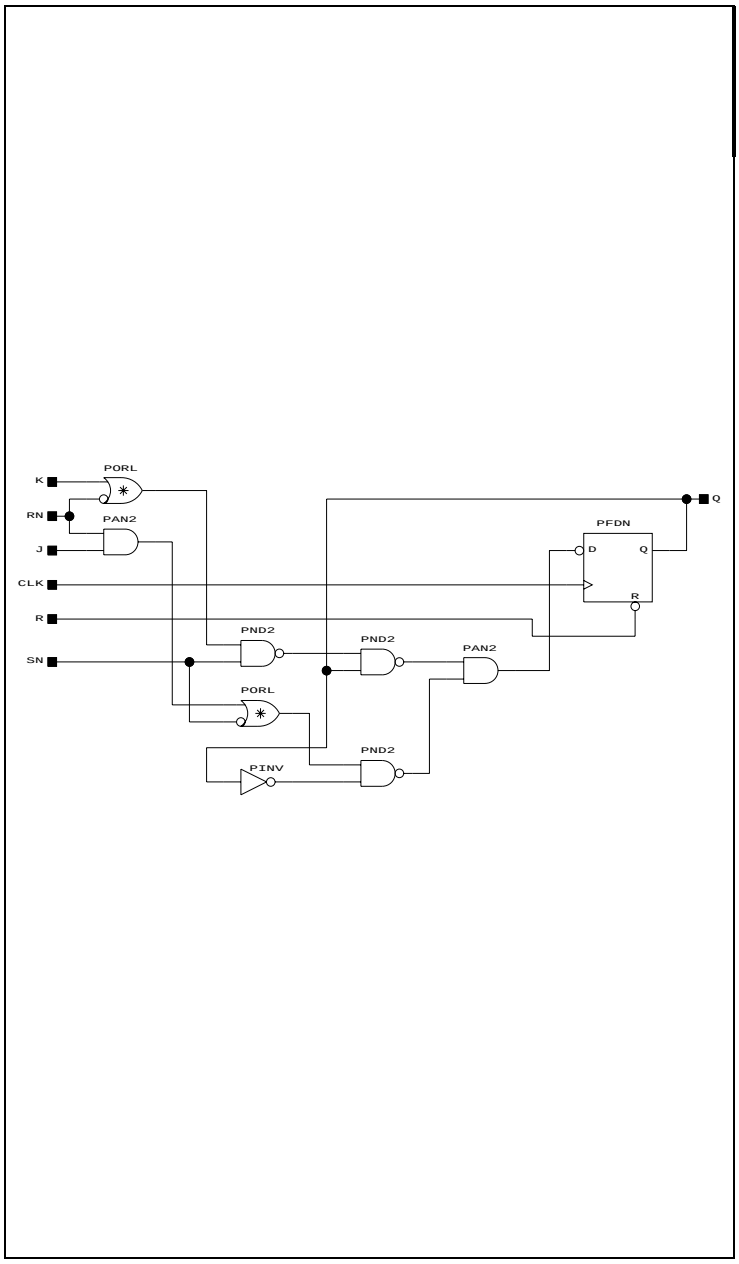
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RN	6.18	9.24	12.61	3.75	3.75	3.75
J	6.14	9.12	12.51	3.94	3.94	3.94
K	6.08	9.15	12.51	3.75	3.75	3.75
SN	5.67	8.34	11.31	2.88	2.88	2.88

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.56	2.92	3.31
CLK → Q	2.54	2.88	3.24	3.16	3.52	3.91

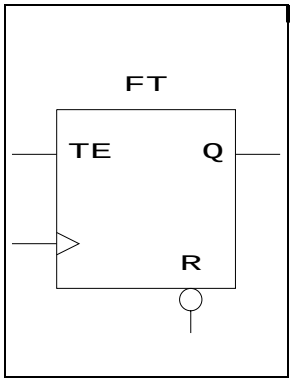
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RN	13.29	15.62	19.87	8.31	8.31	8.31
J	12.89	15.22	19.47	8.91	8.91	8.91
K	12.72	15.06	19.09	8.31	8.31	8.31
SN	12.21	14.33	18.04	6.44	6.44	6.44

Schematic


K
RN
J
CLK
R
SN
PORL
PAN2
PND2
PND2
PAN2
PORL
PND2
PINV
PFDN
D
Q
R
Q

FT - T Flip-Flop Synchronous

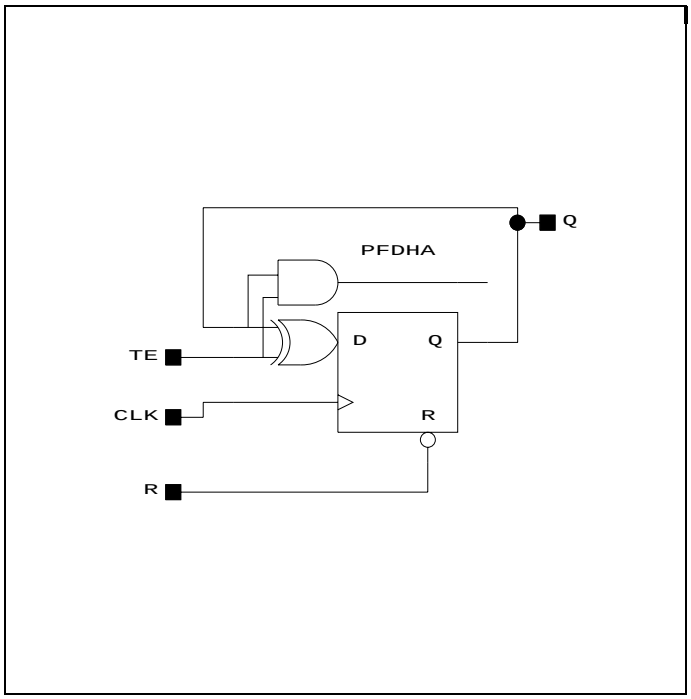
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input R	CLK	TE	Output Q
0	x	x	0
1	r	0	q
1	r	1	q'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.48	1.71	1.93
CLK → Q	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
TE	2.10	2.10	2.10	0.00	0.00	0.00

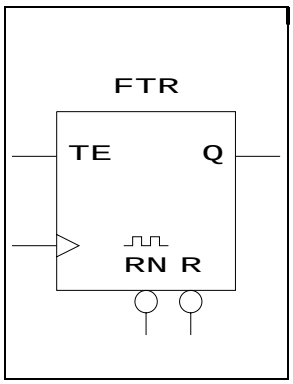
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.48	2.81	3.15
CLK → Q	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
TE	3.50	3.50	3.50	0.00	0.00	0.00

FTR - T Flip-Flop Synchronous Reset Low

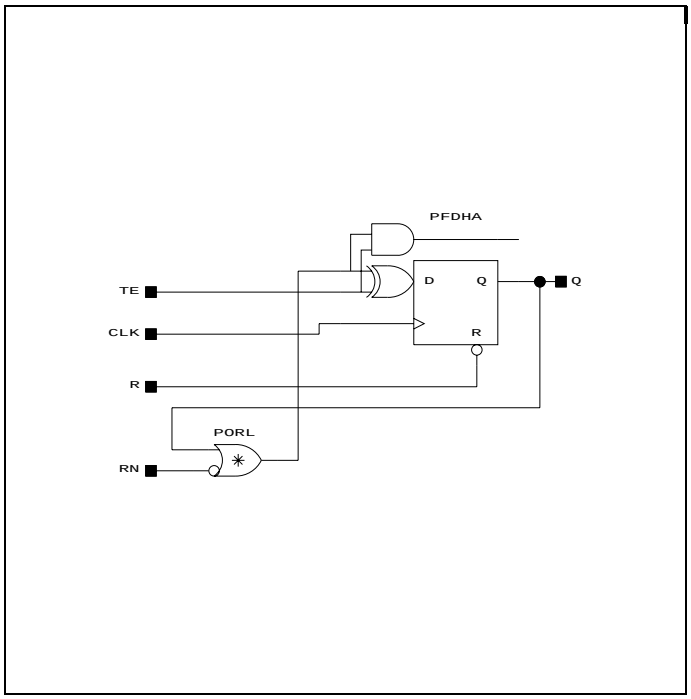
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input				Output
R	CLK	TE	RN	Q
0	x	x	x	0
1	x	0	1	q
1	r	1	0	0
1	r	1	1	q'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.48	1.71	1.93
CLK → Q	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RN	3.07	3.78	4.49	0.87	0.87	0.87
TE	2.10	2.10	2.10	0.00	0.00	0.00

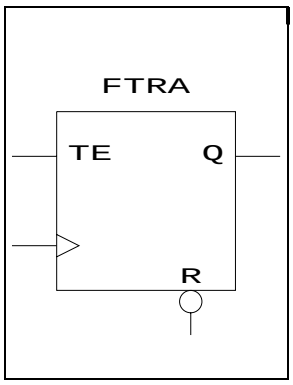
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.48	2.81	3.15
CLK → Q	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RN	6.46	7.08	8.22	1.87	1.87	1.87
TE	3.50	3.50	3.50	0.00	0.00	0.00

FTRA - T Flip-Flop Asynchronous Reset Low

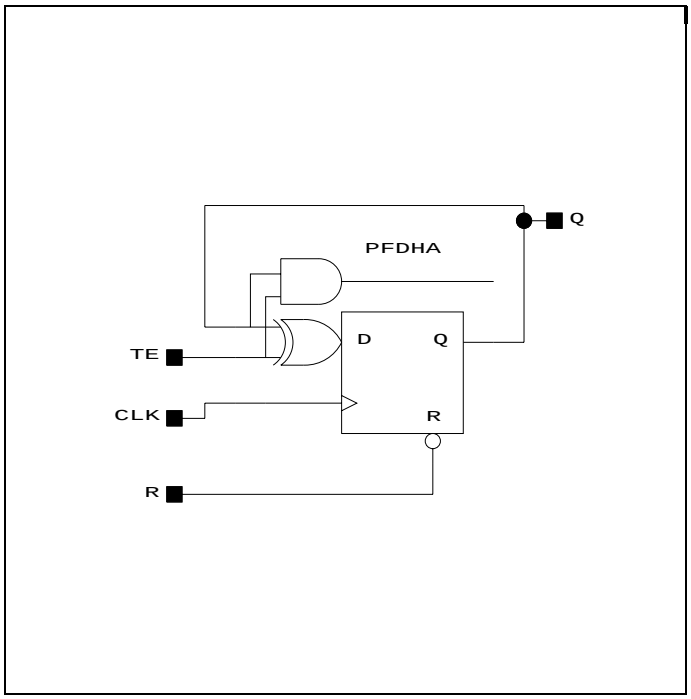
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input			Output
R	CLK	TE	Q
0	x	x	0
1	r	0	q
1	r	1	q'

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.48	1.71	1.93
CLK → Q	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
TE	2.10	2.10	2.10	0.00	0.00	0.00

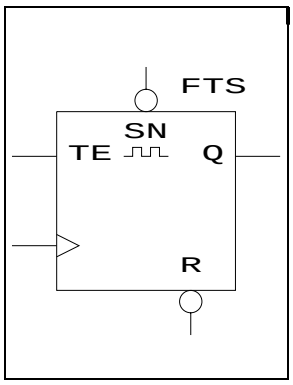
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.48	2.81	3.15
CLK → Q	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
TE	3.50	3.50	3.50	0.00	0.00	0.00

FTS - T Flip-Flop Synchronous Set Low

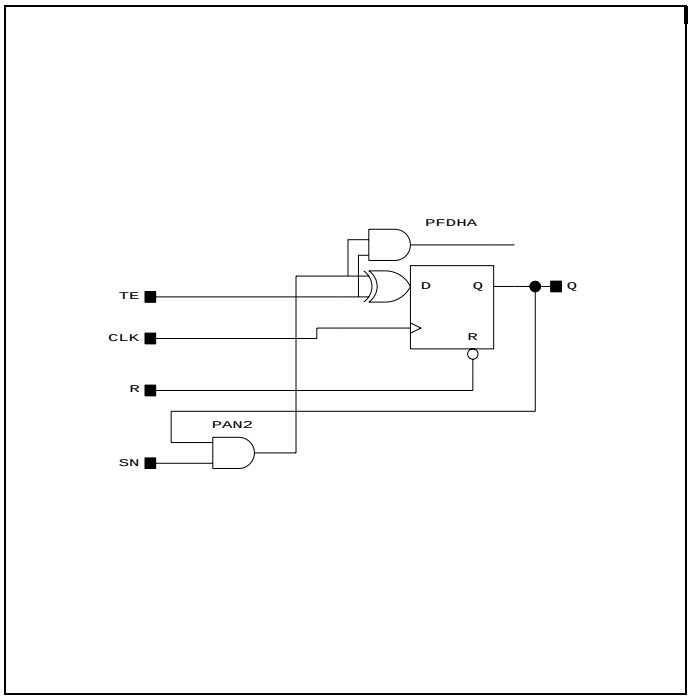
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input R	CLK	TE	SN	Output Q
0	x	x	x	0
1	r	1	0	1
1	r	0	0	0
1	r	1	1	q'
1	r	0	1	q

Switching Speeds for -2ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.48	1.71	1.93
CLK → Q	1.49	1.71	1.92	1.88	2.11	2.33

Pin	Setup Min	Setup Typ	Setup Max	Hold Min	Hold Typ	Hold Max
SN	2.67	2.98	3.39	0.48	0.48	0.48
TE	2.10	2.10	2.10	0.00	0.00	0.00

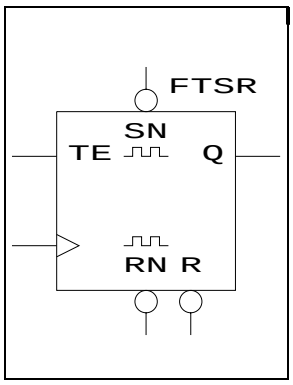
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.48	2.81	3.15
CLK → Q	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
SN	4.97	5.19	5.73	1.07	1.07	1.07
TE	3.50	3.50	3.50	0.00	0.00	0.00

FTSR - T Flip-Flop Synchronous Set/Reset Low

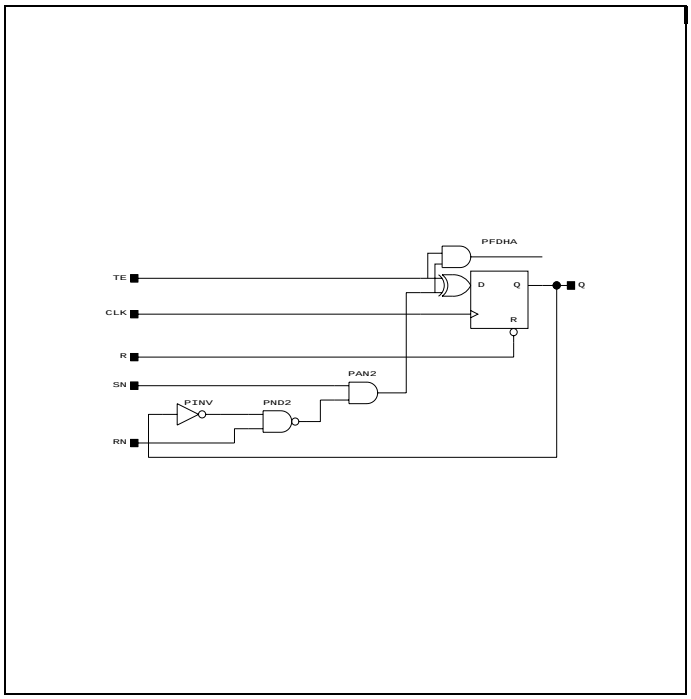
Symbol



Rectangular Area: 2x2cells

Number of Cells: 4

Schematic



Truth Table

Input					Output
R	CLK	TE	RN	SN	Q
0	x	x	x	x	0
1	r	1	1	1	q'
1	r	0	1	1	q
1	r	1	x	0	1
1	r	0	x	0	0
1	r	1	0	1	0
1	r	0	0	1	1

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	1.90	2.20	2.50
CLK → Q.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q	-	-	-	1.48	1.71	1.93
CLK → Q	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RN	3.76	5.19	6.62	1.56	1.56	1.56
SN	2.99	3.70	4.42	0.68	0.68	0.68
TE	2.10	2.10	2.10	0.00	0.00	0.00

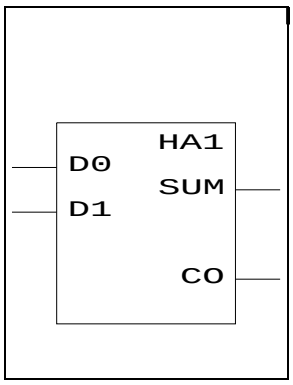
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q.BUS	-	-	-	3.40	3.90	4.80
CLK → Q.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q	-	-	-	2.48	2.81	3.15
CLK → Q	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
RN	7.24	8.29	9.78	3.54	3.54	3.54
SN	5.38	5.91	6.65	1.77	1.77	1.77
TE	3.50	3.50	3.50	0.00	0.00	0.00

HA1 - 1-Bit Half Adder

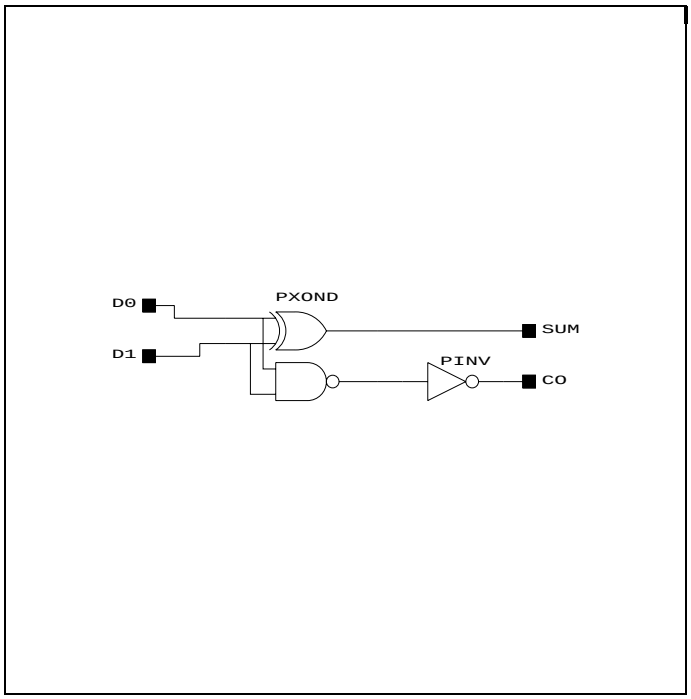
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input		Output	
D0	D1	SUM	CO
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Switching Speeds for -2ns Parts

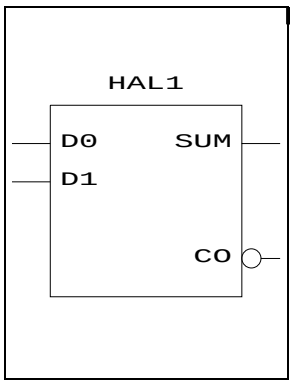
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D1 → CO	1.57	2.88	4.30	1.68	2.88	4.39
D0 → CO	1.57	2.88	4.30	1.68	2.88	4.39
D1 → SUM.BUS	1.20	1.90	2.70	1.30	2.10	2.90
D0 → SUM.BUS	1.20	1.90	2.70	1.30	2.10	2.90
D1 → SUM	0.80	1.40	2.10	0.80	1.50	2.20
D0 → SUM	0.80	1.40	2.10	0.80	1.50	2.20

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D1 → CO	3.66	4.58	6.12	3.56	4.39	6.02
D0 → CO	3.66	4.58	6.12	3.56	4.39	6.02
D1 → SUM.BUS	2.50	3.20	4.50	3.50	4.30	6.00
D0 → SUM.BUS	2.50	3.20	4.50	3.50	4.30	6.00
D1 → SUM	1.80	2.30	3.10	2.50	3.10	4.20
D0 → SUM	1.80	2.30	3.10	2.50	3.10	4.20

HAL1 - 1-Bit Half Adder Carry Low

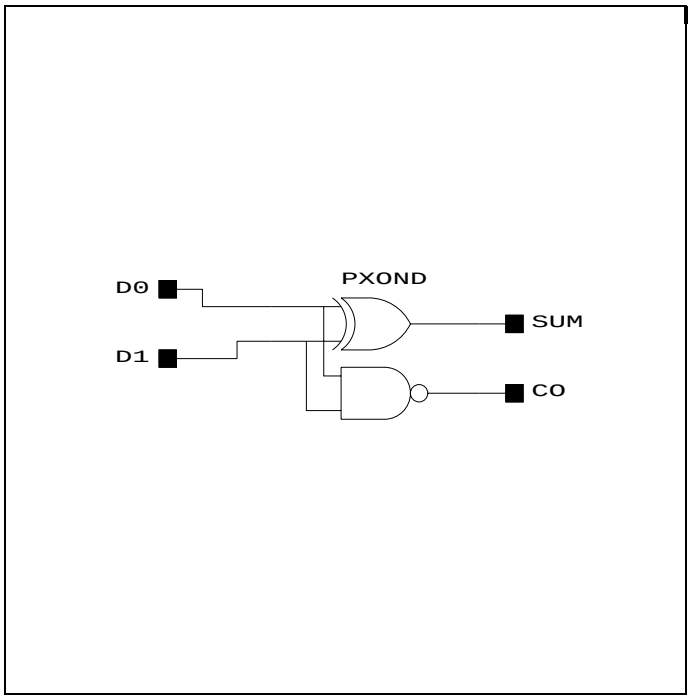
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
D0	D1	SUM	CO
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	0

Switching Speeds for -2ns Parts

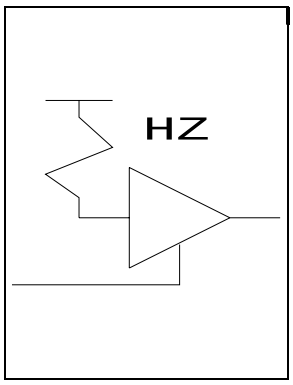
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D0 → SUM	0.80	1.40	2.10	0.80	1.50	2.20
D1 → SUM	0.80	1.40	2.10	0.80	1.50	2.20
D0 → SUM.BUS	1.20	1.90	2.70	1.30	2.10	2.90
D1 → SUM.BUS	1.20	1.90	2.70	1.30	2.10	2.90
D0 → CO	0.80	1.40	2.20	0.70	1.40	2.10
D1 → CO	0.80	1.40	2.20	0.70	1.40	2.10

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D0 → SUM	1.80	2.30	3.10	2.50	3.10	4.20
D1 → SUM	1.80	2.30	3.10	2.50	3.10	4.20
D0 → SUM.BUS	2.50	3.20	4.50	3.50	4.30	6.00
D1 → SUM.BUS	2.50	3.20	4.50	3.50	4.30	6.00
D0 → CO	1.70	2.10	2.90	1.80	2.30	3.00
D1 → CO	1.70	2.10	2.90	1.80	2.30	3.00

HZ - Bus Driver High or Z

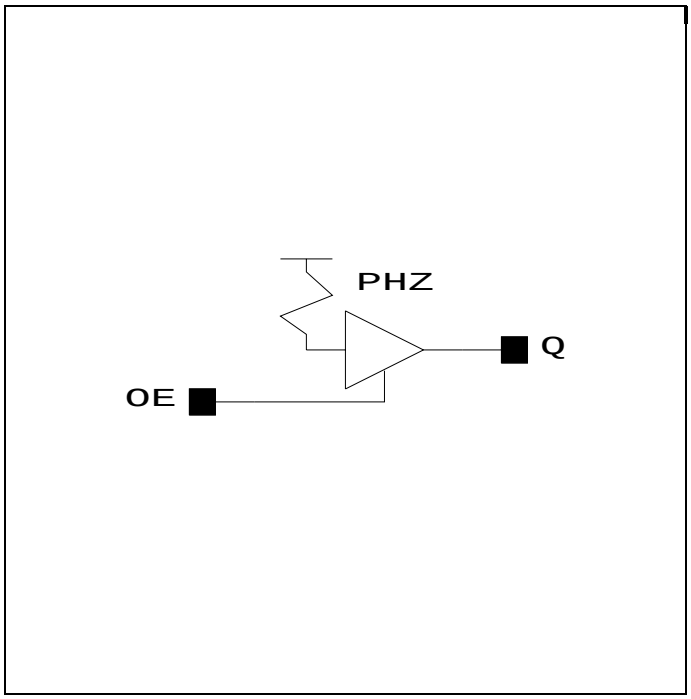
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input OE	Output Q
0	z
1	1

Switching Speeds for -2ns Parts

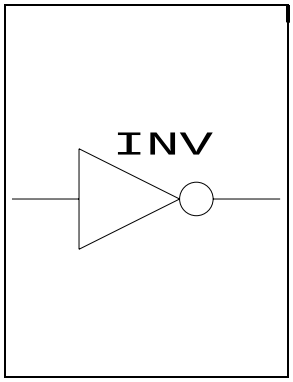
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q	0.70	1.30	2.20	0.00	0.00	0.00

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q	2.10	2.70	3.90	0.00	0.00	0.00

INV - Inverter

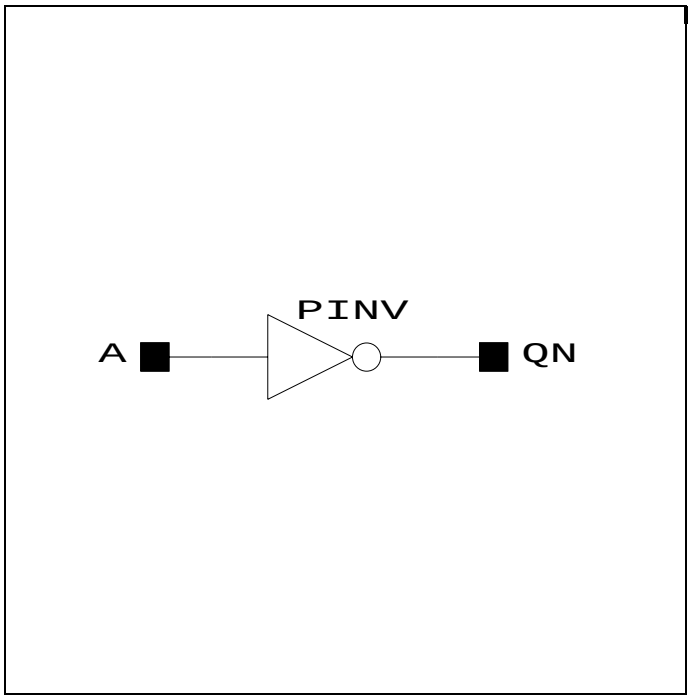
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input A	Output QN
a	a'

Switching Speeds for -2ns Parts

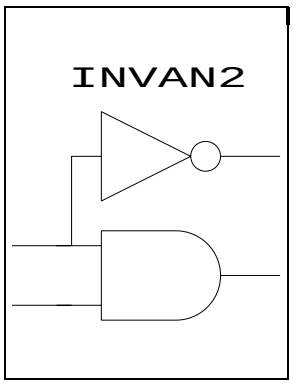
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	0.70	1.10	1.50	0.90	1.30	1.70

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	1.50	1.80	2.30	1.70	2.00	2.40

INVAN2 - Inverter and 2-Input AND L', (A*L)

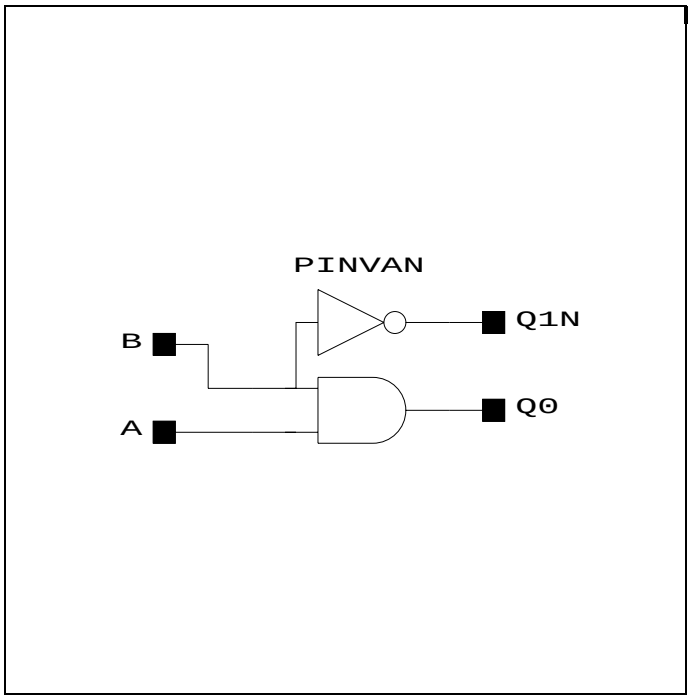
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	B	Q0	Q1N
0	0	0	1
0	1	0	0
1	0	0	1
1	1	1	0

Switching Speeds for -2ns Parts

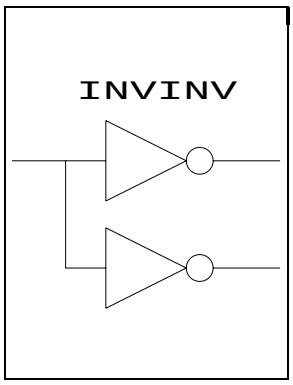
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q0	0.40	0.70	1.10	0.40	0.70	1.10
B → Q0	0.40	0.70	1.10	0.50	0.80	1.20
B → Q1N	0.70	1.10	1.50	0.90	1.30	1.70

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q0	1.00	1.30	1.70	1.00	1.20	1.60
B → Q0	1.00	1.30	1.70	1.40	1.60	2.00
B → Q1N	1.60	1.90	2.40	1.70	2.00	2.50

INVINV - Twin Inverters

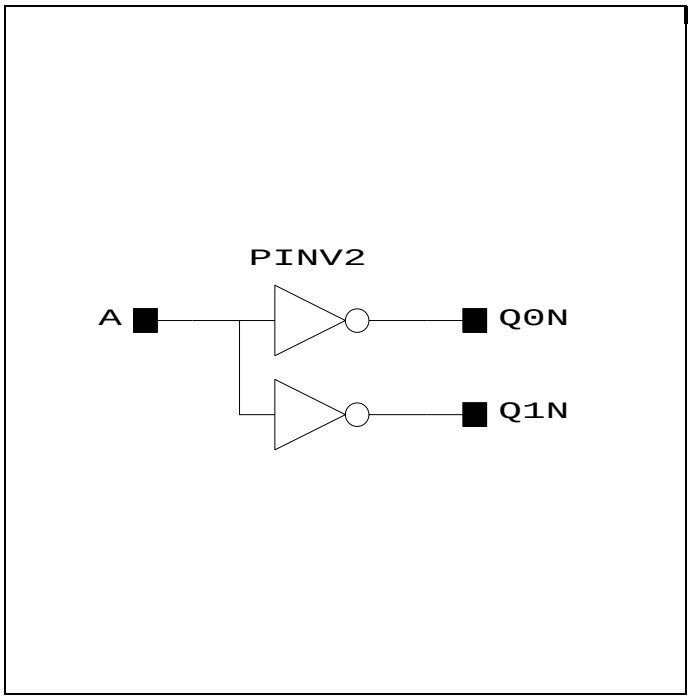
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input	Output	
A	Q0	Q1N
a	a'	a'

Switching Speeds for -2ns Parts

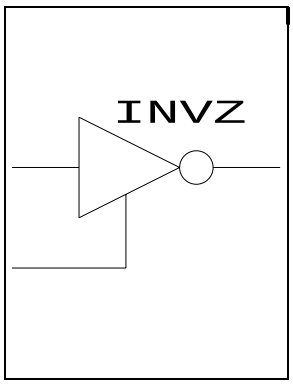
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q0N	0.80	1.40	2.10	0.90	1.60	2.30
A → Q1N	0.80	1.40	2.10	0.90	1.50	2.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q0N	1.80	2.30	3.10	2.90	3.50	4.60
A → Q1N	1.80	2.20	3.00	2.20	2.60	3.40

INVZ - Tristate Inverter

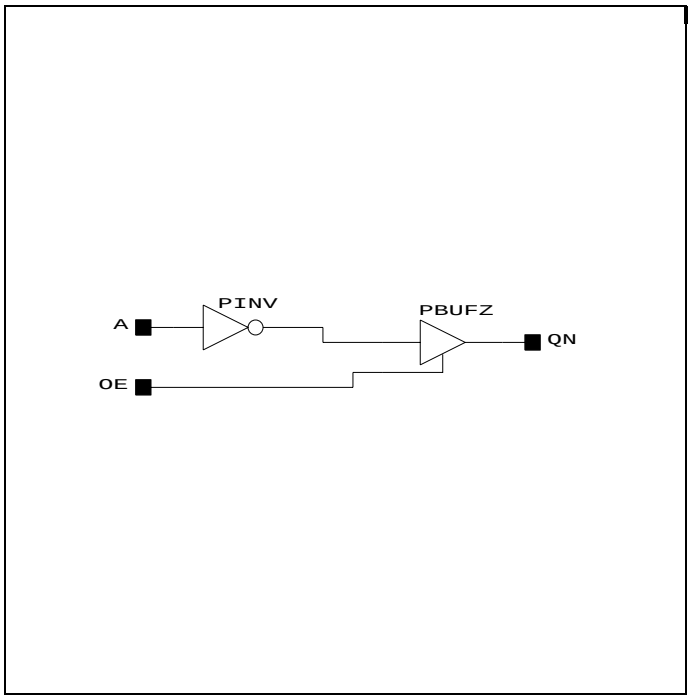
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input OE	A	Output QN
0	x	z
1	a	a'

Switching Speeds for -2ns Parts

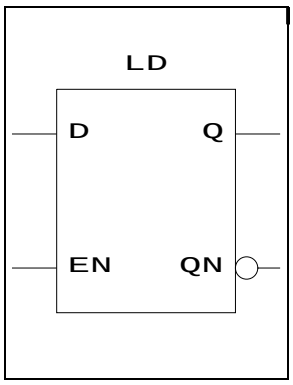
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
OE → QN	0.80	1.41	2.38	0.94	1.67	2.63
A → QN	2.24	3.77	5.36	2.28	3.83	5.41

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
OE → QN	2.27	2.91	4.20	3.22	4.07	5.77
A → QN	4.81	5.89	8.12	5.85	7.23	9.92

LD - D Latch Transparent High

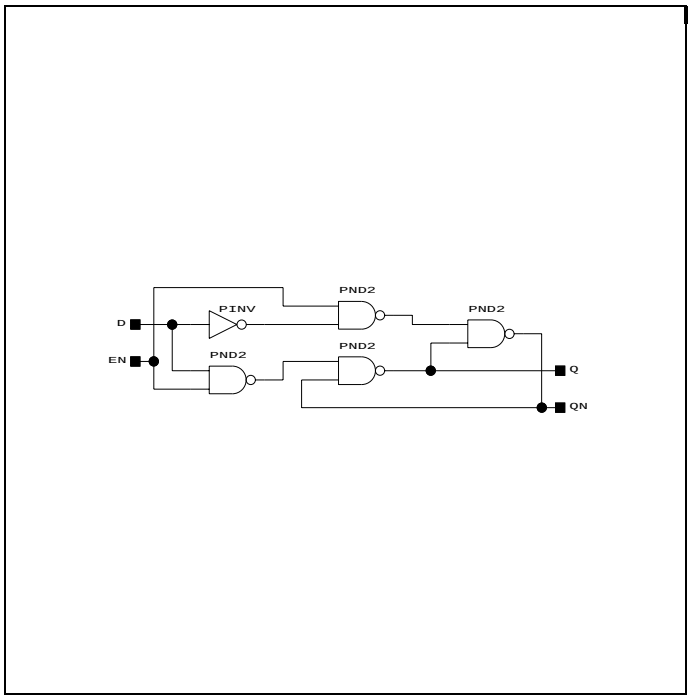
Symbol



Rectangular Area: 3x2cells

Number of Cells: 5

Schematic



Truth Table

Input		Output	
EN	D	Q	QN
0	x	q	qn
1	d	d	d'

Switching Speeds for -2ns Parts

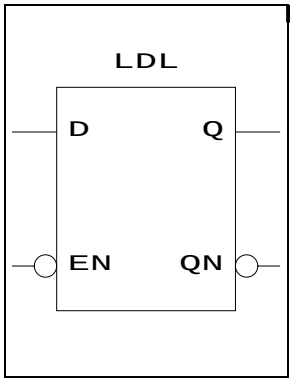
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D → Q	1.75	4.50	8.87	1.64	4.60	9.17
EN → Q	1.75	3.81	6.78	1.74	3.81	6.78
D → QN	2.52	4.60	6.97	2.41	4.50	6.78
EN → QN	1.75	3.81	6.78	1.74	3.81	6.78

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D → Q	4.33	7.45	12.77	3.74	7.46	13.67
EN → Q	4.33	6.37	9.75	4.14	6.46	10.46
D → QN	5.50	7.36	10.55	5.80	7.55	10.46
EN → QN	4.33	6.37	9.75	4.14	6.46	10.46

LDL - D Latch Transparent Low

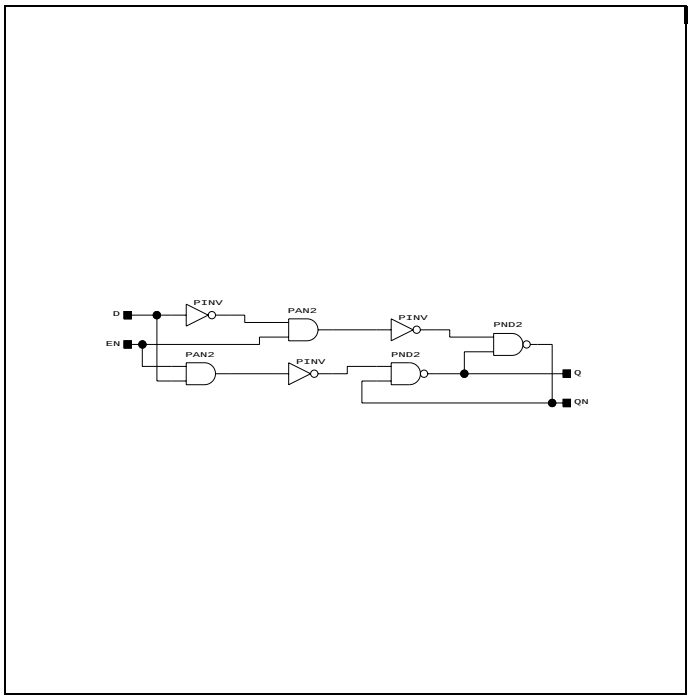
Symbol



Rectangular Area: 4x2cells

Number of Cells: 7

Schematic



Truth Table

Input		Output	
EN	D	Q	QN
1	x	q	qn
0	d	d	d'

Switching Speeds for -2ns Parts

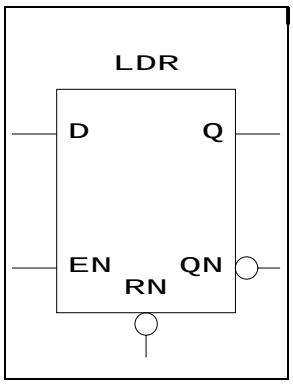
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
EN → QN	2.53	5.09	8.77	2.61	5.10	8.27
D → QN	2.99	5.33	8.07	2.88	5.33	7.98
EN → Q	2.53	5.09	8.77	2.61	5.10	8.27
D → Q	2.13	5.33	10.27	2.11	5.33	10.16

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
EN → QN	5.40	7.91	11.98	5.61	8.00	12.09
D → QN	6.66	8.30	11.29	6.76	8.49	11.39
EN → Q	5.40	7.91	11.98	5.61	8.00	12.09
D → Q	4.90	8.39	14.20	4.91	8.39	14.42

LDR - D Latch Transparent High, Reset Low

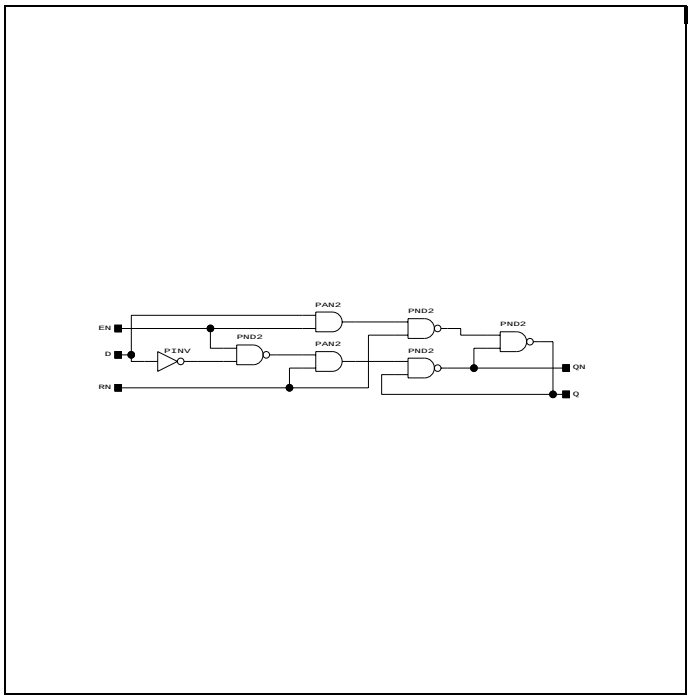
Symbol



Rectangular Area: 4x2cells

Number of Cells: 7

Schematic



Truth Table

Input			Output	
EN	D	RN	Q	QN
x	x	0	0	1
0	x	1	q	qn
1	d	1	d	d'

Switching Speeds for -2ns Parts

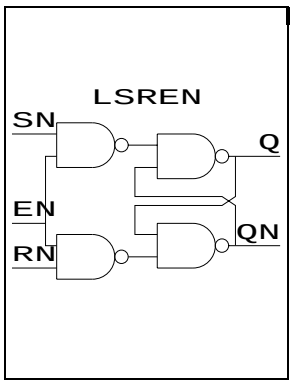
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
D → Q	2.23	5.29	10.07	2.11	5.38	10.36
EN → Q	2.23	4.60	7.98	2.21	4.59	7.97
RN → Q	1.75	3.41	5.69	1.74	3.46	5.78
D → QN	2.99	5.38	8.16	2.89	5.29	7.98
EN → QN	2.22	4.59	7.97	2.22	4.60	7.98
RN → QN	1.45	3.46	6.78	1.25	3.42	6.78

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
D → Q	5.40	8.85	14.59	4.81	8.75	15.50
EN → Q	5.40	7.76	11.57	5.21	7.75	12.29
RN → Q	4.33	5.66	7.96	4.14	5.72	8.37
D → QN	6.57	8.65	12.38	6.87	8.94	12.28
EN → QN	5.40	7.65	11.58	5.21	7.85	12.28
RN → QN	3.24	5.62	9.75	2.94	5.76	10.46

LSREN - SR Latch with NAND with Enable

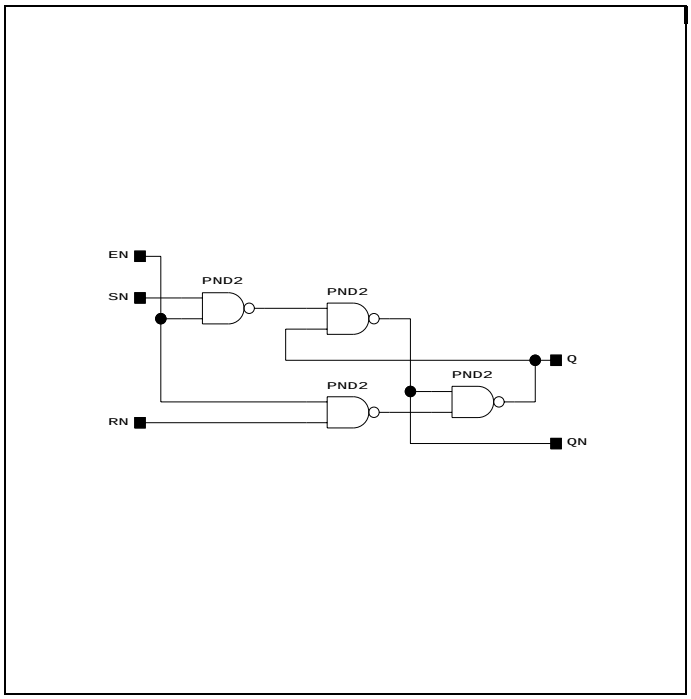
Symbol



Rectangular Area: 2x2cells

Number of Cells: 4

Schematic



Truth Table

Input			Output	
EN	SN	RN	Q	QN
0	x	x	q	qn
1	0	0	q	qn
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Switching Speeds for -2ns Parts

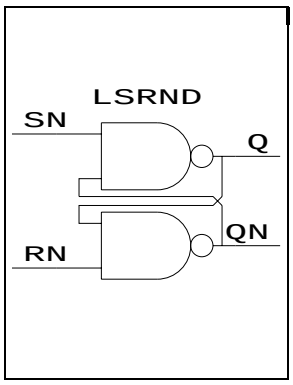
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
EN → Q	1.75	3.81	6.78	1.74	3.81	6.78
RN → Q	2.52	4.45	6.68	2.52	4.55	6.78
SN → Q	1.75	3.07	4.58	1.64	2.97	4.39
EN → QN	1.75	3.81	6.78	1.74	3.81	6.78
RN → QN	1.75	3.07	4.58	1.64	2.97	4.39
SN → QN	2.52	4.45	6.68	2.52	4.55	6.78

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
EN → Q	4.33	6.37	9.75	4.14	6.46	10.46
RN → Q	5.50	6.96	9.35	6.19	7.75	10.46
SN → Q	4.33	5.37	7.34	3.74	4.77	6.33
EN → QN	4.33	6.37	9.75	4.14	6.46	10.46
RN → QN	4.33	5.37	7.34	3.74	4.77	6.33
SN → QN	5.50	6.96	9.35	6.19	7.75	10.46

LSRND - SR Latch with NAND

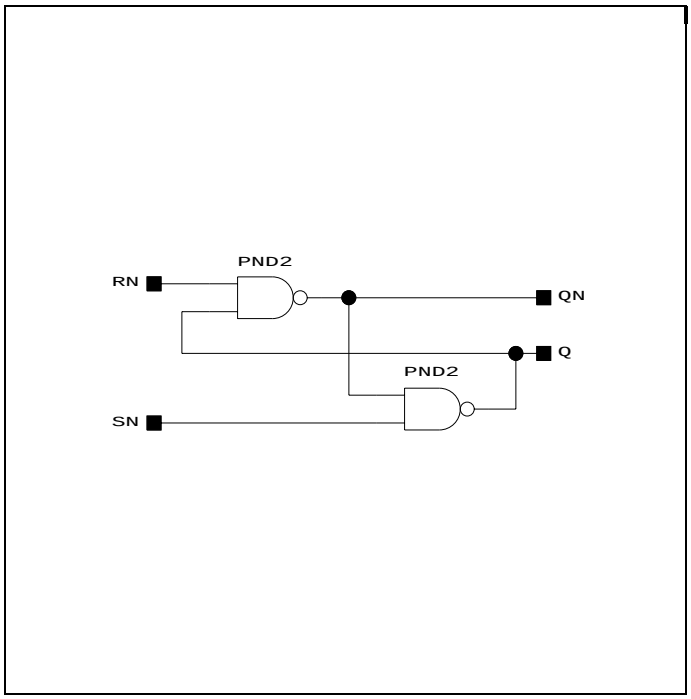
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input		Output	
SN	RN	Q	QN
0	0	1	1
0	1	1	0
1	0	0	1
1	1	q	qn

Switching Speeds for -2ns Parts

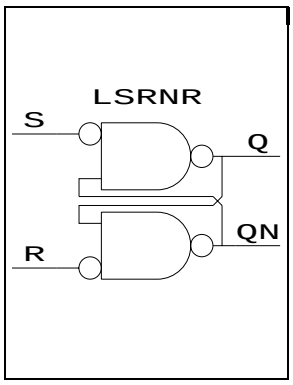
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
RN → QN	0.88	1.49	2.29	0.77	1.49	2.20
SN → QN	1.65	2.97	4.49	1.65	2.97	4.49
RN → Q	1.65	2.97	4.49	1.65	2.97	4.49
SN → Q	0.88	1.49	2.29	0.77	1.49	2.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
RN → QN	1.76	2.19	3.02	1.86	2.38	3.12
SN → QN	3.63	4.57	6.14	3.63	4.57	6.14
RN → Q	3.63	4.57	6.14	3.63	4.57	6.14
SN → Q	1.76	2.19	3.02	1.86	2.38	3.12

LSRNR - SR Latch with NOR

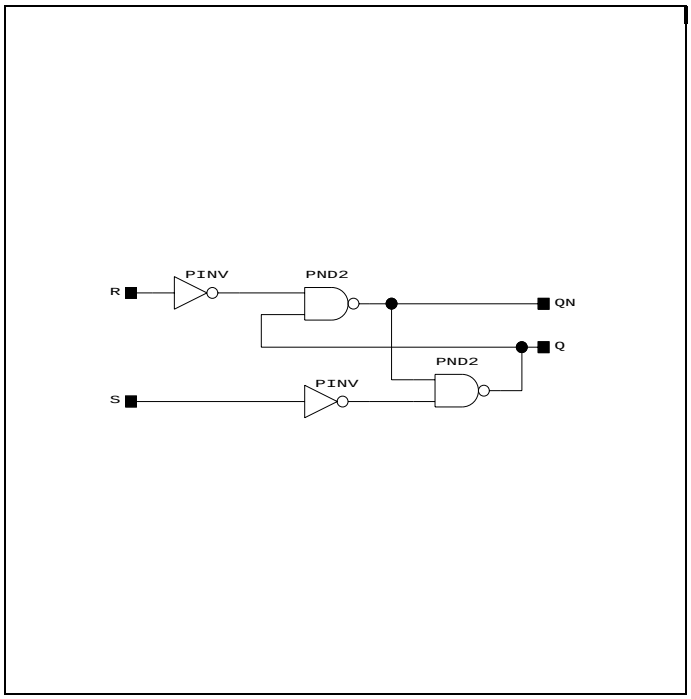
Symbol



Rectangular Area: 2x2cells

Number of Cells: 4

Schematic



Truth Table

Input		Output	
S	R	Q	QN
0	0	q	qn
0	1	0	1
1	0	1	0
1	1	0	0

Switching Speeds for -2ns Parts

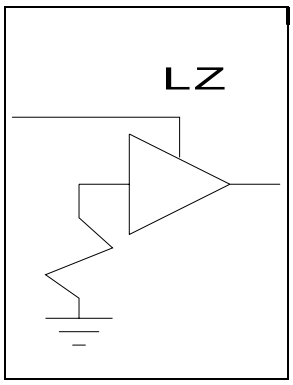
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S → Q	1.85	2.87	4.08	1.55	2.67	3.79
R → Q	2.43	4.16	6.08	2.62	4.35	6.28
S → QN	2.43	4.16	6.08	2.62	4.35	6.28
R → QN	1.85	2.87	4.08	1.55	2.67	3.79

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S → Q	3.54	4.28	5.65	3.54	4.37	5.65
R → Q	5.30	6.56	8.67	5.40	6.66	8.77
S → QN	5.30	6.56	8.67	5.40	6.66	8.77
R → QN	3.54	4.28	5.65	3.54	4.37	5.65

LZ - Bus Driver Low or Z

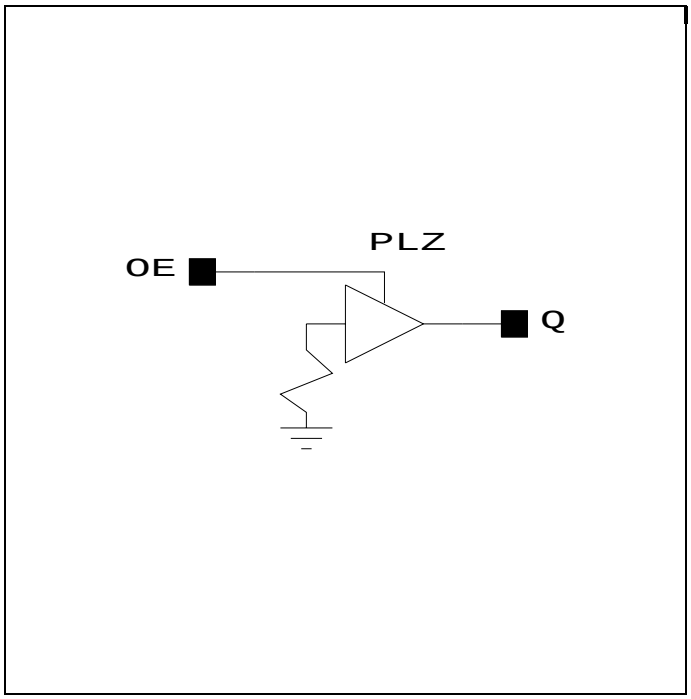
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input OE	Output Q
0	z
1	0

Switching Speeds for -2ns Parts

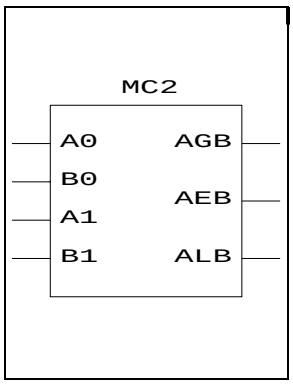
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q	0.00	0.00	0.00	0.80	1.50	2.40

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q	0.00	0.00	0.00	3.00	3.80	5.40

MC2 - 2-Bit Magnitude Comparator

Symbol



Rectangular Area: 3x7cells

Number of Cells: 20

Truth Table

Input				Output		
A1	**A0**	**B1**	**B0**	**ALB**	**AGB**	**AEB**
	a < b			1	0	0
	a > b			0	1	0
	a = b			0	0	1

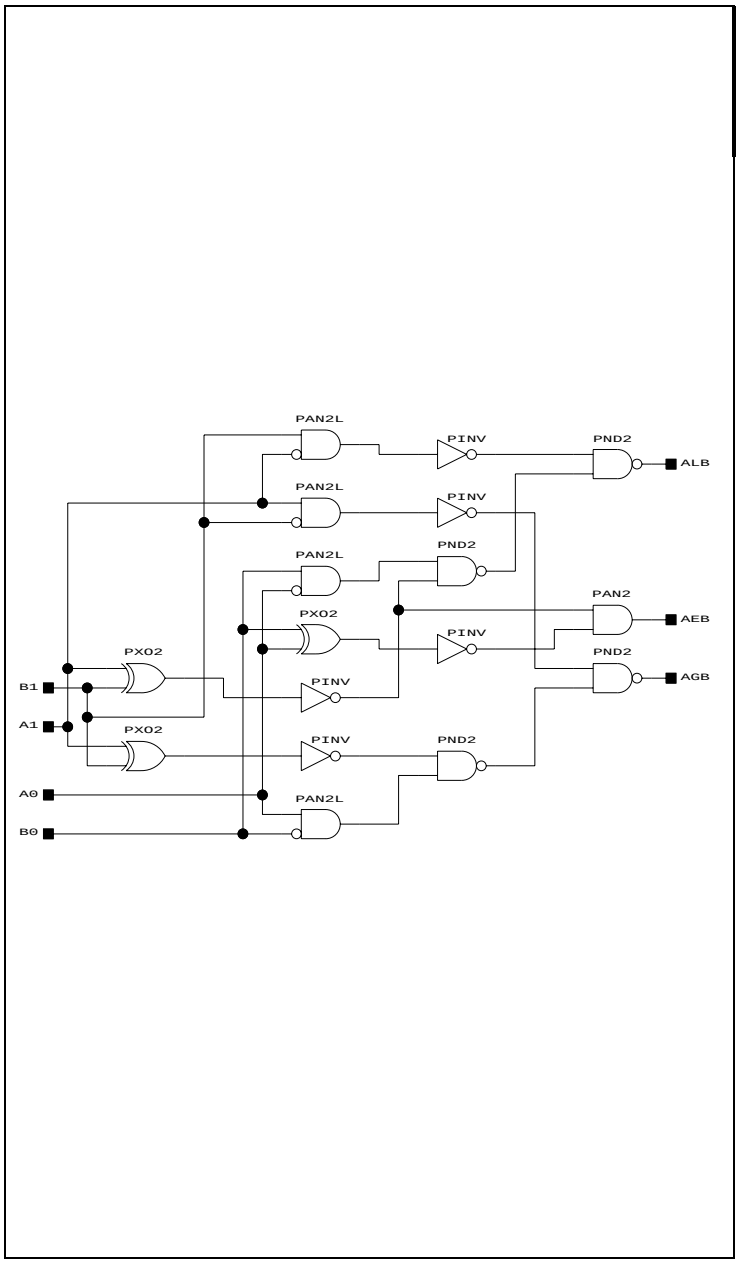
Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
B0 → AGB	2.92	4.85	7.18	3.03	5.05	7.47
A0 → AGB	2.52	4.45	6.78	2.53	4.45	6.77
B1 → AGB	2.45	5.40	10.17	2.54	5.65	10.17
A1 → AGB	2.05	5.15	10.07	2.04	5.35	10.17
B0 → AEB	2.35	4.27	6.48	2.44	4.66	6.79
A0 → AEB	2.25	4.16	6.38	2.44	4.66	6.79
B1 → AEB	2.89	5.33	7.87	2.98	5.52	8.06
A1 → AEB	2.79	5.23	7.77	2.98	5.52	8.06
B0 → ALB	2.05	3.67	5.59	2.05	3.66	5.58
A0 → ALB	2.45	4.07	5.99	2.55	4.26	6.28
B1 → ALB	2.52	5.34	9.17	2.52	5.38	9.06
A1 → ALB	2.92	5.48	9.07	3.02	5.68	9.06

Switching Speeds for -4ns Parts

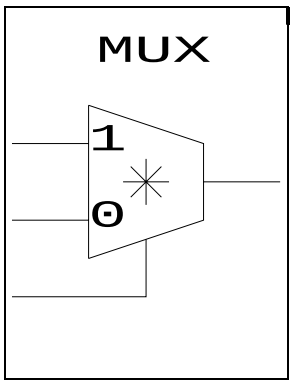
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
B0 → AGB	6.11	7.76	10.28	6.41	7.87	10.47
A0 → AGB	5.61	7.16	9.58	5.71	7.07	9.57
B1 → AGB	5.34	8.80	14.59	5.54	8.67	14.17
A1 → AGB	4.84	8.31	14.19	4.84	8.27	14.17
B0 → AEB	5.93	7.27	9.74	5.64	7.07	9.33
A0 → AEB	5.53	6.87	9.34	5.64	7.07	9.33
B1 → AEB	7.28	8.95	11.86	6.97	8.64	11.58
A1 → AEB	6.88	8.55	11.46	6.97	8.64	11.58
B0 → ALB	4.64	5.77	7.84	4.54	5.78	7.75
A0 → ALB	5.14	6.37	8.54	5.24	6.58	8.65
B1 → ALB	5.91	8.60	13.16	5.82	8.45	12.77
A1 → ALB	6.41	8.70	12.76	6.52	8.86	12.77

Schematic


PAN2L
PINV
PND2
ALB
PAN2L
PINV
PAN2L
PND2
PAN2
PX02
AEB
PINV
PX02
PND2
AGB
PINV
B1
PX02
A1
PINV
PND2
A0
PAN2L
B0

MUX - 2-to-1 Multiplexer (FAST) (A*B') XOR (A*B)

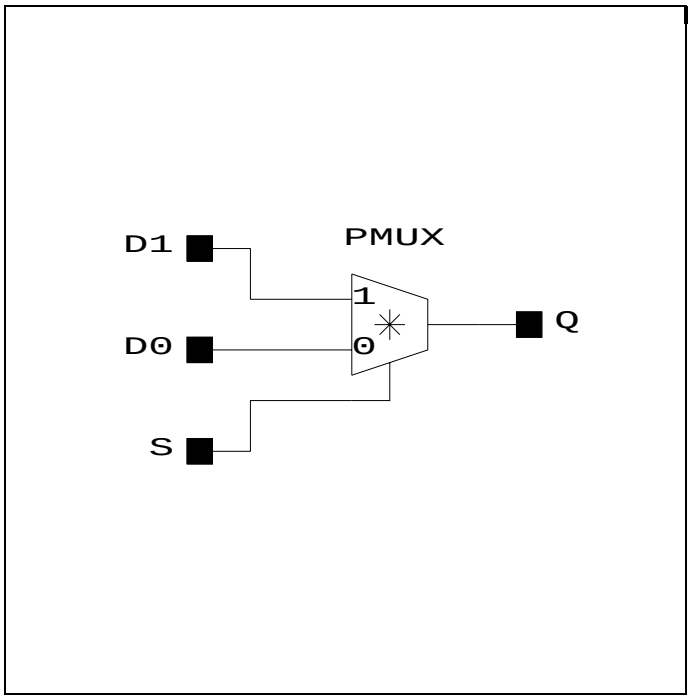
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input S	D1	D0	Output Q
0	x	0	0
0	x	1	1
1	0	x	0
1	1	x	1

Switching Speeds for -2ns Parts

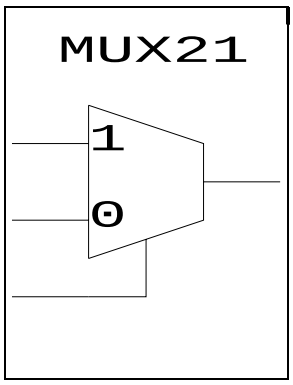
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D0 → Q	0.80	1.60	2.30	0.70	1.40	2.10
D1 → Q	0.80	1.40	2.10	0.80	1.50	2.20
S → Q	1.00	1.90	3.10	1.00	2.00	3.20

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D0 → Q	1.90	2.30	3.10	2.00	2.50	3.30
D1 → Q	1.80	2.30	3.10	2.50	3.10	4.20
S → Q	2.90	3.40	4.60	3.50	4.30	5.70

MUX21 - 2-to-1 Multiplexer

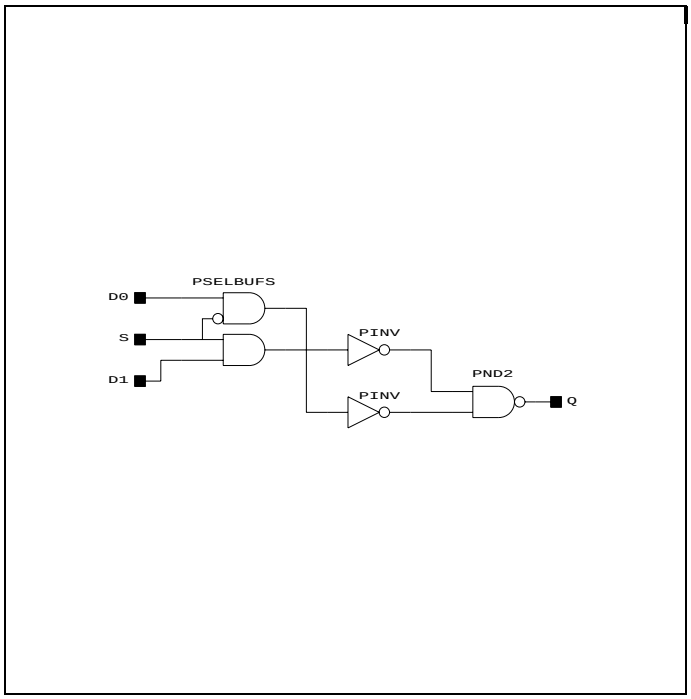
Symbol



Rectangular Area: 2x2cells

Number of Cells: 4

Schematic



Truth Table

Input S	D1	D0	Output Q
0	x	0	0
0	x	1	1
1	0	x	0
1	1	x	1

Switching Speeds for -2ns Parts

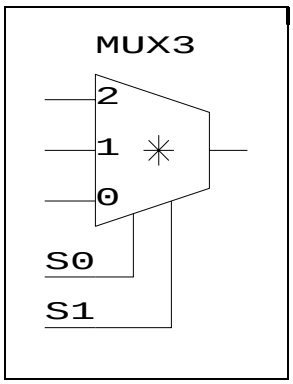
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D1 → Q	2.05	3.67	5.59	2.04	3.86	5.68
D0 → Q	2.15	3.67	5.59	2.05	3.66	5.48
S → Q	2.05	3.87	5.99	2.14	4.11	6.18

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D1 → Q	4.84	6.07	8.14	4.84	5.98	8.04
D0 → Q	4.64	5.67	7.84	4.64	5.88	7.85
S → Q	4.84	6.17	8.54	5.24	6.53	8.75

MUX3 - 3-to-1 Multiplexer (Fast)

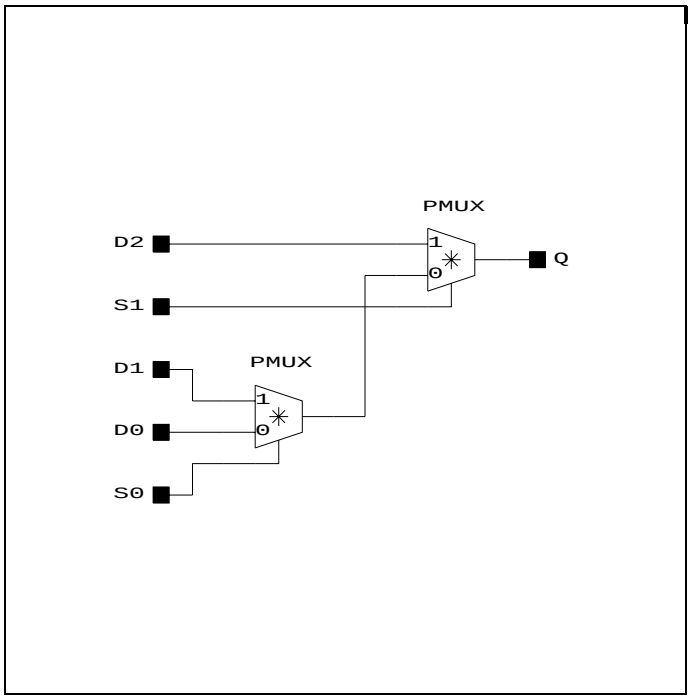
Symbol



Rectangular Area: 3x1cells

Number of Cells: 3

Schematic



Truth Table

Input					Output
S1	S0	D2	D1	D0	Q
0	0	x	x	0	0
0	0	x	x	1	1
0	1	x	0	x	0
0	1	x	1	x	1
1	0	0	x	x	0
1	0	1	x	x	1
1	1	d2	x	x	d2

Switching Speeds for -2ns Parts

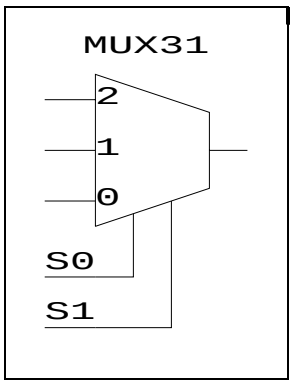
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S1 → Q	1.00	1.90	3.10	1.00	2.00	3.20
D2 → Q	0.80	1.40	2.10	0.80	1.50	2.20
D0 → Q	2.15	4.07	5.88	1.94	3.66	5.48
S0 → Q	2.35	4.36	6.68	2.24	4.26	6.58
D1 → Q	2.15	3.86	5.68	2.04	3.76	5.58

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S1 → Q	2.90	3.40	4.60	3.50	4.30	5.70
D2 → Q	1.80	2.30	3.10	2.50	3.10	4.20
D0 → Q	4.94	6.08	8.14	5.14	6.37	8.45
S0 → Q	5.94	7.18	9.64	6.64	8.17	10.85
D1 → Q	4.84	6.08	8.14	5.64	6.97	9.35

MUX31 - 3-to-1 Multiplexer

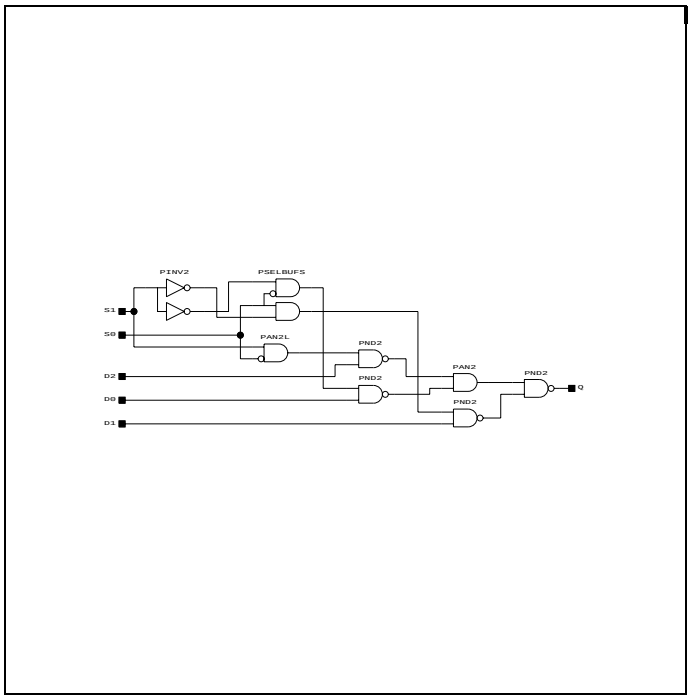
Symbol



Rectangular Area: 4x3cells

Number of Cells: 10

Schematic



Truth Table

Input					Output
S1	S0	D2	D1	D0	Q
0	0	x	x	0	0
0	0	x	x	1	1
0	1	x	0	x	0
0	1	x	1	x	1
1	0	0	x	x	0
1	0	1	x	x	1
1	1	x	x	x	0

Switching Speeds for -2ns Parts

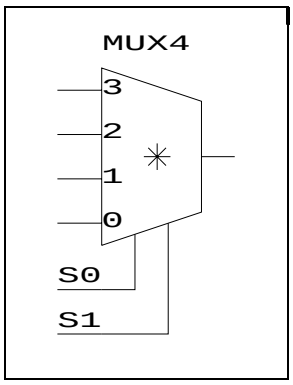
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S1 → Q	3.50	6.40	10.10	3.21	6.14	9.78
S0 → Q	2.63	5.51	9.50	2.61	5.44	9.37
D0 → Q	2.66	4.59	6.82	2.26	4.18	6.29
D1 → Q	1.67	2.98	4.49	1.67	2.98	4.39
D2 → Q	3.13	5.37	8.01	2.74	4.96	7.48

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S1 → Q	7.59	9.91	14.12	7.48	10.16	14.59
S0 → Q	6.41	9.02	13.43	6.22	8.97	13.61
D0 → Q	5.44	6.79	9.18	5.84	7.18	9.54
D1 → Q	4.26	5.28	7.22	4.07	5.09	6.61
D2 → Q	6.52	8.08	10.91	6.91	8.57	11.37

MUX4 - 4-to-1 Multiplexer (Fast)

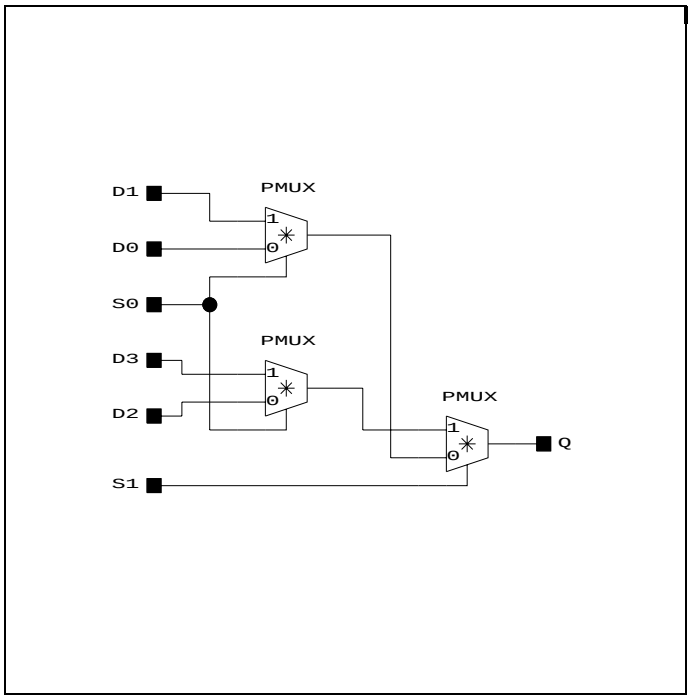
Symbol



Rectangular Area: 2x2cells

Number of Cells: 4

Schematic



Truth Table

Input						Output
S1	S0	D3	D2	D1	D0	Q
0	0	x	x	x	0	0
0	0	x	x	x	1	1
0	1	x	x	0	x	0
0	1	x	x	1	x	1
1	0	x	0	x	x	0
1	0	x	1	x	x	1
1	1	0	x	x	x	0
1	1	1	x	x	x	1

Switching Speeds for -2ns Parts

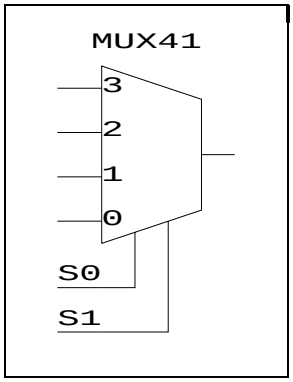
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S0 → Q	1.87	3.87	6.68	1.87	3.92	6.58
S1 → Q	1.00	1.90	3.10	1.00	2.00	3.20
D0 → Q	2.15	4.07	5.88	1.94	3.66	5.48
D3 → Q	1.67	2.88	4.29	1.67	3.08	4.49
D2 → Q	1.67	3.08	4.49	1.57	2.98	4.39
D1 → Q	2.15	3.86	5.68	2.04	3.76	5.58

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S0 -> Q	4.77	6.48	9.64	6.06	7.83	10.85
S1 -> Q	2.90	3.40	4.60	3.50	4.30	5.70
D0 -> Q	4.94	6.08	8.14	5.14	6.37	8.45
D3 -> Q	3.67	4.69	6.31	5.06	6.28	8.52
D2 -> Q	3.77	4.69	6.31	4.56	5.68	7.62
D1 -> Q	4.84	6.08	8.14	5.64	6.97	9.35

MUX41 - 4-to-1 Multiplexer

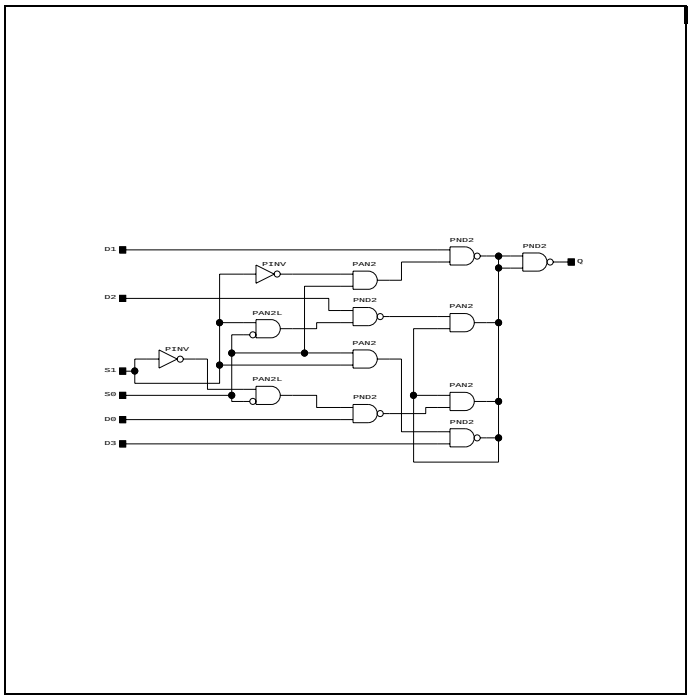
Symbol



Rectangular Area: 5x4cells

Number of Cells: 18

Schematic



Truth Table

Input						Output
S1	S0	D3	D2	D1	D0	Q
0	0	x	x	x	0	0
0	0	x	x	x	1	1
0	1	x	x	0	x	0
0	1	x	x	1	x	1
1	0	x	0	x	x	0
1	0	x	1	x	x	1
1	1	0	x	x	x	0
1	1	1	x	x	x	1

Switching Speeds for -2ns Parts

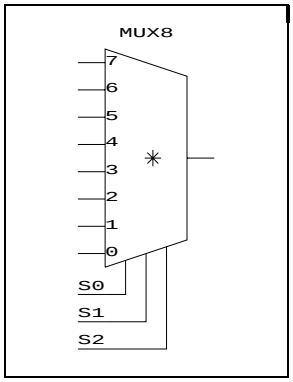
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
S0 → Q	2.83	6.90	13.01	3.04	6.84	12.66
S1 → Q	2.83	7.16	13.82	2.94	7.15	13.49
D0 → Q	3.60	6.15	9.20	3.22	5.74	8.67
D1 → Q	4.02	6.97	10.33	3.42	6.25	9.48
D2 → Q	4.39	7.75	11.52	3.90	7.03	10.77
D3 → Q	1.67	2.99	4.50	1.58	2.88	4.39

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S0 → Q	6.41	10.97	18.33	6.82	11.11	18.36
S1 → Q	6.41	11.32	19.40	6.42	11.43	19.58
D0 → Q	7.59	9.37	12.64	7.98	9.96	13.21
D1 → Q	8.40	10.49	14.06	8.68	10.76	14.39
D2 → Q	9.47	11.88	15.79	9.65	12.05	16.13
D3 → Q	3.56	4.48	6.02	3.96	4.89	6.42

MUX8 - 8-to-1 Multiplexer (Fast)

Symbol



Rectangular Area: 3x4cells

Number of Cells: 10

Truth Table

Input											Output
S2	S1	S0	D7	D6	D5	D4	D3	D2	D1	D0	Q
0	0	0	x	x	x	x	x	x	x	d0	d0
0	0	1	x	x	x	x	x	x	d1	x	d1
0	1	0	x	x	x	x	x	d2	x	x	d2
0	1	1	x	x	x	x	d3	x	x	x	d3
1	0	0	x	x	x	d4	x	x	x	x	d4
1	0	1	x	x	d5	x	x	x	x	x	d5
1	1	0	x	d6	x	x	x	x	x	x	d6
1	1	1	d7	x	x	x	x	x	x	x	d7

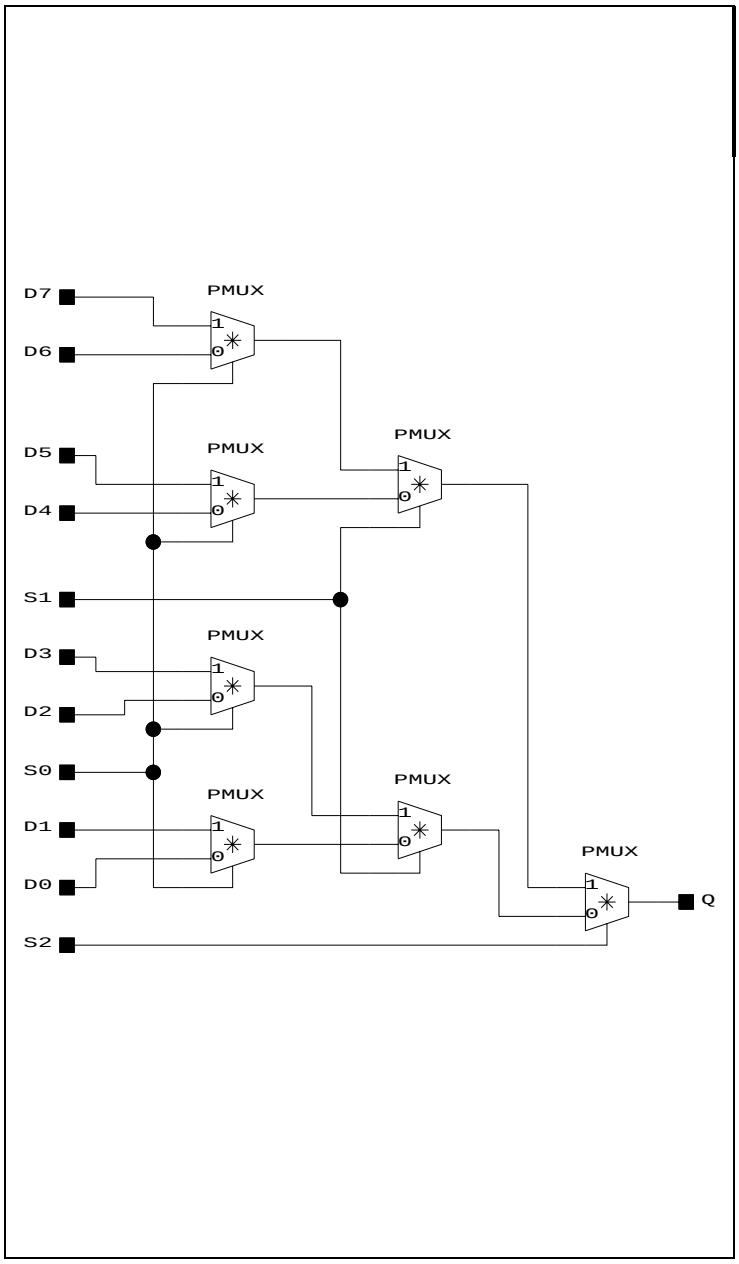
Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S2 → Q	1.00	1.90	3.10	1.00	2.00	3.20
S1 → Q	1.87	3.87	6.68	1.87	3.92	6.58
S0 → Q	2.74	5.85	10.26	2.74	5.84	9.96
D0 → Q	3.50	6.53	9.46	3.18	5.92	8.86
D1 → Q	3.50	6.33	9.26	3.28	6.02	8.96
D2 → Q	3.02	5.55	8.07	2.81	5.24	7.77
D3 → Q	3.02	5.34	7.87	2.91	5.34	7.87
D6 → Q	2.54	4.56	6.68	2.44	4.56	6.68
D7 → Q	2.54	4.36	6.48	2.54	4.66	6.78
D4 → Q	3.02	5.55	8.07	2.81	5.24	7.77
D5 → Q	3.02	5.34	7.87	2.91	5.34	7.87

Switching Speeds for -4ns Parts

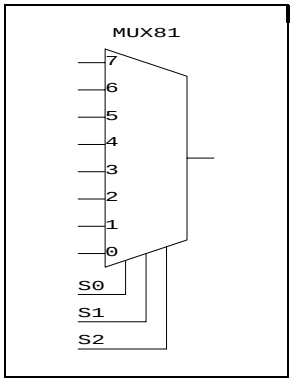
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
S2 → Q	2.90	3.40	4.60	3.50	4.30	5.70
S1 → Q	4.77	6.48	9.64	6.06	7.83	10.85
S0 → Q	6.64	9.57	14.68	8.63	11.35	16.01
D0 → Q	7.99	9.86	13.18	8.27	10.24	13.61
D1 → Q	7.89	9.86	13.18	8.77	10.84	14.51
D2 → Q	6.82	8.47	11.35	7.70	9.55	12.77
D3 → Q	6.72	8.47	11.35	8.20	10.15	13.67
D6 → Q	5.64	7.08	9.52	7.13	8.86	11.94
D7 → Q	5.54	7.08	9.52	7.63	9.46	12.84
D4 → Q	6.82	8.47	11.35	7.70	9.55	12.77
D5 → Q	6.72	8.47	11.35	8.20	10.15	13.67

Schematic



MUX81 - 8-to-1 Multiplexer

Symbol



Rectangular Area: 7x9cells

Number of Cells: 52

Truth Table

Input											Output
S2	S1	S0	D7	D6	D5	D4	D3	D2	D1	D0	Q
0	0	0	x	x	x	x	x	x	x	d0	d0
0	0	1	x	x	x	x	x	x	d1	x	d1
0	1	0	x	x	x	x	x	d2	x	x	d2
0	1	1	x	x	x	x	d3	x	x	x	d3
1	0	0	x	x	x	d4	x	x	x	x	d4
1	0	1	x	x	d5	x	x	x	x	x	d5
1	1	0	x	d6	x	x	x	x	x	x	d6
1	1	1	d7	x	x	x	x	x	x	x	d7

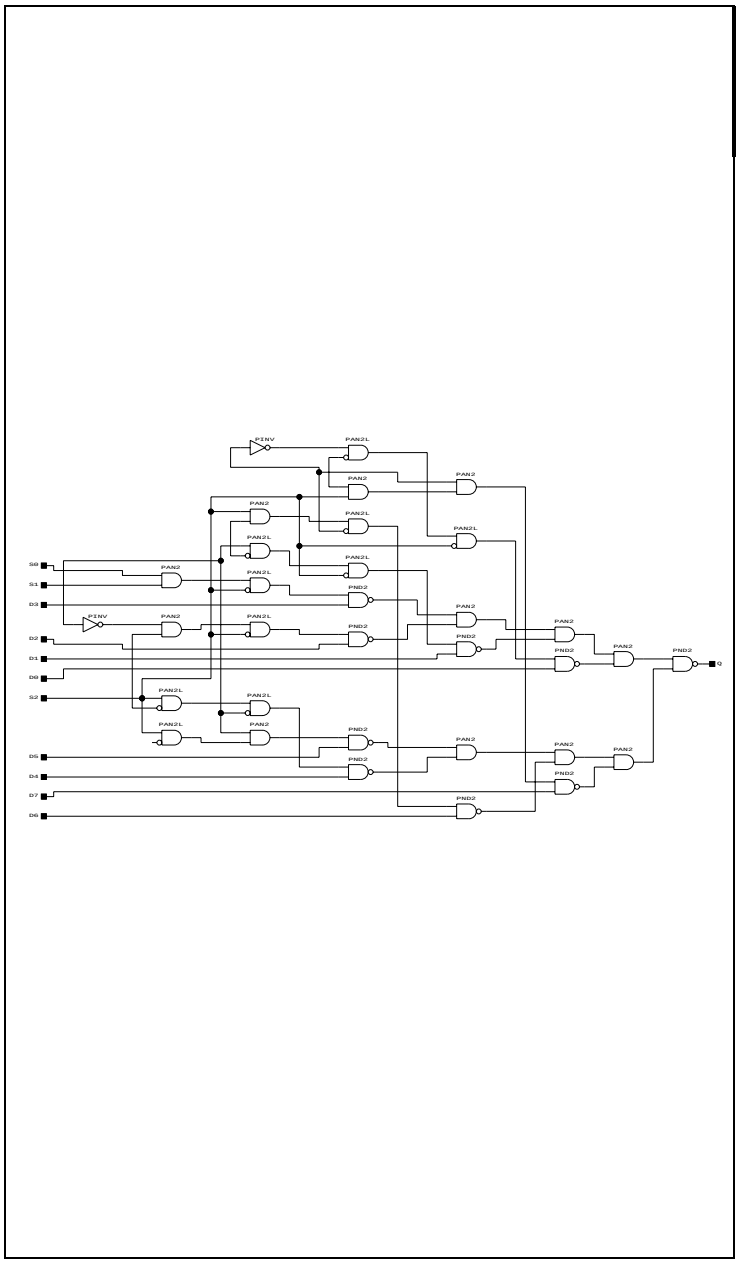
Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D0 → Q	4.44	7.71	11.58	4.18	7.31	11.15
D1 → Q	5.80	10.09	15.09	5.34	9.39	14.34
D2 → Q	7.16	12.48	18.60	6.50	11.46	17.53
D3 → Q	7.16	12.48	18.60	6.50	11.46	17.53
D4 → Q	7.63	13.26	19.79	6.98	12.26	18.74
D5 → Q	7.63	13.26	19.79	6.98	12.26	18.74
D6 → Q	6.27	10.87	16.28	5.82	10.18	15.55
D7 → Q	4.91	8.49	12.77	4.66	8.11	12.36
S1 → Q	6.18	13.14	23.68	6.09	12.72	23.01
S2 → Q	5.70	12.55	23.28	5.62	12.04	22.31
S0 → Q	5.77	13.20	24.48	5.70	12.84	23.92

Switching Speeds for -4ns Parts

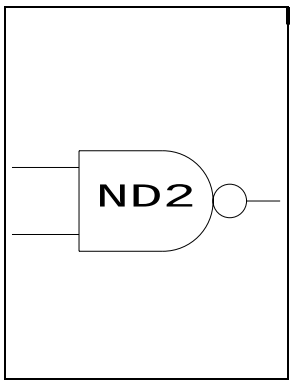
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D0 → Q	9.43	12.05	16.10	10.02	12.34	16.74
D1 → Q	12.28	15.75	20.99	12.87	15.82	21.58
D2 → Q	15.14	19.45	25.88	15.71	19.30	26.42
D3 → Q	15.04	19.45	25.88	15.71	19.20	26.41
D4 → Q	16.31	20.74	27.81	16.78	20.79	28.24
D5 → Q	16.41	20.74	27.81	16.78	20.89	28.25
D6 → Q	13.56	17.04	22.92	13.94	17.41	23.41
D7 → Q	10.70	13.34	18.04	11.10	13.93	18.57
S1 → Q	13.15	21.11	33.98	13.44	20.89	34.15
S2 → Q	12.08	20.17	33.28	12.47	19.85	33.25
S0 → Q	12.85	21.22	34.87	13.24	21.19	35.17

Schematic



ND2 - 2-Input NAND

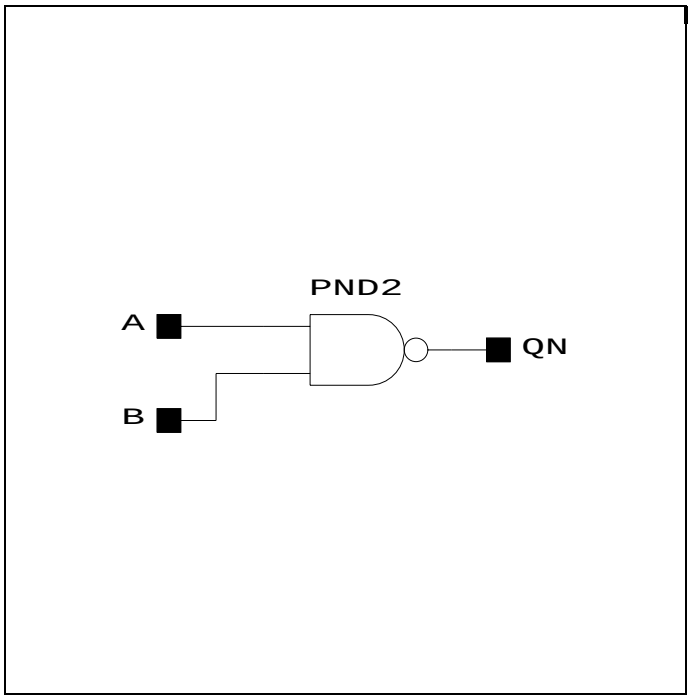
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input A	Input B	Output QN
0	0	1
0	1	1
1	0	1
1	1	0

Switching Speeds for -2ns Parts

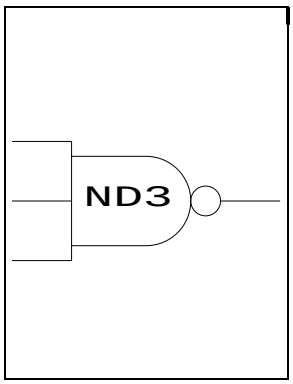
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	0.80	1.40	2.10	0.90	1.50	2.20
B → QN	0.80	1.40	2.10	0.80	1.40	2.10

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	2.20	2.60	3.40	1.80	2.20	3.00
B → QN	1.80	2.20	3.00	1.80	2.20	3.00

ND3 - 3-Input NAND

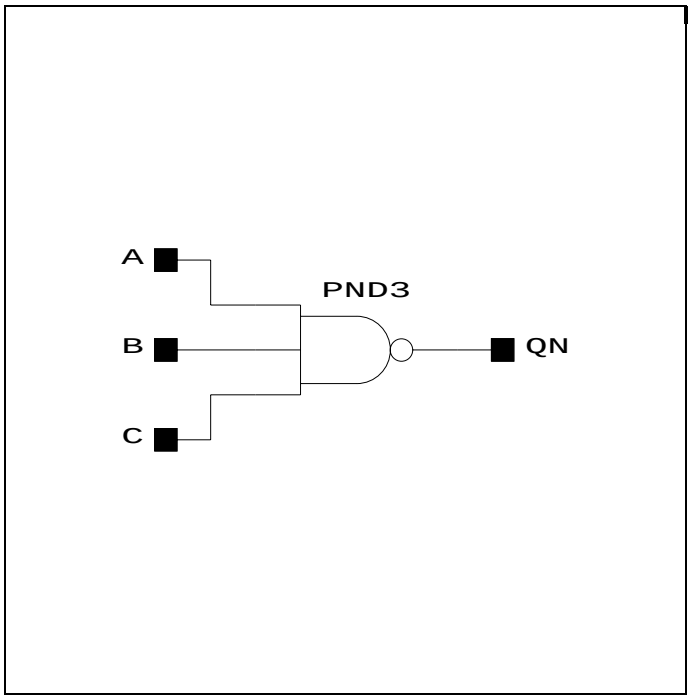
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input			Output
A	B	C	QN
0	x	x	1
x	0	x	1
x	x	0	1
1	1	1	0

Switching Speeds for -2ns Parts

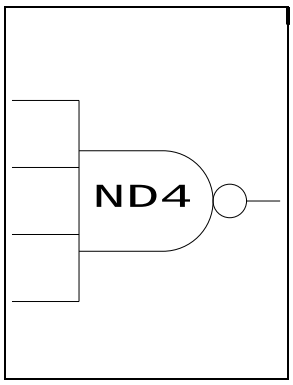
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	0.80	1.40	2.20	0.70	1.40	2.10
B → QN	0.80	1.40	2.20	0.70	1.40	2.10
C → QN	0.90	1.50	2.30	0.70	1.40	2.10

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	1.70	2.10	2.90	1.80	2.30	3.00
B → QN	1.70	2.10	2.90	1.80	2.30	3.00
C → QN	1.70	2.10	2.90	2.20	2.70	3.40

ND4 - 4-Input NAND

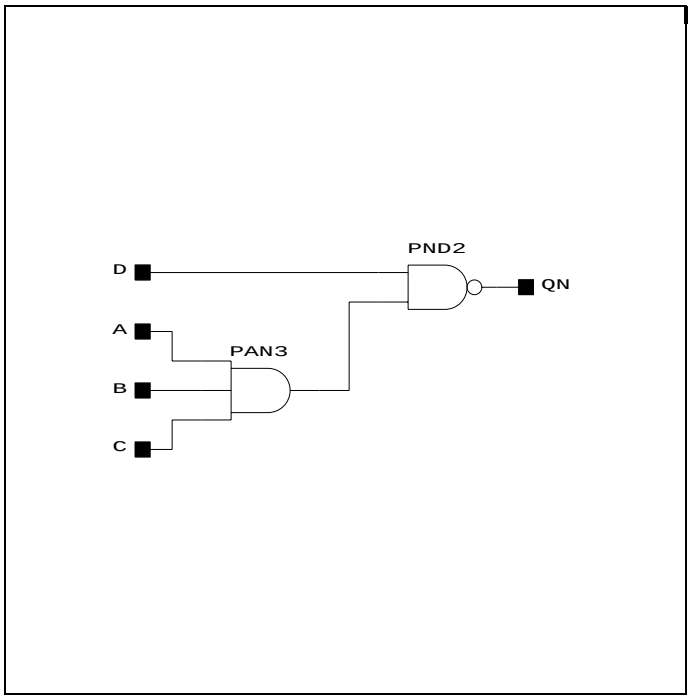
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input A	B	C	D	Output QN
0	x	x	x	1
x	0	x	x	1
x	x	0	x	1
x	x	x	0	1
1	1	1	1	0

Switching Speeds for -2ns Parts

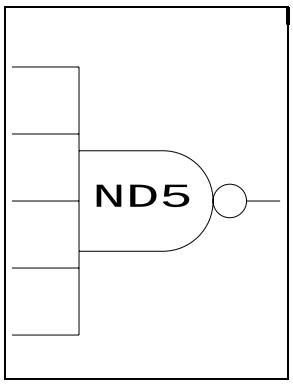
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D → QN	0.80	1.40	2.20	0.70	1.40	2.10
C → QN	1.79	3.11	4.62	1.38	2.69	4.10
B → QN	1.69	3.01	4.52	1.38	2.69	4.10
A → QN	1.69	3.01	4.52	1.38	2.69	4.10

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D → QN	1.70	2.10	2.90	1.80	2.30	3.00
C → QN	3.98	4.91	6.45	3.57	4.49	6.02
B → QN	3.58	4.51	6.05	3.57	4.49	6.02
A → QN	3.58	4.51	6.05	3.57	4.49	6.02

ND5 - 5-Input NAND

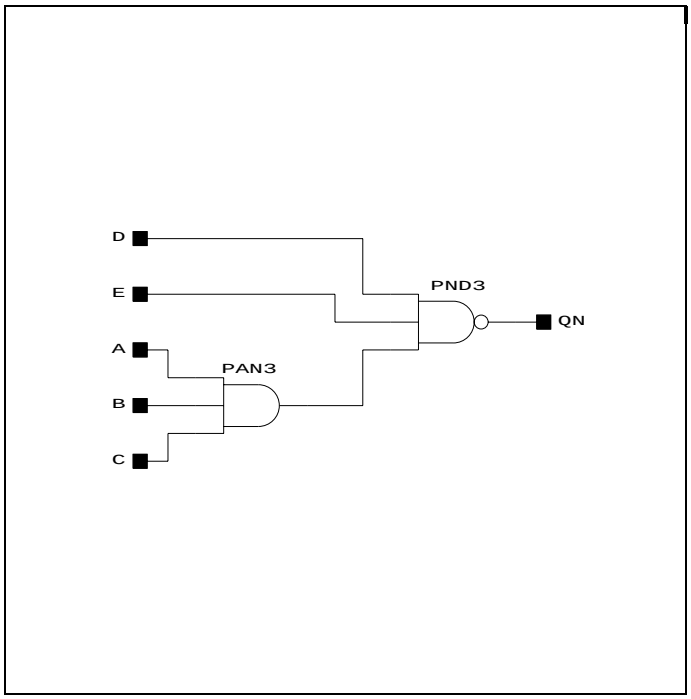
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input A	B	C	D	E	Output QN
0	x	x	x	x	1
x	0	x	x	x	1
x	x	0	x	x	1
x	x	x	0	x	1
x	x	x	x	0	1
1	1	1	1	1	0

Switching Speeds for -2ns Parts

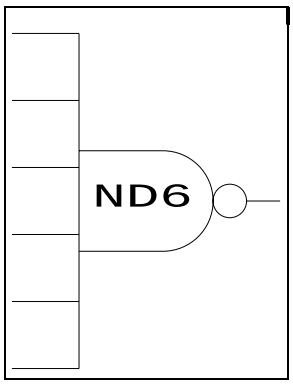
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
E → QN	0.90	1.50	2.30	0.70	1.40	2.10
D → QN	0.80	1.40	2.20	0.70	1.40	2.10
C → QN	1.79	3.11	4.62	1.38	2.69	4.10
B → QN	1.69	3.01	4.52	1.38	2.69	4.10
A → QN	1.69	3.01	4.52	1.38	2.69	4.10

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
E → QN	1.70	2.10	2.90	2.20	2.70	3.40
D → QN	1.70	2.10	2.90	1.80	2.30	3.00
C → QN	3.98	4.91	6.45	3.57	4.49	6.02
B → QN	3.58	4.51	6.05	3.57	4.49	6.02
A → QN	3.58	4.51	6.05	3.57	4.49	6.02

ND6 - 6-Input NAND

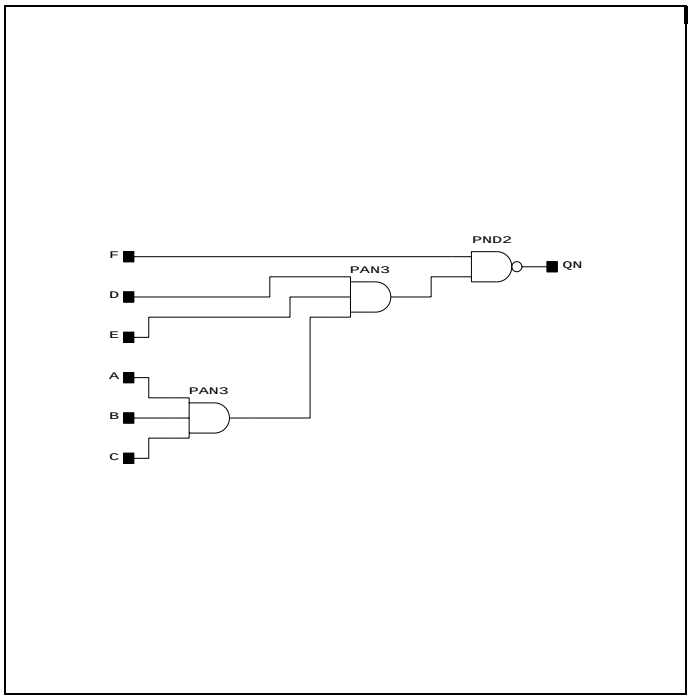
Symbol



Rectangular Area: 3x1cells

Number of Cells: 3

Schematic



Truth Table

Input						Output
A	B	C	D	E	F	QN
0	x	x	x	x	x	1
x	0	x	x	x	x	1
x	x	0	x	x	x	1
x	x	x	0	x	x	1
x	x	x	x	0	x	1
x	x	x	x	x	0	1
1	1	1	1	1	1	0

Switching Speeds for -2ns Parts

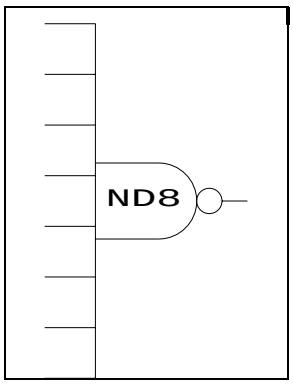
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
F → QN	0.80	1.40	2.20	0.70	1.40	2.10
E → QN	1.79	3.11	4.62	1.38	2.69	4.10
D → QN	1.69	3.01	4.52	1.38	2.69	4.10
C → QN	2.68	4.71	6.94	2.06	3.98	6.10
B → QN	2.58	4.61	6.84	2.06	3.98	6.10
A → QN	2.58	4.61	6.84	2.06	3.98	6.10

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
F → QN	1.70	2.10	2.90	1.80	2.30	3.00
E → QN	3.98	4.91	6.45	3.57	4.49	6.02
D → QN	3.58	4.51	6.05	3.57	4.49	6.02
C → QN	5.86	7.32	9.61	5.34	6.68	9.04
B → QN	5.46	6.92	9.21	5.34	6.68	9.04
A → QN	5.46	6.92	9.21	5.34	6.68	9.04

ND8 - 8-Input NAND

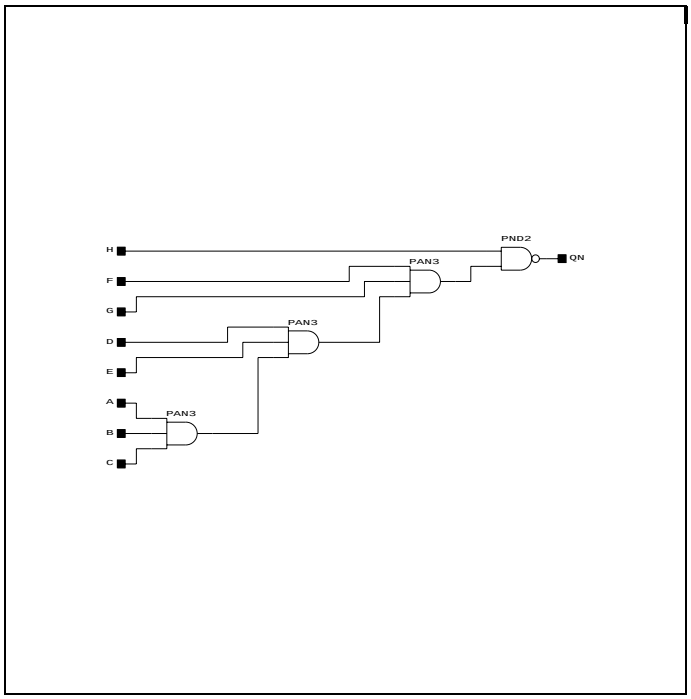
Symbol



Rectangular Area: 4x1cells

Number of Cells: 4

Schematic



Truth Table

Input								Output
A	B	C	D	E	F	G	H	QN
0	x	x	x	x	x	x	x	1
x	0	x	x	x	x	x	x	1
x	x	0	x	x	x	x	x	1
x	x	x	0	x	x	x	x	1
x	x	x	x	0	x	x	x	1
x	x	x	x	x	0	x	x	1
x	x	x	x	x	x	0	x	1
x	x	x	x	x	x	x	0	1
1	1	1	1	1	1	1	1	0

Switching Speeds for -2ns Parts

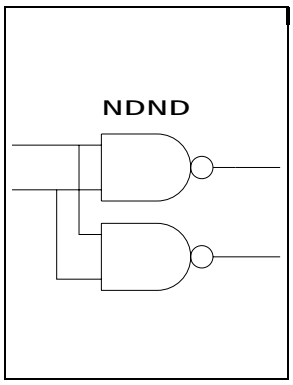
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
H → QN	0.80	1.40	2.20	0.70	1.40	2.10
G → QN	1.79	3.11	4.62	1.38	2.69	4.10
F → QN	1.69	3.01	4.52	1.38	2.69	4.10
E → QN	2.68	4.71	6.94	2.06	3.98	6.10
D → QN	2.58	4.61	6.84	2.06	3.98	6.10
C → QN	3.57	6.32	9.26	2.74	5.27	8.10
B → QN	3.47	6.22	9.16	2.74	5.27	8.10
A → QN	3.47	6.22	9.16	2.74	5.27	8.10

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
H → QN	1.70	2.10	2.90	1.80	2.30	3.00
G → QN	3.98	4.91	6.45	3.57	4.49	6.02
F → QN	3.58	4.51	6.05	3.57	4.49	6.02
E → QN	5.86	7.32	9.61	5.34	6.68	9.04
D → QN	5.46	6.92	9.21	5.34	6.68	9.04
C → QN	7.74	9.73	12.76	7.12	8.87	12.06
B → QN	7.34	9.33	12.36	7.12	8.87	12.06
A → QN	7.34	9.33	12.36	7.12	8.87	12.06

NDND - Twin 2-Input NANDs

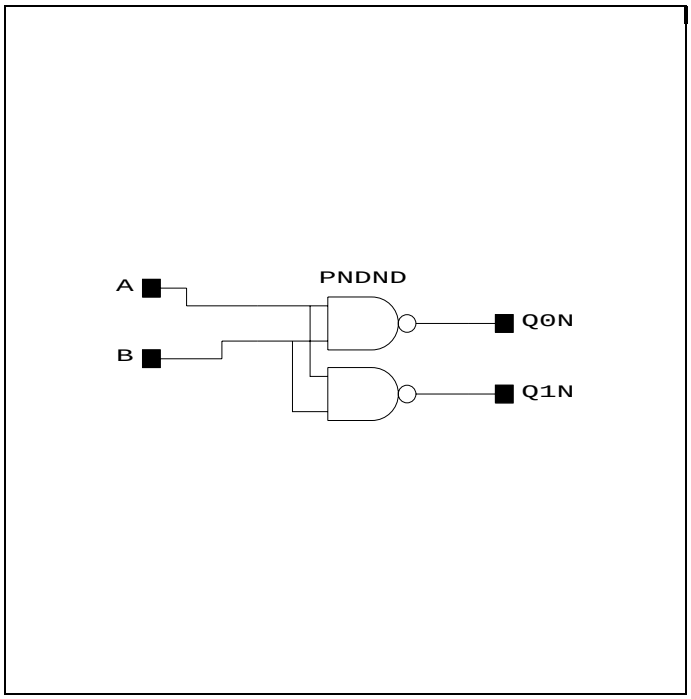
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	B	Q1N	Q0N
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	0

Switching Speeds for -2ns Parts

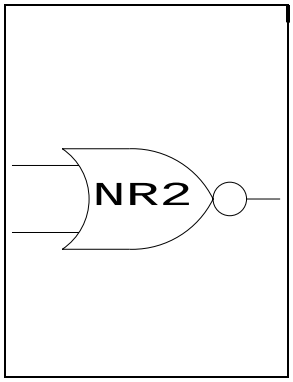
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q0N	0.90	1.50	2.20	0.80	1.50	2.20
B → Q0N	0.80	1.40	2.10	0.80	1.50	2.20
A → Q1N	0.80	1.40	2.20	0.80	1.50	2.20
B → Q1N	0.80	1.40	2.20	0.70	1.40	2.10

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q0N	2.20	2.70	3.50	2.50	3.10	4.20
B → Q0N	1.80	2.30	3.10	2.50	3.10	4.20
A → Q1N	2.10	2.50	3.30	1.80	2.30	3.00
B → Q1N	1.70	2.10	2.90	1.80	2.30	3.00

NR2 - 2-Input NOR

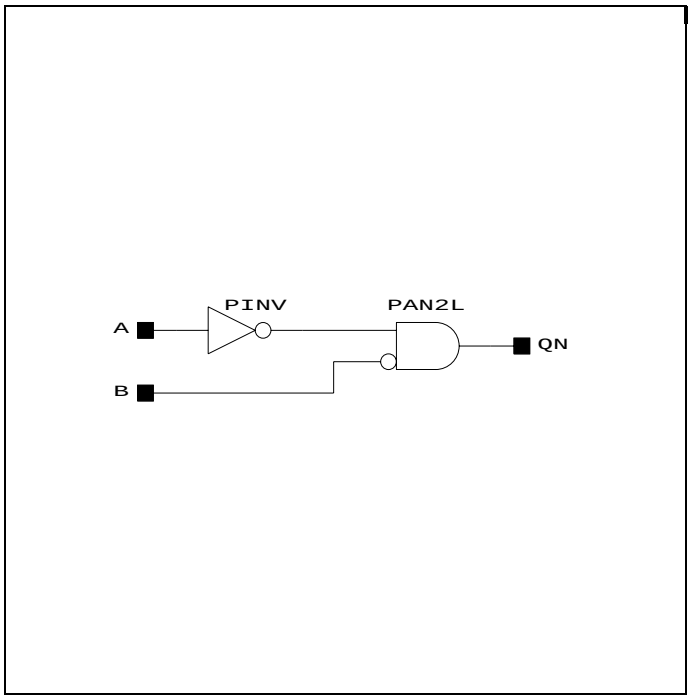
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input A	Input B	Output QN
0	0	1
0	1	0
1	0	0
1	1	0

Switching Speeds for -2ns Parts

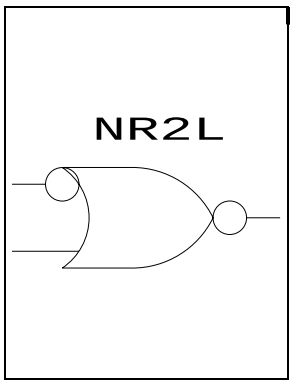
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	1.18	1.88	2.69	1.37	2.08	2.89
B → QN	0.80	1.10	1.50	0.90	1.30	1.80

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	2.57	3.09	4.12	2.67	3.29	4.13
B → QN	1.50	1.80	2.40	1.60	2.00	2.50

NR2L - 2-Input NOR with Inverted Input (A*B')

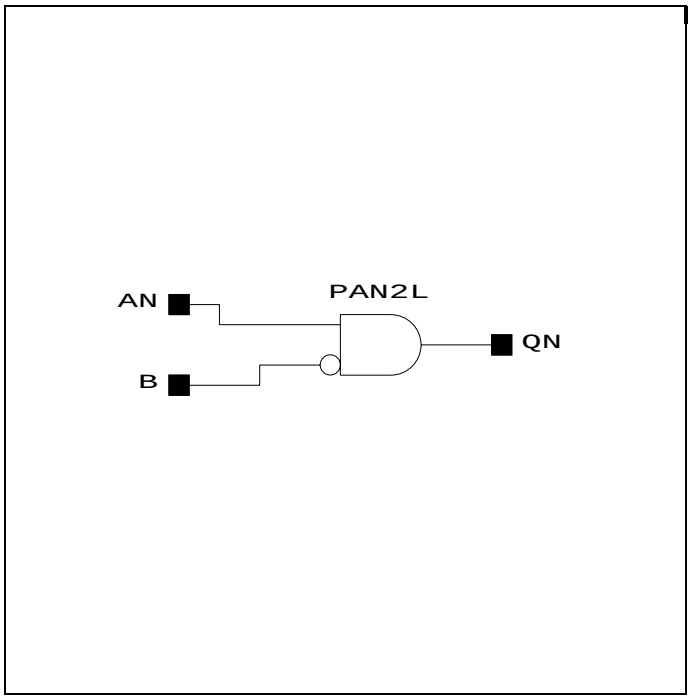
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input AN	Input B	Output QN
0	0	0
0	1	0
1	0	1
1	1	0

Switching Speeds for -2ns Parts

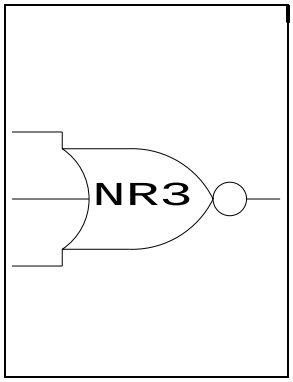
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
AN → QN	0.40	0.70	1.10	0.40	0.70	1.10
B → QN	0.80	1.10	1.50	0.90	1.30	1.80

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
AN → QN	1.00	1.20	1.70	0.90	1.20	1.60
B → QN	1.50	1.80	2.40	1.60	2.00	2.50

NR3 - 3-Input NOR

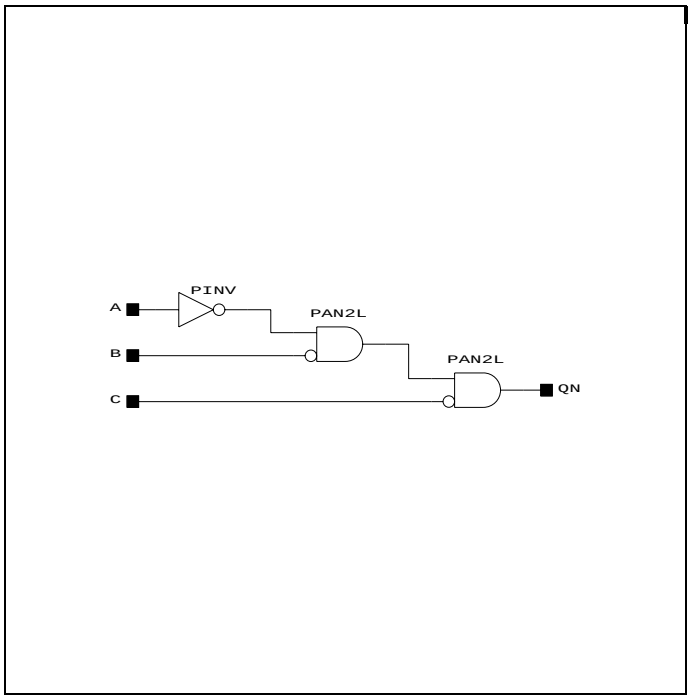
Symbol



Rectangular Area: 3x1cells

Number of Cells: 3

Schematic



Truth Table

Input A	B	C	Output QN
1	x	x	0
x	1	x	0
x	x	1	0
0	0	0	1

Switching Speeds for -2ns Parts

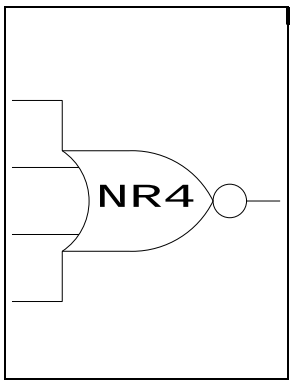
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	1.66	2.67	3.88	1.84	2.86	4.08
B → QN	1.28	1.88	2.69	1.37	2.08	2.99
C → QN	0.80	1.10	1.50	0.90	1.30	1.80

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	3.64	4.38	5.94	3.64	4.58	5.86
B → QN	2.57	3.09	4.22	2.57	3.29	4.23
C → QN	1.50	1.80	2.40	1.60	2.00	2.50

NR4 - 4-Input NOR

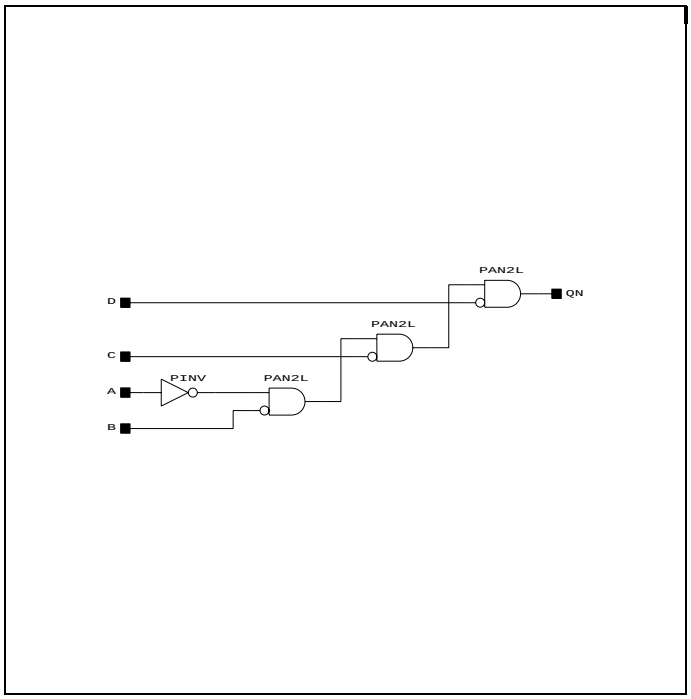
Symbol



Rectangular Area: 4x1cells

Number of Cells: 4

Schematic



Truth Table

Input A	B	C	D	Output QN
0	0	0	0	1
1	x	x	x	0
x	1	x	x	0
x	x	1	x	0
x	x	x	1	0

Switching Speeds for -2ns Parts

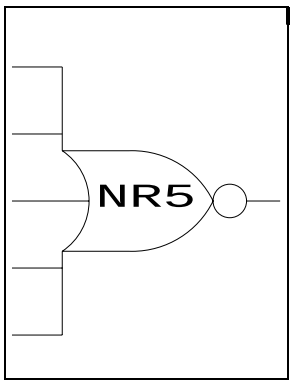
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → QN	2.14	3.46	5.07	2.31	3.64	5.27
B → QN	1.76	2.67	3.88	1.84	2.86	4.18
C → QN	1.28	1.88	2.69	1.37	2.08	2.99
D → QN	0.80	1.10	1.50	0.90	1.30	1.80

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → QN	4.72	5.67	7.76	4.62	5.87	7.60
B → QN	3.64	4.38	6.04	3.54	4.58	5.96
C → QN	2.57	3.09	4.22	2.57	3.29	4.23
D → QN	1.50	1.80	2.40	1.60	2.00	2.50

NR5 - 5-Input NOR

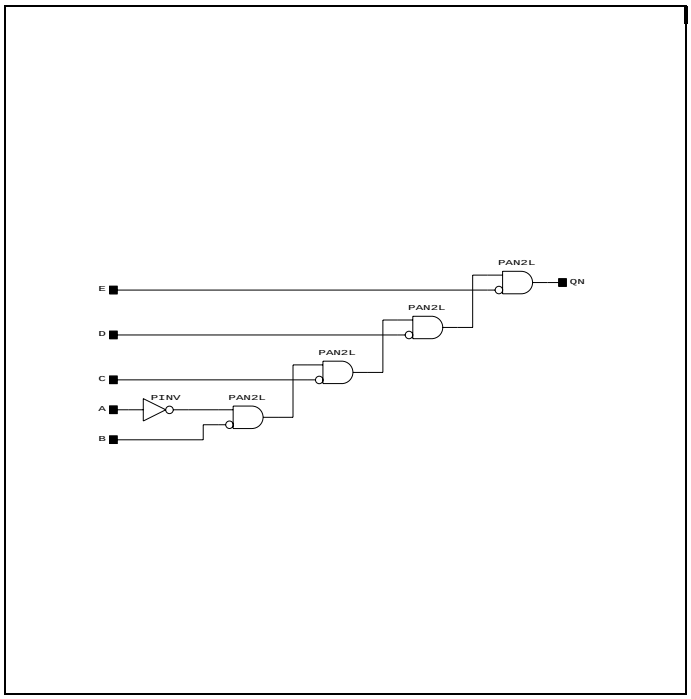
Symbol



Rectangular Area: 5x1cells

Number of Cells: 5

Schematic



Truth Table

Input A	B	C	D	E	Output QN
0	0	0	0	0	1
1	x	x	x	x	0
x	1	x	x	x	0
x	x	1	x	x	0
x	x	x	1	x	0
x	x	x	x	1	0

Switching Speeds for -2ns Parts

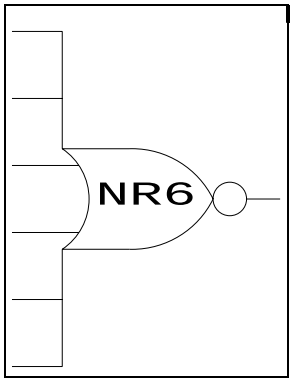
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → QN	2.62	4.24	6.26	2.78	4.42	6.46
B → QN	2.24	3.46	5.07	2.31	3.64	5.37
C → QN	1.76	2.67	3.88	1.84	2.86	4.18
D → QN	1.28	1.88	2.69	1.37	2.08	2.99
E → QN	0.80	1.10	1.50	0.90	1.30	1.80

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → QN	5.79	6.96	9.58	5.59	7.16	9.33
B → QN	4.72	5.67	7.86	4.52	5.87	7.70
C → QN	3.64	4.38	6.04	3.54	4.58	5.96
D → QN	2.57	3.09	4.22	2.57	3.29	4.23
E → QN	1.50	1.80	2.40	1.60	2.00	2.50

NR6 - 6-Input NOR

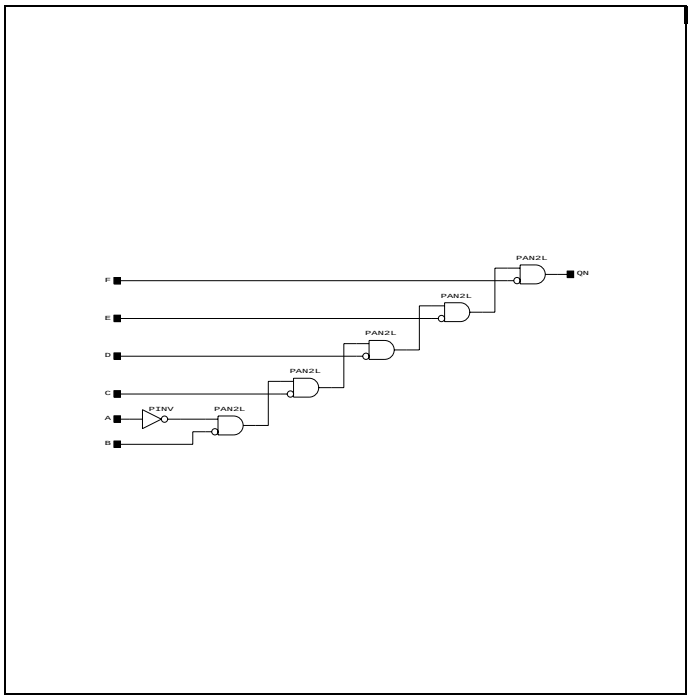
Symbol



Rectangular Area: 6x1cells

Number of Cells: 6

Schematic



Truth Table

Input A	B	C	D	E	F	Output QN
0	0	0	0	0	0	1
1	x	x	x	x	x	0
x	1	x	x	x	x	0
x	x	1	x	x	x	0
x	x	x	1	x	x	0
x	x	x	x	1	x	0
x	x	x	x	x	1	0

Switching Speeds for -2ns Parts

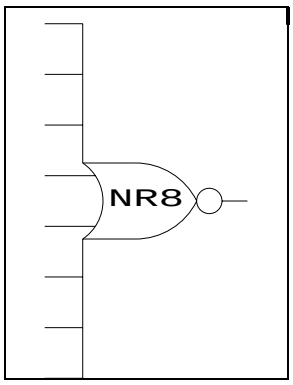
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → QN	3.10	5.02	7.45	3.25	5.20	7.65
B → QN	2.72	4.24	6.26	2.78	4.42	6.56
C → QN	2.24	3.46	5.07	2.31	3.64	5.37
D → QN	1.76	2.67	3.88	1.84	2.86	4.18
E → QN	1.28	1.88	2.69	1.37	2.08	2.99
F → QN	0.80	1.10	1.50	0.90	1.30	1.80

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → QN	6.86	8.25	11.40	6.56	8.45	11.06
B → QN	5.79	6.96	9.68	5.49	7.16	9.43
C → QN	4.72	5.67	7.86	4.52	5.87	7.70
D → QN	3.64	4.38	6.04	3.54	4.58	5.96
E → QN	2.57	3.09	4.22	2.57	3.29	4.23
F → QN	1.50	1.80	2.40	1.60	2.00	2.50

NR8 - 8-Input NOR

Symbol



Rectangular Area: 8x1cells

Number of Cells: 8

Truth Table

Input								Output
A	B	C	D	E	F	G	H	QN
0	0	0	0	0	0	0	0	1
1	x	x	x	x	x	x	x	0
x	1	x	x	x	x	x	x	0
x	x	1	x	x	x	x	x	0
x	x	x	1	x	x	x	x	0
x	x	x	x	1	x	x	x	0
x	x	x	x	x	1	x	x	0
x	x	x	x	x	x	1	x	0
x	x	x	x	x	x	x	1	0

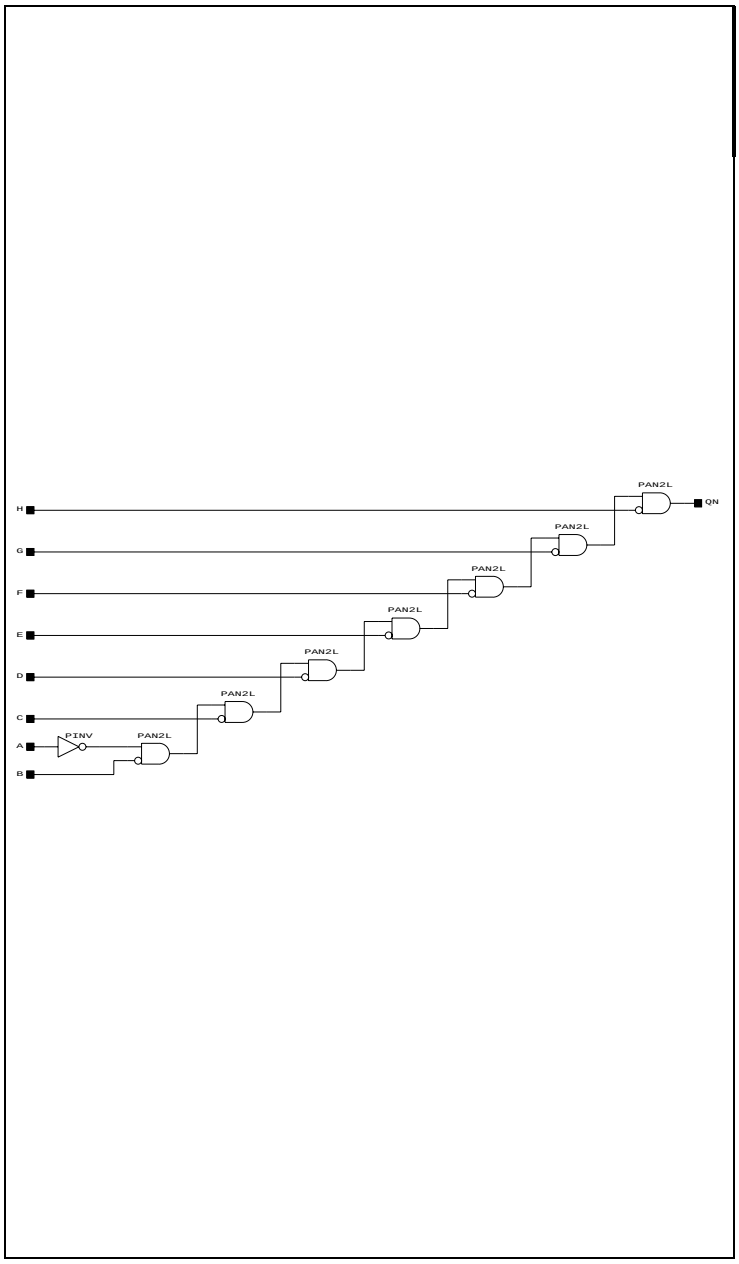
Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	4.06	6.59	9.83	4.19	6.76	10.03
B → QN	3.68	5.81	8.64	3.72	5.98	8.94
C → QN	3.20	5.02	7.45	3.25	5.20	7.75
D → QN	2.72	4.24	6.26	2.78	4.42	6.56
E → QN	2.24	3.46	5.07	2.31	3.64	5.37
F → QN	1.76	2.67	3.88	1.84	2.86	4.18
G → QN	1.28	1.88	2.69	1.37	2.08	2.99
H → QN	0.80	1.10	1.50	0.90	1.30	1.80

Switching Speeds for -4ns Parts

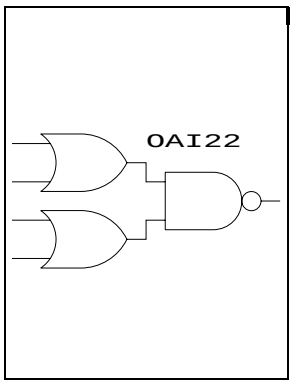
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	9.00	10.83	15.05	8.50	11.03	14.52
B → QN	7.93	9.54	13.32	7.43	9.74	12.89
C → QN	6.86	8.25	11.50	6.46	8.45	11.16
D → QN	5.79	6.96	9.68	5.49	7.16	9.43
E → QN	4.72	5.67	7.86	4.52	5.87	7.70
F → QN	3.64	4.38	6.04	3.54	4.58	5.96
G → QN	2.57	3.09	4.22	2.57	3.29	4.23
H → QN	1.50	1.80	2.40	1.60	2.00	2.50

Schematic



OAI22 - OR-AND Inverter 2-2 Inputs

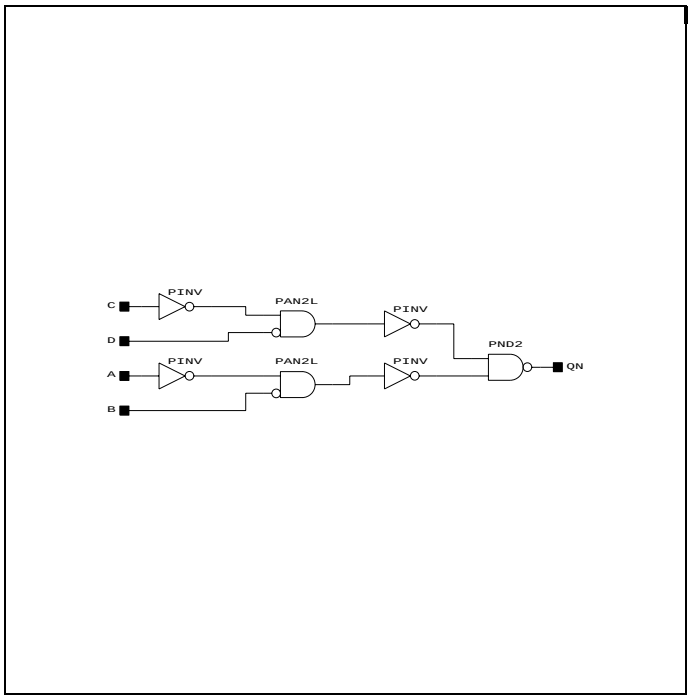
Symbol



Rectangular Area: 2x4cells

Number of Cells: 7

Schematic



Truth Table

Input A	B	C	D	Output QN
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Switching Speeds for -2ns Parts

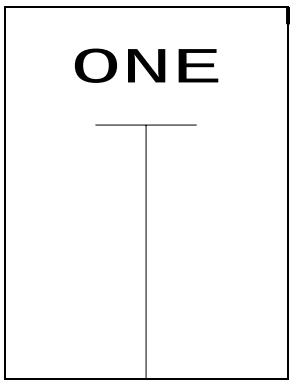
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	2.93	4.86	7.18	3.02	5.05	7.27
B → QN	2.55	4.07	5.99	2.55	4.26	6.18
C → QN	2.83	4.85	7.17	3.01	5.24	7.47
D → QN	2.45	4.07	5.98	2.54	4.46	6.38

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN	6.21	7.56	10.26	6.41	7.97	10.38
B → QN	5.14	6.27	8.54	5.34	6.68	8.75
C → QN	6.41	7.86	10.56	6.52	8.07	10.47
D → QN	5.34	6.57	8.84	5.44	6.78	8.84

ONE/ONEB - Logic One

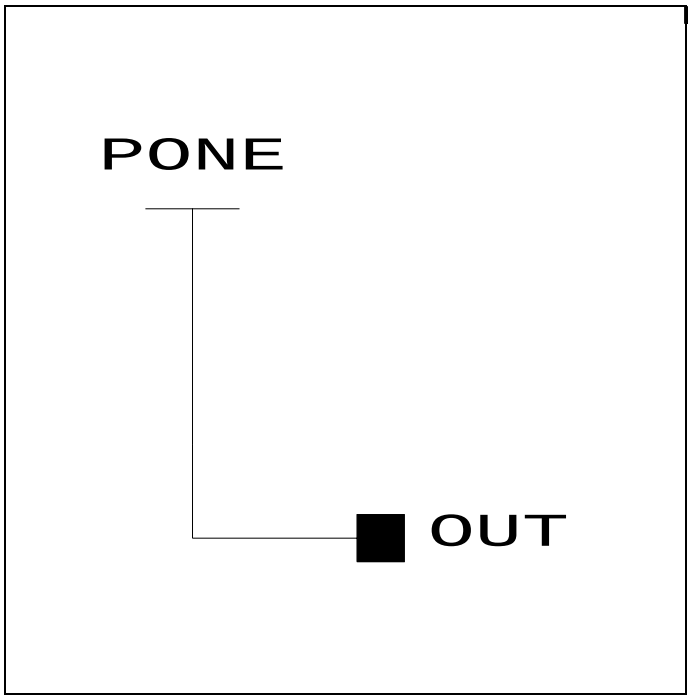
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Output OUT/OUTB
1

Switching Speeds for -2ns Parts

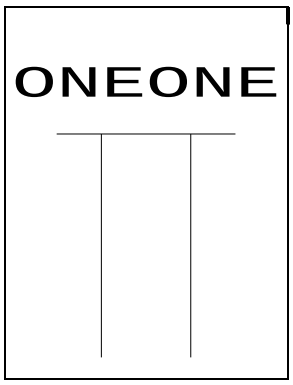
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max

ONEONE - Twin Logic Ones

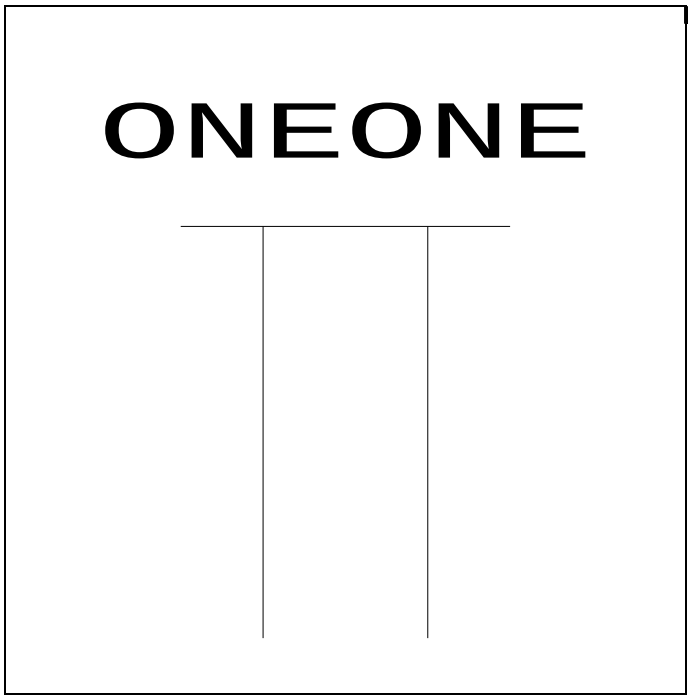
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Output	
OUT0	OUT1
1	1

Switching Speeds for -2ns Parts

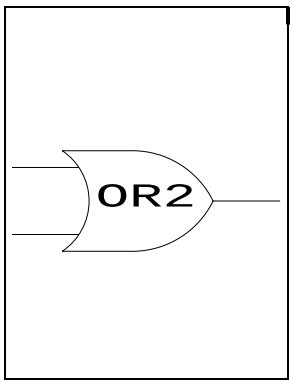
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max

OR2 - 2-Input OR

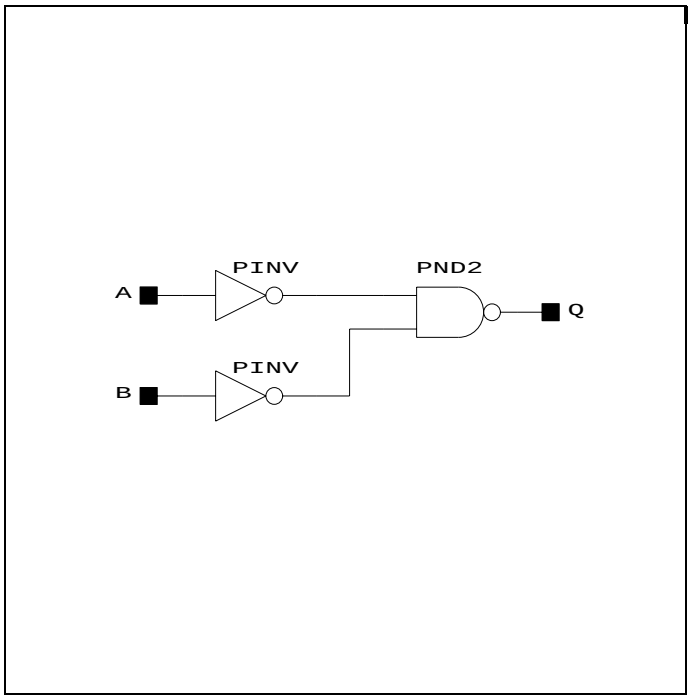
Symbol



Rectangular Area: 3x1cells

Number of Cells: 3

Schematic



Truth Table

Input A	Input BN	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

Switching Speeds for -2ns Parts

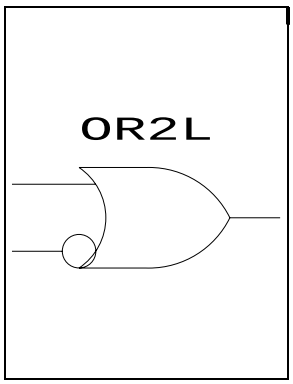
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.77	2.78	3.99	1.48	2.59	3.69
B → Q	1.77	2.78	3.99	1.48	2.59	3.69

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.47	4.19	5.53	3.47	4.29	5.53
B → Q	3.47	4.19	5.43	3.37	4.19	5.42

OR2L - 2-Input OR (A + B')

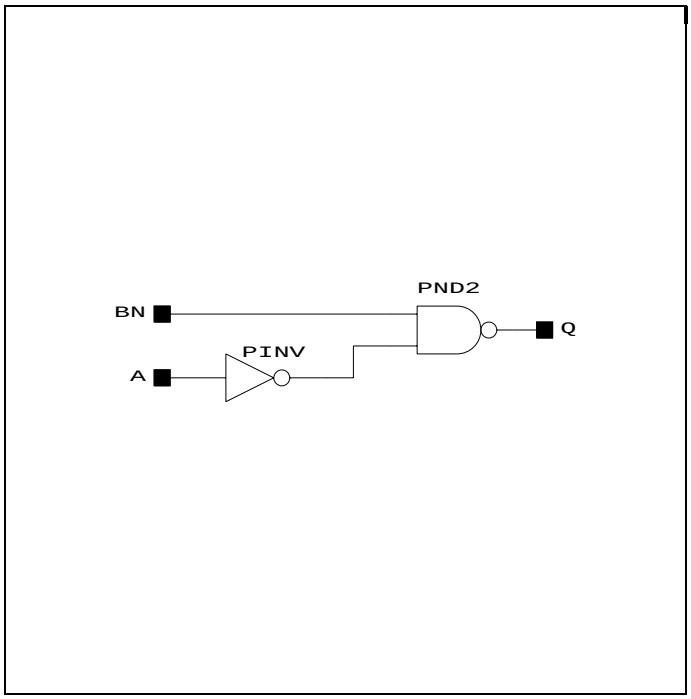
Symbol



Rectangular Area: 2x1cells

Number of Cells: 2

Schematic



Truth Table

Input A	BN	Output Q
0	0	1
0	1	0
1	0	1
1	1	1

Switching Speeds for -2ns Parts

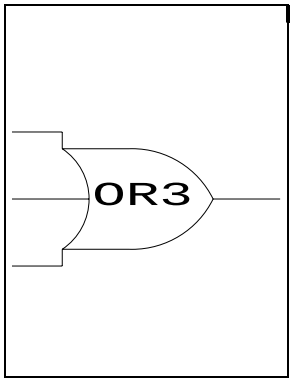
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.77	2.78	3.89	1.58	2.59	3.69
BN → Q	0.80	1.40	2.10	0.90	1.50	2.20

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.57	4.29	5.53	3.37	4.09	5.42
BN → Q	2.20	2.60	3.40	1.80	2.20	3.00

OR3 - 3-Input OR

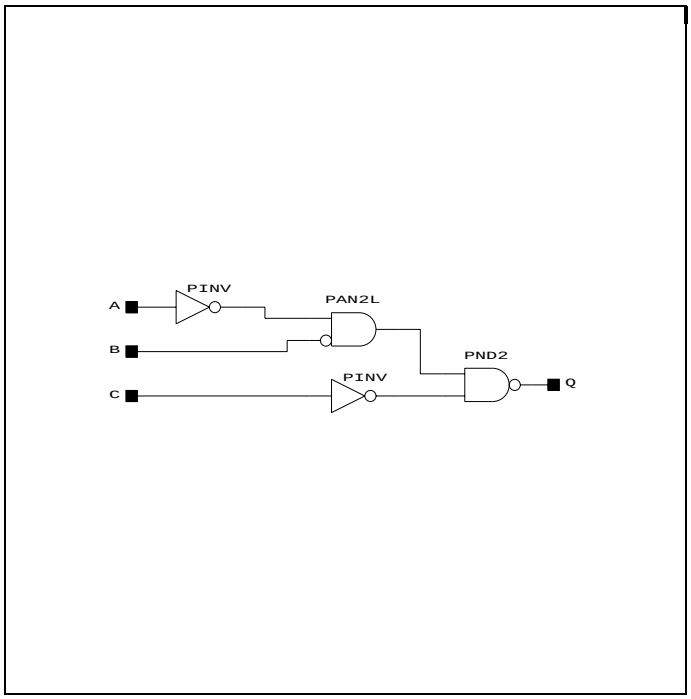
Symbol



Rectangular Area: 4x1cells

Number of Cells: 4

Schematic



Truth Table

Input		Output	
A	B	C	Q
0	0	0	0
1	x	x	1
x	1	x	1
x	x	1	1

Switching Speeds for -2ns Parts

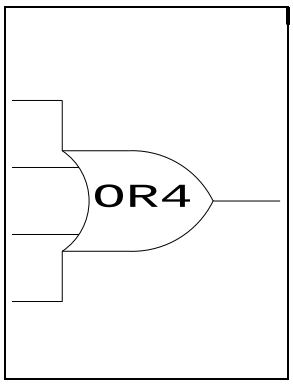
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	2.24	3.56	5.18	1.96	3.37	4.88
B → Q	1.77	2.78	4.09	1.58	2.59	3.69
C → Q	1.77	2.78	3.99	1.48	2.59	3.69

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	4.44	5.48	7.16	4.44	5.48	7.24
B → Q	3.37	4.19	5.53	3.37	4.19	5.52
C → Q	3.47	4.19	5.53	3.47	4.29	5.53

OR4 - 4-Input OR

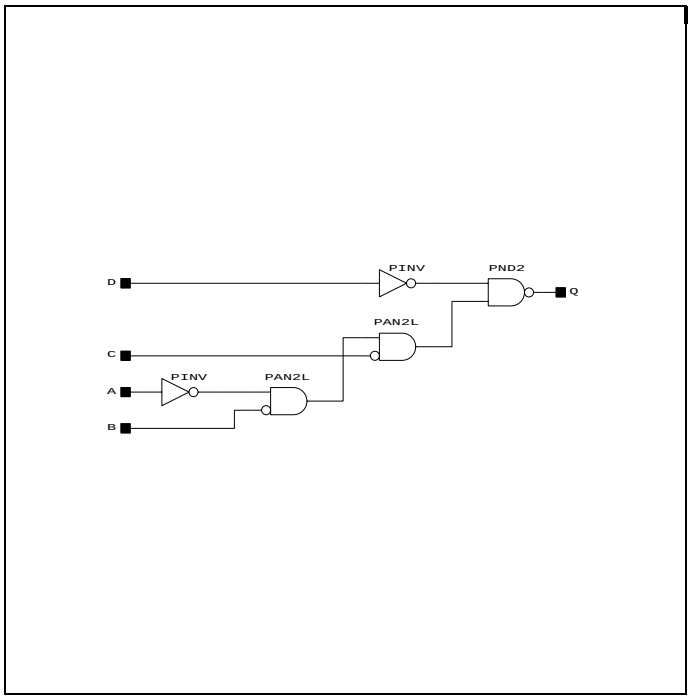
Symbol



Rectangular Area: 5x1cells

Number of Cells: 5

Schematic



Truth Table

Input A	B	C	D	Output Q
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

Switching Speeds for -2ns Parts

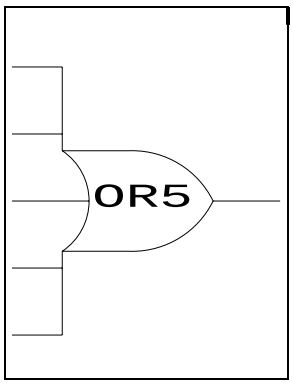
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → Q	2.71	4.34	6.37	2.44	4.16	6.07
B → Q	2.24	3.56	5.28	2.06	3.37	4.88
C → Q	1.77	2.78	4.09	1.58	2.59	3.69
D → Q	1.77	2.78	3.99	1.48	2.59	3.69

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → Q	5.42	6.77	8.90	5.52	6.77	9.06
B → Q	4.34	5.48	7.26	4.44	5.48	7.34
C → Q	3.37	4.19	5.53	3.37	4.19	5.52
D → Q	3.47	4.19	5.53	3.47	4.29	5.53

OR5 - 5-Input OR

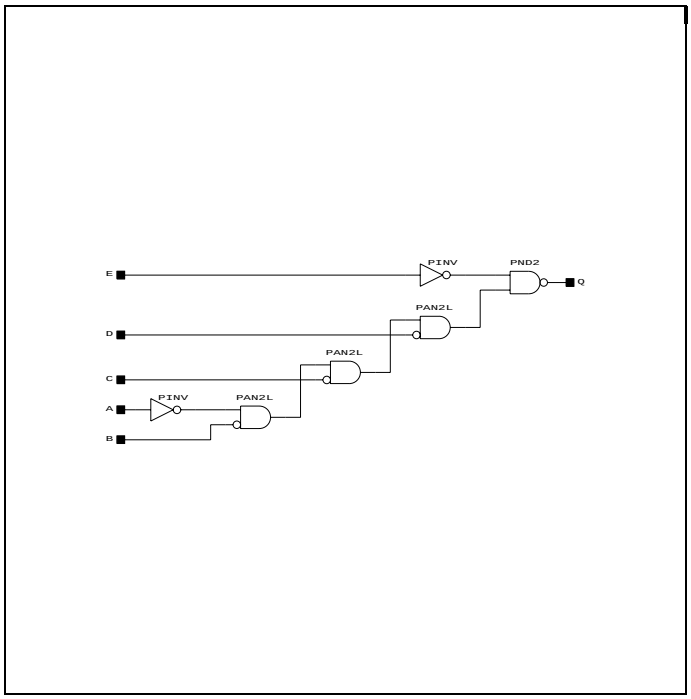
Symbol



Rectangular Area: 6x1cells

Number of Cells: 6

Schematic



Truth Table

Input A	B	C	D	E	Output Q
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Switching Speeds for -2ns Parts

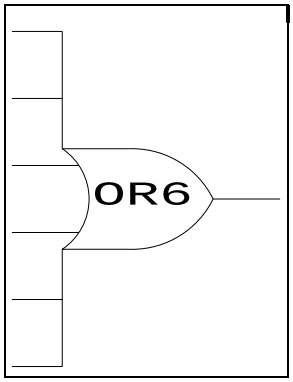
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → Q	3.18	5.12	7.56	2.92	4.94	7.26
B → Q	2.71	4.34	6.47	2.54	4.16	6.07
C → Q	2.24	3.56	5.28	2.06	3.37	4.88
D → Q	1.77	2.78	4.09	1.58	2.59	3.69
E → Q	1.77	2.78	3.99	1.48	2.59	3.69

Switching Speeds for -4ns Parts

Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
A → Q	6.39	8.06	10.63	6.59	8.06	10.88
B → Q	5.32	6.77	9.00	5.52	6.77	9.16
C → Q	4.34	5.48	7.26	4.44	5.48	7.34
D → Q	3.37	4.19	5.53	3.37	4.19	5.52
E → Q	3.47	4.19	5.53	3.47	4.29	5.53

OR6 - 6-Input OR

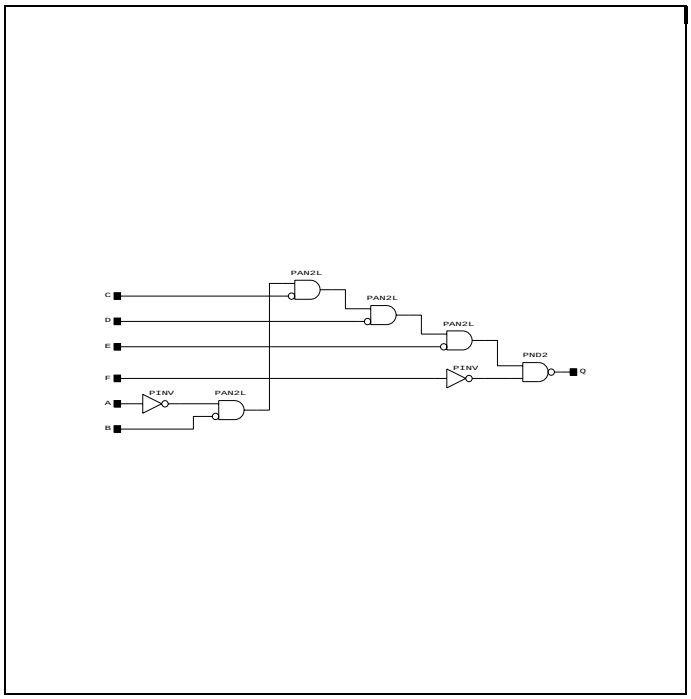
Symbol



Rectangular Area: 7x1cells

Number of Cells: 7

Schematic



Truth Table

Input						Output
A	B	C	D	E	F	Q
0	0	0	0	0	0	0
1	x	x	x	x	x	1
x	1	x	x	x	x	1
x	x	1	x	x	x	1
x	x	x	1	x	x	1
x	x	x	x	1	x	1
x	x	x	x	x	1	1

Switching Speeds for -2ns Parts

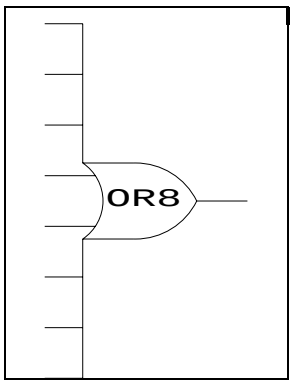
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	3.65	5.90	8.75	3.40	5.72	8.45
B → Q	3.18	5.12	7.66	3.02	4.94	7.26
C → Q	2.71	4.34	6.47	2.54	4.16	6.07
D → Q	2.24	3.56	5.28	2.06	3.37	4.88
E → Q	1.77	2.78	4.09	1.58	2.59	3.69
F → Q	1.77	2.78	3.99	1.48	2.59	3.69

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	7.36	9.35	12.36	7.66	9.35	12.70
B → Q	6.29	8.06	10.73	6.59	8.06	10.98
C → Q	5.32	6.77	9.00	5.52	6.77	9.16
D → Q	4.34	5.48	7.26	4.44	5.48	7.34
E → Q	3.37	4.19	5.53	3.37	4.19	5.52
F → Q	3.47	4.19	5.53	3.47	4.29	5.53

OR8 - 8-Input OR

Symbol



Rectangular Area: 9x1cells

Number of Cells: 9

Truth Table

Input								Output
A	B	C	D	E	F	G	H	Q
0	0	0	0	0	0	0	0	0
1	x	x	x	x	x	x	x	1
x	1	x	x	x	x	x	x	1
x	x	1	x	x	x	x	x	1
x	x	x	1	x	x	x	x	1
x	x	x	x	1	x	x	x	1
x	x	x	x	x	1	x	x	1
x	x	x	x	x	x	1	x	1
x	x	x	x	x	x	x	1	1

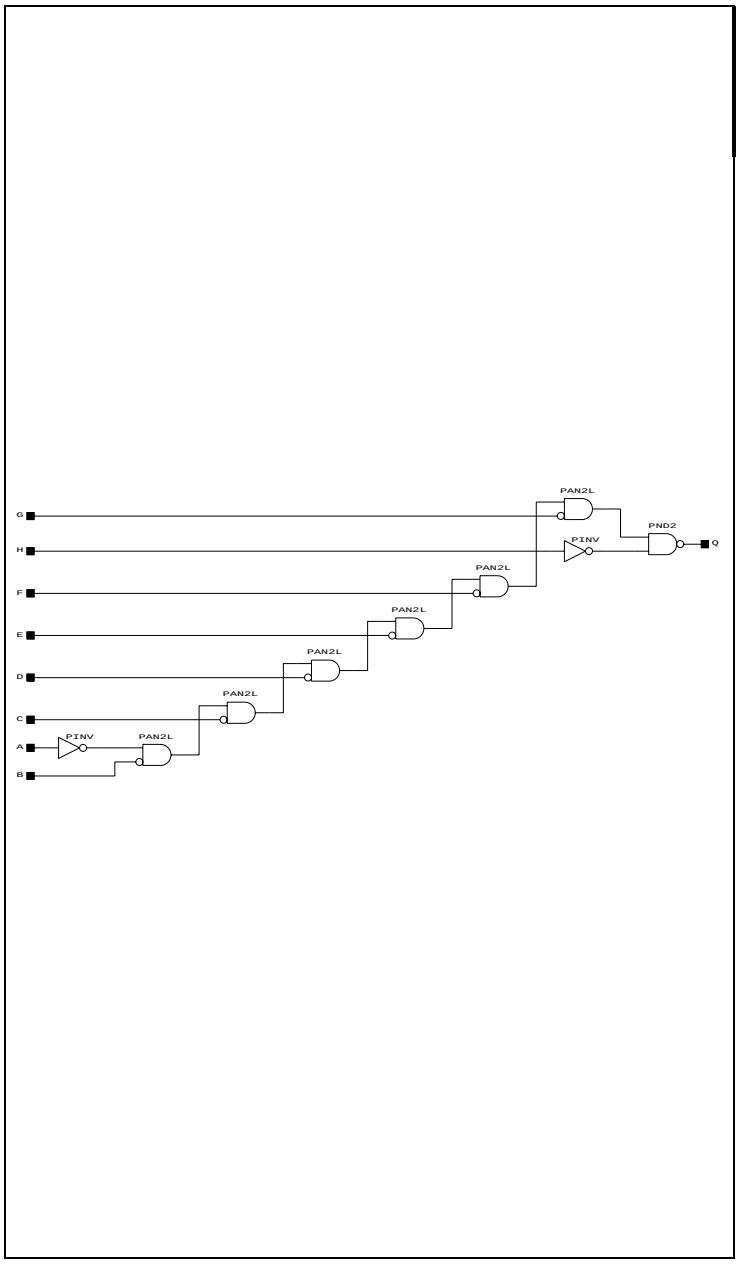
Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	4.59	7.46	11.13	4.36	7.29	10.83
B → Q	4.12	6.68	10.04	3.98	6.51	9.64
C → Q	3.65	5.90	8.85	3.50	5.72	8.45
D → Q	3.18	5.12	7.66	3.02	4.94	7.26
E → Q	2.71	4.34	6.47	2.54	4.16	6.07
F → Q	2.24	3.56	5.28	2.06	3.37	4.88
G → Q	1.77	2.78	4.09	1.58	2.59	3.69
H → Q	1.77	2.78	3.99	1.48	2.59	3.69

Switching Speeds for -4ns Parts

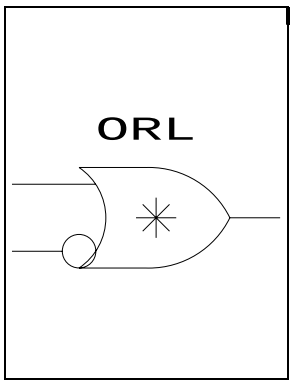
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	9.30	11.93	15.82	9.80	11.93	16.35
B → Q	8.23	10.64	14.19	8.73	10.64	14.62
C → Q	7.26	9.35	12.46	7.66	9.35	12.80
D → Q	6.29	8.06	10.73	6.59	8.06	10.98
E → Q	5.32	6.77	9.00	5.52	6.77	9.16
F → Q	4.34	5.48	7.26	4.44	5.48	7.34
G → Q	3.37	4.19	5.53	3.37	4.19	5.52
H → Q	3.47	4.19	5.53	3.47	4.29	5.53

Schematic


PAN2L
G
PND2
H
PINV
Q
PAN2L
F
PAN2L
E
PAN2L
D
PAN2L
C
PINV
PAN2L
A
B

ORL - 2-Input OR (AN*B) XOR AN'

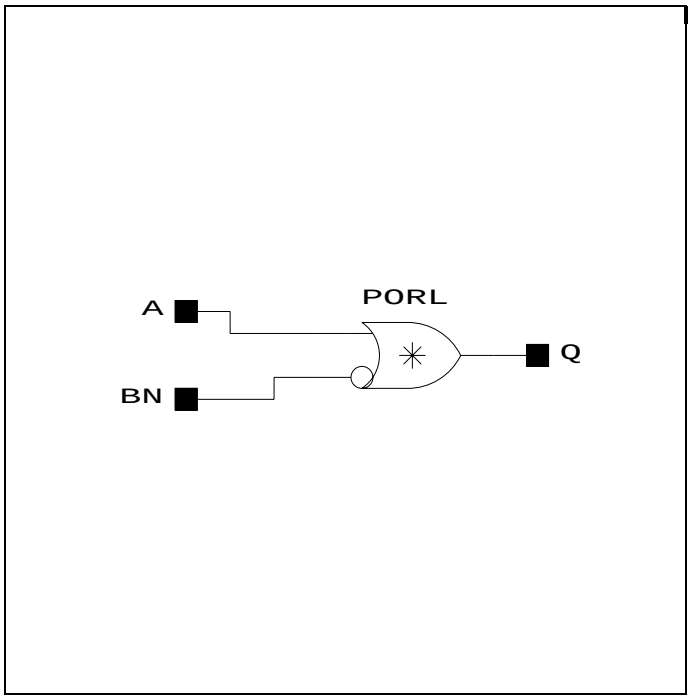
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input A	BN	Output Q
0	0	1
0	1	0
1	0	1
1	1	1

Switching Speeds for -2ns Parts

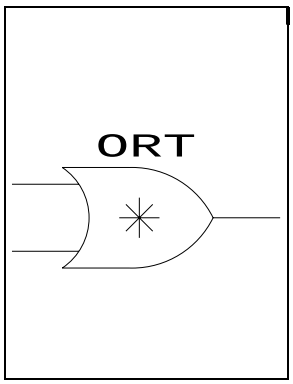
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	0.80	1.40	2.10	0.80	1.50	2.20
BN → Q	0.80	1.40	2.10	0.90	1.60	2.30

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.80	2.30	3.10	2.50	3.10	4.20
BN → Q	1.80	2.30	3.10	2.90	3.50	4.60

ORT - 2-Input OR = (A*B') XOR B

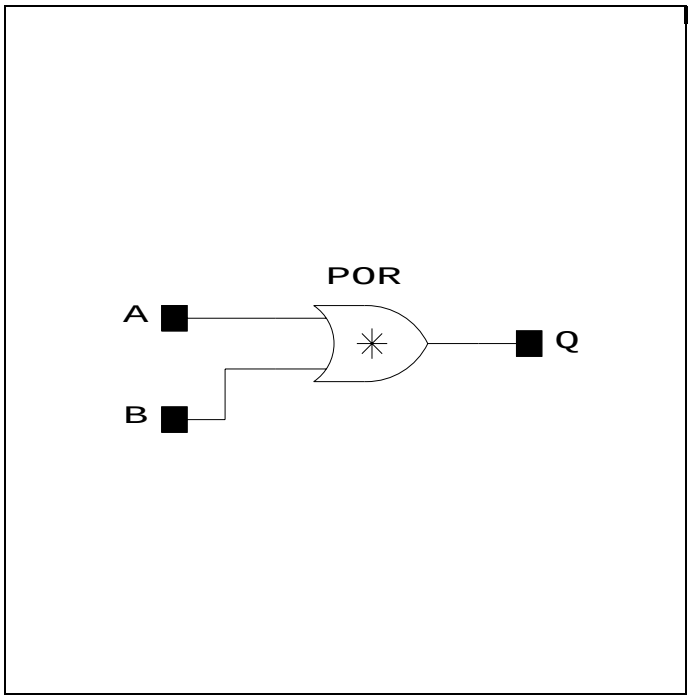
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	1

Switching Speeds for -2ns Parts

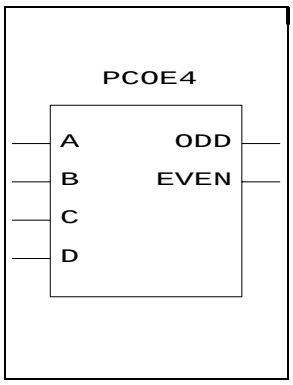
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	0.80	1.40	2.10	0.80	1.50	2.20
B → Q	0.80	1.40	2.10	0.90	1.60	2.30

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.80	2.30	3.10	2.50	3.10	4.20
B → Q	1.80	2.30	3.10	2.90	3.50	4.60

PCOE4 - 4-Bit Parity Checker Odd/Even

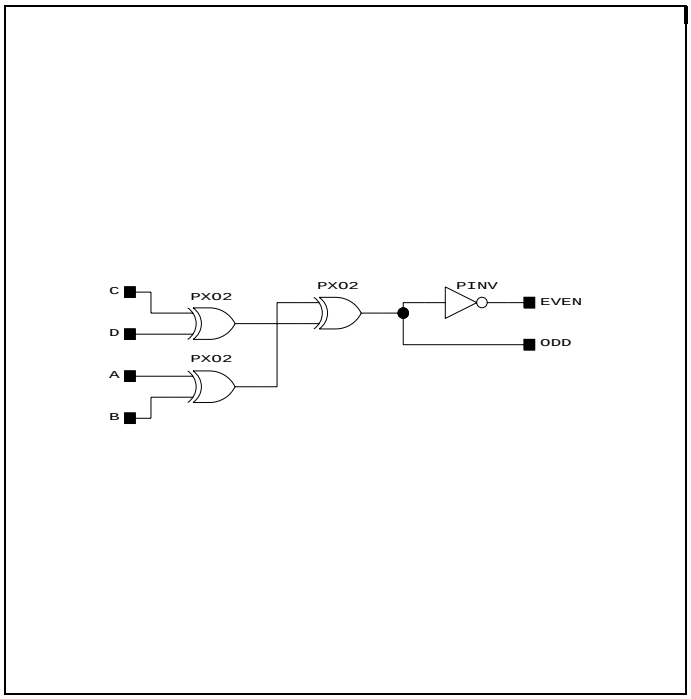
Symbol



Rectangular Area: 3x2cells

Number of Cells: 5

Schematic



Truth Table

Input A	B	C	D	Output EVEN	ODD
	even parity			1	0
	odd parity			0	1

Switching Speeds for -2ns Parts

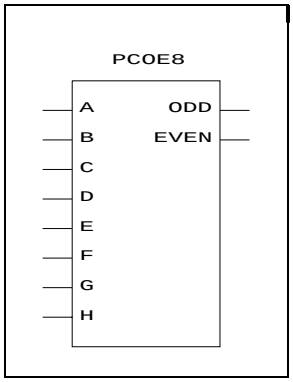
Pin	Rise Min	Rise Typ	Rise Max	Fall Min	Fall Typ	Fall Max
D → ODD.BUS	2.54	4.26	6.18	2.64	4.46	6.38
C → ODD.BUS	2.54	4.26	6.18	2.64	4.46	6.38
B → ODD.BUS	2.07	3.48	4.99	2.17	3.68	5.19
A → ODD.BUS	2.07	3.48	4.99	2.17	3.68	5.19
D → ODD	2.21	3.84	5.67	2.21	3.94	5.77
C → ODD	2.21	3.84	5.67	2.21	3.94	5.77
B → ODD	1.74	3.06	4.48	1.74	3.16	4.58
A → ODD	1.74	3.06	4.48	1.74	3.16	4.58
D → EVEN.BUS	3.41	6.04	8.67	3.41	5.84	8.47
C → EVEN.BUS	3.41	6.04	8.67	3.41	5.84	8.47
B → EVEN.BUS	2.94	5.26	7.48	2.94	5.06	7.28
A → EVEN.BUS	2.94	5.26	7.48	2.94	5.06	7.28
D → EVEN	3.01	5.54	8.07	2.91	5.24	7.77
C → EVEN	3.01	5.54	8.07	2.91	5.24	7.77
B → EVEN	2.54	4.76	6.88	2.44	4.46	6.58
A → EVEN	2.54	4.76	6.88	2.44	4.46	6.58

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
D → ODD.BUS	5.44	7.67	10.55	6.44	8.77	12.05
C → ODD.BUS	5.44	7.67	10.55	6.44	8.77	12.05
B → ODD.BUS	4.37	6.38	8.82	5.37	7.48	10.32
A → ODD.BUS	4.37	6.38	8.82	5.37	7.48	10.32
D → ODD	4.82	6.86	9.26	5.51	7.65	10.37
C → ODD	4.82	6.86	9.26	5.51	7.65	10.37
B → ODD	3.74	5.57	7.53	4.44	6.36	8.64
A → ODD	3.74	5.57	7.53	4.44	6.36	8.64
D → EVEN.BUS	8.11	10.85	14.87	7.82	10.56	14.36
C → EVEN.BUS	8.11	10.85	14.87	7.82	10.56	14.36
B → EVEN.BUS	7.04	9.56	13.14	6.74	9.27	12.63
A → EVEN.BUS	7.04	9.56	13.14	6.74	9.27	12.63
D → EVEN	7.41	9.95	13.47	6.82	9.36	12.56
C → EVEN	7.41	9.95	13.47	6.82	9.36	12.56
B → EVEN	6.34	8.66	11.74	5.74	8.07	10.83
A → EVEN	6.34	8.66	11.74	5.74	8.07	10.83

PCOE8 - 8-Bit Parity Checker Odd/Even

Symbol



Rectangular Area: 4x3cells

Number of Cells: 11

Truth Table

Input A...H	Output EVEN	ODD
even parity	1	0
odd parity	0	1

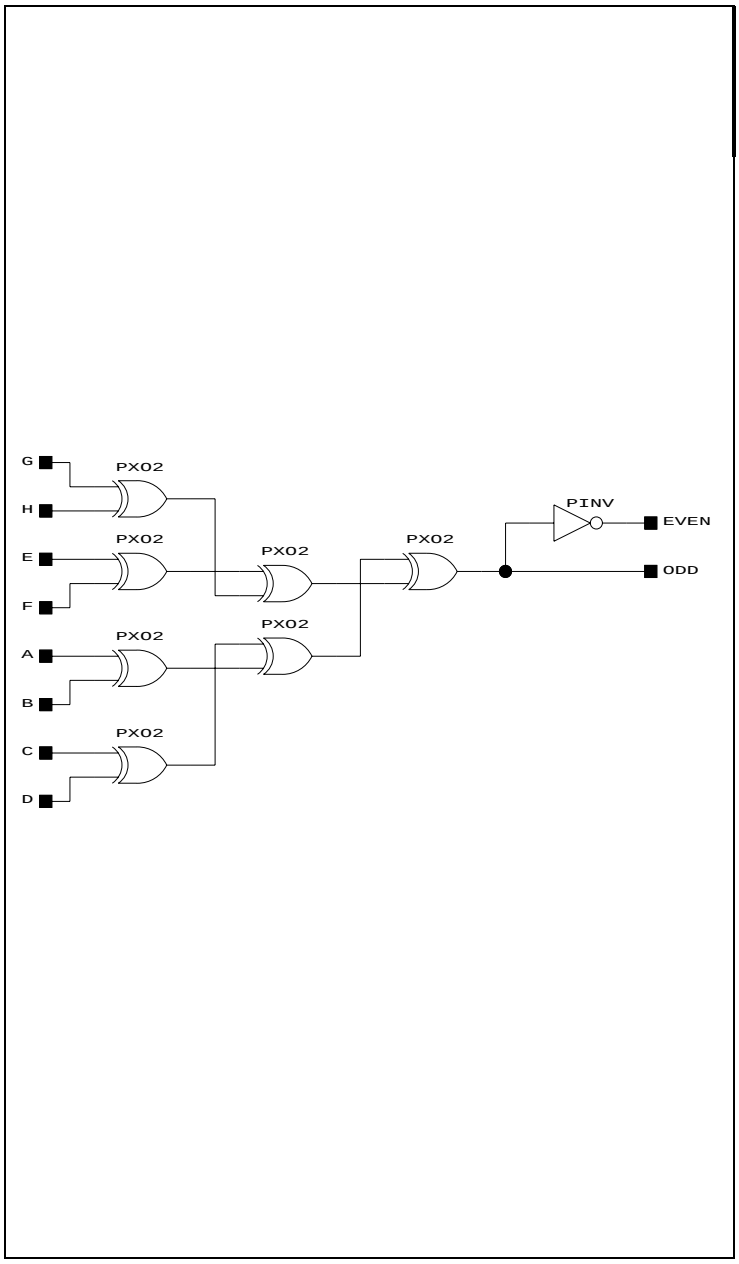
Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
H → EVEN.BUS	4.75	8.40	12.15	4.75	8.20	11.95
G → EVEN.BUS	4.75	8.40	12.15	4.75	8.20	11.95
F → EVEN.BUS	4.28	7.62	10.96	4.28	7.42	10.76
E → EVEN.BUS	4.28	7.62	10.96	4.28	7.42	10.76
D → EVEN.BUS	3.81	6.84	9.77	3.81	6.64	9.57
C → EVEN.BUS	3.81	6.84	9.77	3.81	6.64	9.57
B → EVEN.BUS	4.28	7.62	10.96	4.28	7.42	10.76
A → EVEN.BUS	4.28	7.62	10.96	4.28	7.42	10.76
H → EVEN	4.35	7.90	11.55	4.25	7.60	11.25
G → EVEN	4.35	7.90	11.55	4.25	7.60	11.25
F → EVEN	3.88	7.12	10.36	3.78	6.82	10.06
E → EVEN	3.88	7.12	10.36	3.78	6.82	10.06
D → EVEN	3.41	6.34	9.17	3.31	6.04	8.87
C → EVEN	3.41	6.34	9.17	3.31	6.04	8.87
B → EVEN	3.88	7.12	10.36	3.78	6.82	10.06
A → EVEN	3.88	7.12	10.36	3.78	6.82	10.06
H → ODD.BUS	3.88	6.62	9.66	3.98	6.82	9.86
G → ODD.BUS	3.88	6.62	9.66	3.98	6.82	9.86
F → ODD.BUS	3.41	5.84	8.47	3.51	6.04	8.67
E → ODD.BUS	3.41	5.84	8.47	3.51	6.04	8.67
D → ODD.BUS	2.94	5.06	7.28	3.04	5.26	7.48
C → ODD.BUS	2.94	5.06	7.28	3.04	5.26	7.48
B → ODD.BUS	3.41	5.84	8.47	3.51	6.04	8.67
A → ODD.BUS	3.41	5.84	8.47	3.51	6.04	8.67
H → ODD	3.55	6.20	9.15	3.55	6.30	9.25
G → ODD	3.55	6.20	9.15	3.55	6.30	9.25
F → ODD	3.08	5.42	7.96	3.08	5.52	8.06
E → ODD	3.08	5.42	7.96	3.08	5.52	8.06
D → ODD	2.61	4.64	6.77	2.61	4.74	6.87
C → ODD	2.61	4.64	6.77	2.61	4.74	6.87
B → ODD	3.08	5.42	7.96	3.08	5.52	8.06
A → ODD	3.08	5.42	7.96	3.08	5.52	8.06

Switching Speeds for -4ns Parts

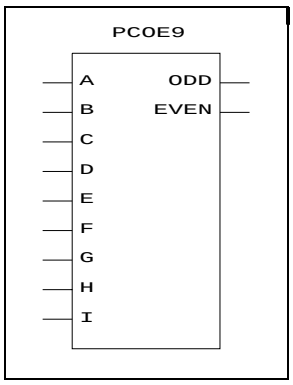
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
H → EVEN.BUS	11.05	15.32	20.93	10.76	15.03	20.42
G → EVEN.BUS	11.05	15.32	20.93	10.76	15.03	20.42
F → EVEN.BUS	9.98	14.03	19.19	9.69	13.74	18.68
E → EVEN.BUS	9.98	14.03	19.19	9.69	13.74	18.68
D → EVEN.BUS	8.91	12.74	17.46	8.62	12.45	16.95
C → EVEN.BUS	8.91	12.74	17.46	8.62	12.45	16.95
B → EVEN.BUS	9.98	14.03	19.19	9.69	13.74	18.68
A → EVEN.BUS	9.98	14.03	19.19	9.69	13.74	18.68
H → EVEN	10.35	14.42	19.53	9.76	13.83	18.62
G → EVEN	10.35	14.42	19.53	9.76	13.83	18.62
F → EVEN	9.28	13.13	17.79	8.69	12.54	16.88
E → EVEN	9.28	13.13	17.79	8.69	12.54	16.88
D → EVEN	8.21	11.84	16.06	7.62	11.25	15.15
C → EVEN	8.21	11.84	16.06	7.62	11.25	15.15
B → EVEN	9.28	13.13	17.79	8.69	12.54	16.88
A → EVEN	9.28	13.13	17.79	8.69	12.54	16.88
H → ODD.BUS	8.39	12.14	16.61	9.39	13.24	18.11
G → ODD.BUS	8.39	12.14	16.61	9.39	13.24	18.11
F → ODD.BUS	7.32	10.85	14.87	8.32	11.95	16.37
E → ODD.BUS	7.32	10.85	14.87	8.32	11.95	16.37
D → ODD.BUS	6.24	9.56	13.14	7.24	10.66	14.64
C → ODD.BUS	6.24	9.56	13.14	7.24	10.66	14.64
B → ODD.BUS	7.32	10.85	14.87	8.32	11.95	16.37
A → ODD.BUS	7.32	10.85	14.87	8.32	11.95	16.37
H → ODD	7.76	11.33	15.32	8.45	12.12	16.43
G → ODD	7.76	11.33	15.32	8.45	12.12	16.43
F → ODD	6.69	10.04	13.58	7.38	10.83	14.69
E → ODD	6.69	10.04	13.58	7.38	10.83	14.69
D → ODD	5.62	8.75	11.85	6.31	9.54	12.96
C → ODD	5.62	8.75	11.85	6.31	9.54	12.96
B → ODD	6.69	10.04	13.58	7.38	10.83	14.69
A → ODD	6.69	10.04	13.58	7.38	10.83	14.69

Schematic



PCOE9 - 9-Bit Parity Checker Odd/Even

Symbol



Rectangular Area: 4x4cells

Number of Cells: 12

Truth Table

Input A...I	Output EVEN	ODD
even parity	1	0
odd parity	0	1

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
B → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
C → ODD.BUS	3.81	6.64	9.57	3.91	6.84	9.77
D → ODD.BUS	3.81	6.64	9.57	3.91	6.84	9.77
E → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
F → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
G → ODD.BUS	4.75	8.20	11.95	4.85	8.40	12.15
H → ODD.BUS	4.75	8.20	11.95	4.85	8.40	12.15
I → ODD.BUS	1.20	1.90	2.70	1.30	2.10	2.90
A → ODD	3.95	7.00	10.25	3.95	7.10	10.35
B → ODD	3.95	7.00	10.25	3.95	7.10	10.35
C → ODD	3.48	6.22	9.06	3.48	6.32	9.16
D → ODD	3.48	6.22	9.06	3.48	6.32	9.16
E → ODD	3.95	7.00	10.25	3.95	7.10	10.35
F → ODD	3.95	7.00	10.25	3.95	7.10	10.35
G → ODD	4.42	7.78	11.44	4.42	7.88	11.54
H → ODD	4.42	7.78	11.44	4.42	7.88	11.54
I → ODD	0.87	1.48	2.19	0.87	1.58	2.29
A → EVEN.BUS	5.15	9.20	13.25	5.15	9.00	13.05
B → EVEN.BUS	5.15	9.20	13.25	5.15	9.00	13.05
C → EVEN.BUS	4.68	8.42	12.06	4.68	8.22	11.86
D → EVEN.BUS	4.68	8.42	12.06	4.68	8.22	11.86
E → EVEN.BUS	5.15	9.20	13.25	5.15	9.00	13.05
F → EVEN.BUS	5.15	9.20	13.25	5.15	9.00	13.05
G → EVEN.BUS	5.62	9.98	14.44	5.62	9.78	14.24
H → EVEN.BUS	5.62	9.98	14.44	5.62	9.78	14.24
I → EVEN.BUS	2.07	3.68	5.19	2.07	3.48	4.99
A → EVEN	4.75	8.70	12.65	4.65	8.40	12.35

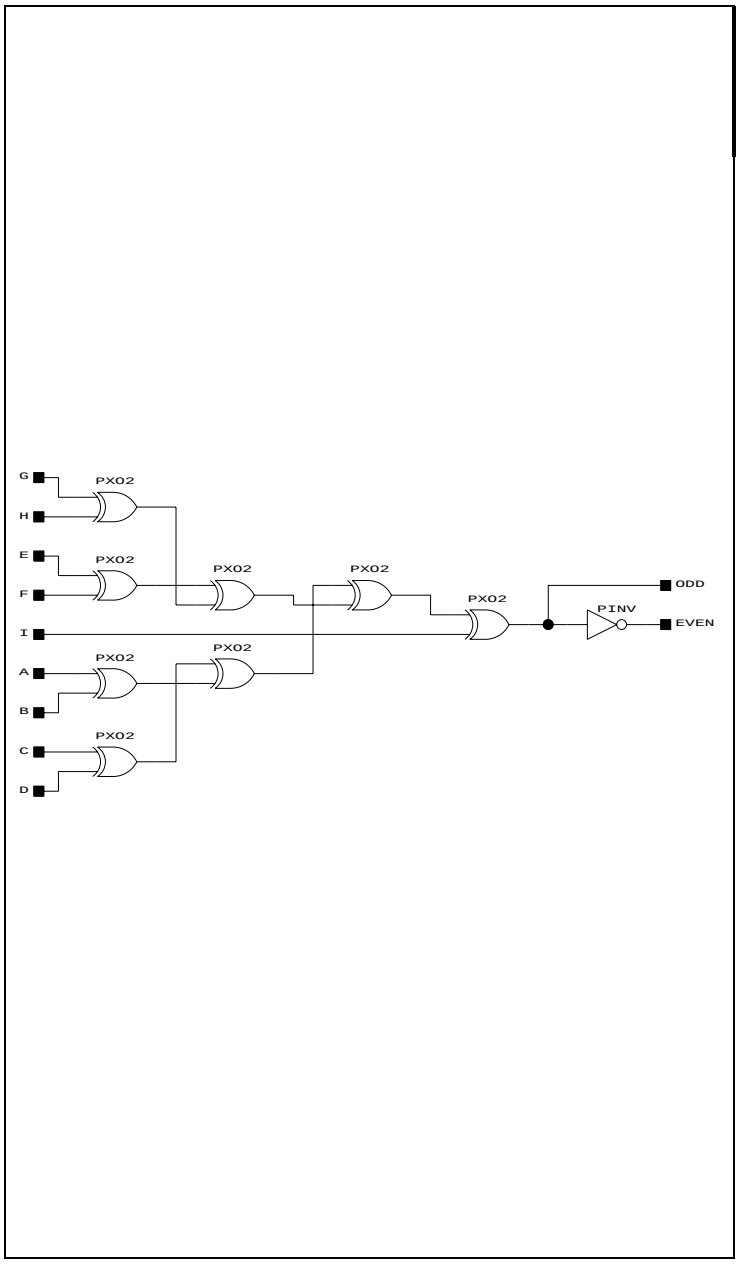
B → EVEN	4.75	8.70	12.65	4.65	8.40	12.35
C → EVEN	4.28	7.92	11.46	4.18	7.62	11.16
D → EVEN	4.28	7.92	11.46	4.18	7.62	11.16
E → EVEN	4.75	8.70	12.65	4.65	8.40	12.35
F → EVEN	4.75	8.70	12.65	4.65	8.40	12.35
G → EVEN	5.22	9.48	13.84	5.12	9.18	13.54
H → EVEN	5.22	9.48	13.84	5.12	9.18	13.54
I → EVEN	1.67	3.18	4.59	1.57	2.88	4.29

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
B → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
C → ODD.BUS	8.12	12.74	17.46	9.12	13.84	18.96
D → ODD.BUS	8.12	12.74	17.46	9.12	13.84	18.96
E → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
F → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
G → ODD.BUS	10.26	15.32	20.93	11.26	16.42	22.43
H → ODD.BUS	10.26	15.32	20.93	11.26	16.42	22.43
I → ODD.BUS	2.50	3.20	4.50	3.50	4.30	6.00
A → ODD	8.56	13.22	17.90	9.25	14.01	19.02
B → ODD	8.56	13.22	17.90	9.25	14.01	19.02
C → ODD	7.49	11.93	16.17	8.18	12.72	17.28
D → ODD	7.49	11.93	16.17	8.18	12.72	17.28
E → ODD	8.56	13.22	17.90	9.25	14.01	19.02
F → ODD	8.56	13.22	17.90	9.25	14.01	19.02
G → ODD	9.63	14.51	19.64	10.32	15.30	20.75
H → ODD	9.63	14.51	19.64	10.32	15.30	20.75
I → ODD	1.87	2.39	3.21	2.56	3.18	4.32
A → EVEN.BUS	11.85	17.21	23.52	11.56	16.92	23.00
B → EVEN.BUS	11.85	17.21	23.52	11.56	16.92	23.00
C → EVEN.BUS	10.78	15.92	21.78	10.49	15.63	21.27
D → EVEN.BUS	10.78	15.92	21.78	10.49	15.63	21.27
E → EVEN.BUS	11.85	17.21	23.52	11.56	16.92	23.00
F → EVEN.BUS	11.85	17.21	23.52	11.56	16.92	23.00
G → EVEN.BUS	12.92	18.50	25.25	12.63	18.21	24.74
H → EVEN.BUS	12.92	18.50	25.25	12.63	18.21	24.74
I → EVEN.BUS	5.16	6.38	8.82	4.87	6.09	8.31
A → EVEN	11.15	16.31	22.12	10.56	15.72	21.20

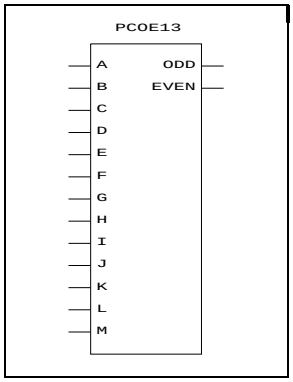
B → EVEN	11.15	16.31	22.12	10.56	15.72	21.20
C → EVEN	10.08	15.02	20.38	9.49	14.43	19.47
D → EVEN	10.08	15.02	20.38	9.49	14.43	19.47
E → EVEN	11.15	16.31	22.12	10.56	15.72	21.20
F → EVEN	11.15	16.31	22.12	10.56	15.72	21.20
G → EVEN	12.22	17.60	23.85	11.63	17.01	22.94
H → EVEN	12.22	17.60	23.85	11.63	17.01	22.94
I → EVEN	4.46	5.48	7.42	3.87	4.89	6.51

Schematic



PCOE13 - 13-Bit Parity Checker Odd/Even

Symbol



Rectangular Area: 5x4cells

Number of Cells: 19

Truth Table

Input A...M	Output EVEN	ODD
even parity	1	0
odd parity	0	1

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → ODD.BUS	4.68	8.22	11.86	4.78	8.42	12.06
B → ODD.BUS	4.68	8.22	11.86	4.78	8.42	12.06
C → ODD.BUS	5.15	9.00	13.05	5.25	9.20	13.25
D → ODD.BUS	5.15	9.00	13.05	5.25	9.20	13.25
E → ODD.BUS	5.62	9.78	14.24	5.72	9.98	14.44
F → ODD.BUS	5.62	9.78	14.24	5.72	9.98	14.44
G → ODD.BUS	5.62	9.78	14.24	5.72	9.98	14.44
H → ODD.BUS	5.62	9.78	14.24	5.72	9.98	14.44
I → ODD.BUS	4.75	8.20	11.95	4.85	8.40	12.15
J → ODD.BUS	4.75	8.20	11.95	4.85	8.40	12.15
K → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
L → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
M → ODD.BUS	1.20	1.90	2.70	1.30	2.10	2.90
A → ODD	4.35	7.80	11.35	4.35	7.90	11.45
B → ODD	4.35	7.80	11.35	4.35	7.90	11.45
C → ODD	4.82	8.58	12.54	4.82	8.68	12.64
D → ODD	4.82	8.58	12.54	4.82	8.68	12.64
E → ODD	5.29	9.36	13.73	5.29	9.46	13.83
F → ODD	5.29	9.36	13.73	5.29	9.46	13.83
G → ODD	5.29	9.36	13.73	5.29	9.46	13.83
H → ODD	5.29	9.36	13.73	5.29	9.46	13.83
I → ODD	4.42	7.78	11.44	4.42	7.88	11.54
J → ODD	4.42	7.78	11.44	4.42	7.88	11.54
K → ODD	3.95	7.00	10.25	3.95	7.10	10.35
L → ODD	3.95	7.00	10.25	3.95	7.10	10.35
M → ODD	0.87	1.48	2.19	0.87	1.58	2.29
A → EVEN.BUS	5.55	10.00	14.35	5.55	9.80	14.15
B → EVEN.BUS	5.55	10.00	14.35	5.55	9.80	14.15

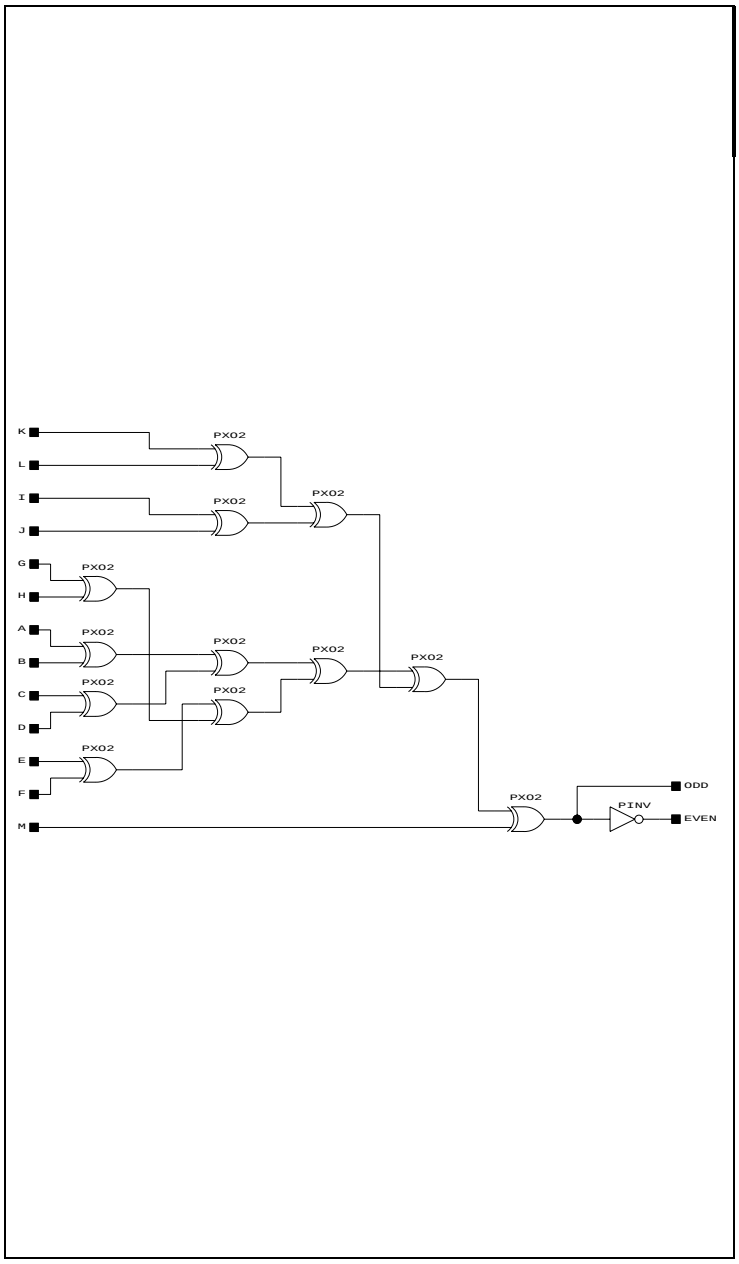
C → EVEN.BUS	6.02	10.78	15.54	6.02	10.58	15.34
D → EVEN.BUS	6.02	10.78	15.54	6.02	10.58	15.34
E → EVEN.BUS	6.49	11.56	16.73	6.49	11.36	16.53
F → EVEN.BUS	6.49	11.56	16.73	6.49	11.36	16.53
G → EVEN.BUS	6.49	11.56	16.73	6.49	11.36	16.53
H → EVEN.BUS	6.49	11.56	16.73	6.49	11.36	16.53
I → EVEN.BUS	5.62	9.98	14.44	5.62	9.78	14.24
J → EVEN.BUS	5.62	9.98	14.44	5.62	9.78	14.24
K → EVEN.BUS	5.15	9.20	13.25	5.15	9.00	13.05
L → EVEN.BUS	5.15	9.20	13.25	5.15	9.00	13.05
M → EVEN.BUS	2.07	3.68	5.19	2.07	3.48	4.99
A → EVEN	5.15	9.50	13.75	5.05	9.20	13.45
B → EVEN	5.15	9.50	13.75	5.05	9.20	13.45
C → EVEN	5.62	10.28	14.94	5.52	9.98	14.64
D → EVEN	5.62	10.28	14.94	5.52	9.98	14.64
E → EVEN	6.09	11.06	16.13	5.99	10.76	15.83
F → EVEN	6.09	11.06	16.13	5.99	10.76	15.83
G → EVEN	6.09	11.06	16.13	5.99	10.76	15.83
H → EVEN	6.09	11.06	16.13	5.99	10.76	15.83
I → EVEN	5.22	9.48	13.84	5.12	9.18	13.54
J → EVEN	5.22	9.48	13.84	5.12	9.18	13.54
K → EVEN	4.75	8.70	12.65	4.65	8.40	12.35
L → EVEN	4.75	8.70	12.65	4.65	8.40	12.35
M → EVEN	1.67	3.18	4.59	1.57	2.88	4.29

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → ODD.BUS	9.99	15.92	21.78	10.99	17.02	23.28
B → ODD.BUS	9.99	15.92	21.78	10.99	17.02	23.28
C → ODD.BUS	11.06	17.21	23.52	12.06	18.31	25.02
D → ODD.BUS	11.06	17.21	23.52	12.06	18.31	25.02
E → ODD.BUS	12.13	18.50	25.35	13.13	19.60	26.85
F → ODD.BUS	12.13	18.50	25.35	13.13	19.60	26.85
G → ODD.BUS	12.13	18.50	25.25	13.13	19.60	26.75
H → ODD.BUS	12.13	18.50	25.25	13.13	19.60	26.75
I → ODD.BUS	10.26	15.32	20.93	11.26	16.42	22.43
J → ODD.BUS	10.26	15.32	20.93	11.26	16.42	22.43
K → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
L → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
M → ODD.BUS	2.50	3.20	4.50	3.50	4.30	6.00
A → ODD	9.36	15.11	20.49	10.05	15.90	21.60
B → ODD	9.36	15.11	20.49	10.05	15.90	21.60
C → ODD	10.43	16.40	22.22	11.12	17.19	23.34
D → ODD	10.43	16.40	22.22	11.12	17.19	23.34
E → ODD	11.50	17.69	24.06	12.20	18.48	25.17
F → ODD	11.50	17.69	24.06	12.20	18.48	25.17
G → ODD	11.50	17.69	23.96	12.20	18.48	25.07
H → ODD	11.50	17.69	23.96	12.20	18.48	25.07
I → ODD	9.63	14.51	19.64	10.32	15.30	20.75
J → ODD	9.63	14.51	19.64	10.32	15.30	20.75
K → ODD	8.56	13.22	17.90	9.25	14.01	19.02
L → ODD	8.56	13.22	17.90	9.25	14.01	19.02
M → ODD	1.87	2.39	3.21	2.56	3.18	4.32
A → EVEN.BUS	12.65	19.10	26.10	12.36	18.81	25.59
B → EVEN.BUS	12.65	19.10	26.10	12.36	18.81	25.59

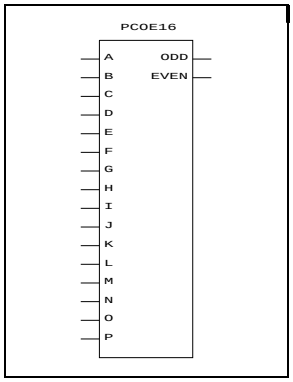
C → EVEN.BUS	13.72	20.39	27.84	13.43	20.10	27.32
D → EVEN.BUS	13.72	20.39	27.84	13.43	20.10	27.32
E → EVEN.BUS	14.80	21.68	29.67	14.50	21.39	29.16
F → EVEN.BUS	14.80	21.68	29.67	14.50	21.39	29.16
G → EVEN.BUS	14.80	21.68	29.57	14.50	21.39	29.06
H → EVEN.BUS	14.80	21.68	29.57	14.50	21.39	29.06
I → EVEN.BUS	12.92	18.50	25.25	12.63	18.21	24.74
J → EVEN.BUS	12.92	18.50	25.25	12.63	18.21	24.74
K → EVEN.BUS	11.85	17.21	23.52	11.56	16.92	23.00
L → EVEN.BUS	11.85	17.21	23.52	11.56	16.92	23.00
M → EVEN.BUS	5.16	6.38	8.82	4.87	6.09	8.31
A → EVEN	11.95	18.20	24.70	11.36	17.61	23.79
B → EVEN	11.95	18.20	24.70	11.36	17.61	23.79
C → EVEN	13.02	19.49	26.44	12.43	18.90	25.52
D → EVEN	13.02	19.49	26.44	12.43	18.90	25.52
E → EVEN	14.10	20.78	28.27	13.50	20.19	27.36
F → EVEN	14.10	20.78	28.27	13.50	20.19	27.36
G → EVEN	14.10	20.78	28.17	13.50	20.19	27.26
H → EVEN	14.10	20.78	28.17	13.50	20.19	27.26
I → EVEN	12.22	17.60	23.85	11.63	17.01	22.94
J → EVEN	12.22	17.60	23.85	11.63	17.01	22.94
K → EVEN	11.15	16.31	22.12	10.56	15.72	21.20
L → EVEN	11.15	16.31	22.12	10.56	15.72	21.20
M → EVEN	4.46	5.48	7.42	3.87	4.89	6.51

Schematic


K
L
I
J
G
H
A
B
C
D
E
F
M
PXO2
PXO2
PXO2
PXO2
PXO2
PXO2
PXO2
PXO2
PXO2
PXO2
PINV
ODD
EVEN

PCOE16 - 16-Bit Parity Checker Odd/Even

Symbol



Rectangular Area: 6x5cells

Number of Cells: 24

Truth Table

Input A...P	Output EVEN	ODD
even parity	1	0
odd parity	0	1

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
P → EVEN.BUS	6.09	10.76	15.63	6.10	10.57	15.44
O → EVEN.BUS	6.09	10.76	15.63	6.10	10.57	15.44
N → EVEN.BUS	5.62	9.98	14.44	5.63	9.79	14.25
M → EVEN.BUS	5.62	9.98	14.44	5.63	9.79	14.25
L → EVEN.BUS	5.15	9.20	13.25	5.16	9.01	13.06
K → EVEN.BUS	5.15	9.20	13.25	5.16	9.01	13.0
J → EVEN.BUS	5.62	9.98	14.44	5.63	9.79	14.25
I → EVEN.BUS	5.62	9.98	14.44	5.63	9.79	14.25
H → EVEN.BUS	6.56	11.54	16.82	6.57	11.35	16.63
G → EVEN.BUS	6.56	11.54	16.82	6.57	11.35	16.63
F → EVEN.BUS	6.09	10.76	15.63	6.10	10.57	15.44
E → EVEN.BUS	6.09	10.76	15.63	6.10	10.57	15.44
D → EVEN.BUS	5.62	9.98	14.44	5.63	9.79	14.25
C → EVEN.BUS	5.62	9.98	14.44	5.63	9.79	14.25
B → EVEN.BUS	6.09	10.76	15.63	6.10	10.57	15.44
A → EVEN.BUS	6.09	10.76	15.63	6.10	10.57	15.44
P → EVEN	5.69	10.26	15.03	5.60	9.97	14.74
O → EVEN	5.69	10.26	15.03	5.60	9.97	14.74
N → EVEN	5.22	9.48	13.84	5.13	9.19	13.55
M → EVEN	5.22	9.48	13.84	5.13	9.19	13.55
L → EVEN	4.75	8.70	12.65	4.66	8.41	12.36
K → EVEN	4.75	8.70	12.65	4.66	8.41	12.36
J → EVEN	5.22	9.48	13.84	5.13	9.19	13.55
I → EVEN	5.22	9.48	13.84	5.13	9.19	13.55
H → EVEN	6.16	11.04	16.22	6.07	10.75	15.93
G → EVEN	6.16	11.04	16.22	6.07	10.75	15.93
F → EVEN	5.69	10.26	15.03	5.60	9.97	14.74
E → EVEN	5.69	10.26	15.03	5.60	9.97	14.74

D → EVEN	5.22	9.48	13.84	5.13	9.19	13.55
C → EVEN	5.22	9.48	13.84	5.13	9.19	13.55
B → EVEN	5.69	10.26	15.03	5.60	9.97	14.74
A → EVEN	5.69	10.26	15.03	5.60	9.97	14.74
P → ODD.BUS	4.75	8.20	11.95	4.85	8.40	12.15
O → ODD.BUS	4.75	8.20	11.95	4.85	8.40	12.15
N → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
M → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
L → ODD.BUS	3.81	6.64	9.57	3.91	6.84	9.77
K → ODD.BUS	3.81	6.64	9.57	3.91	6.84	9.77
J → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
I → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
H → ODD.BUS	5.22	8.98	13.14	5.32	9.18	13.34
G → ODD.BUS	5.22	8.98	13.14	5.32	9.18	13.34
F → ODD.BUS	4.75	8.20	11.95	4.85	8.40	12.15
E → ODD.BUS	4.75	8.20	11.95	4.85	8.40	12.15
D → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
C → ODD.BUS	4.28	7.42	10.76	4.38	7.62	10.96
B → ODD.BUS	4.75	8.20	11.95	4.85	8.40	12.15
A → ODD.BUS	4.75	8.20	11.95	4.85	8.40	12.15
P → ODD	4.42	7.78	11.44	4.42	7.88	11.54
O → ODD	4.42	7.78	11.44	4.42	7.88	11.54
N → ODD	3.95	7.00	10.25	3.95	7.10	10.35
M → ODD	3.95	7.00	10.25	3.95	7.10	10.35
L → ODD	3.48	6.22	9.06	3.48	6.32	9.16
K → ODD	3.48	6.22	9.06	3.48	6.32	9.16
J → ODD	3.95	7.00	10.25	3.95	7.10	10.35
I → ODD	3.95	7.00	10.25	3.95	7.10	10.35
H → ODD	4.89	8.56	12.63	4.89	8.66	12.73
G → ODD	4.89	8.56	12.63	4.89	8.66	12.73
F → ODD	4.42	7.78	11.44	4.42	7.88	11.54
E → ODD	4.42	7.78	11.44	4.42	7.88	11.54

D → ODD	3.95	7.00	10.25	3.95	7.10	10.35
C → ODD	3.95	7.00	10.25	3.95	7.10	10.35
B → ODD	4.42	7.78	11.44	4.42	7.88	11.54
A → ODD	4.42	7.78	11.44	4.42	7.88	11.54

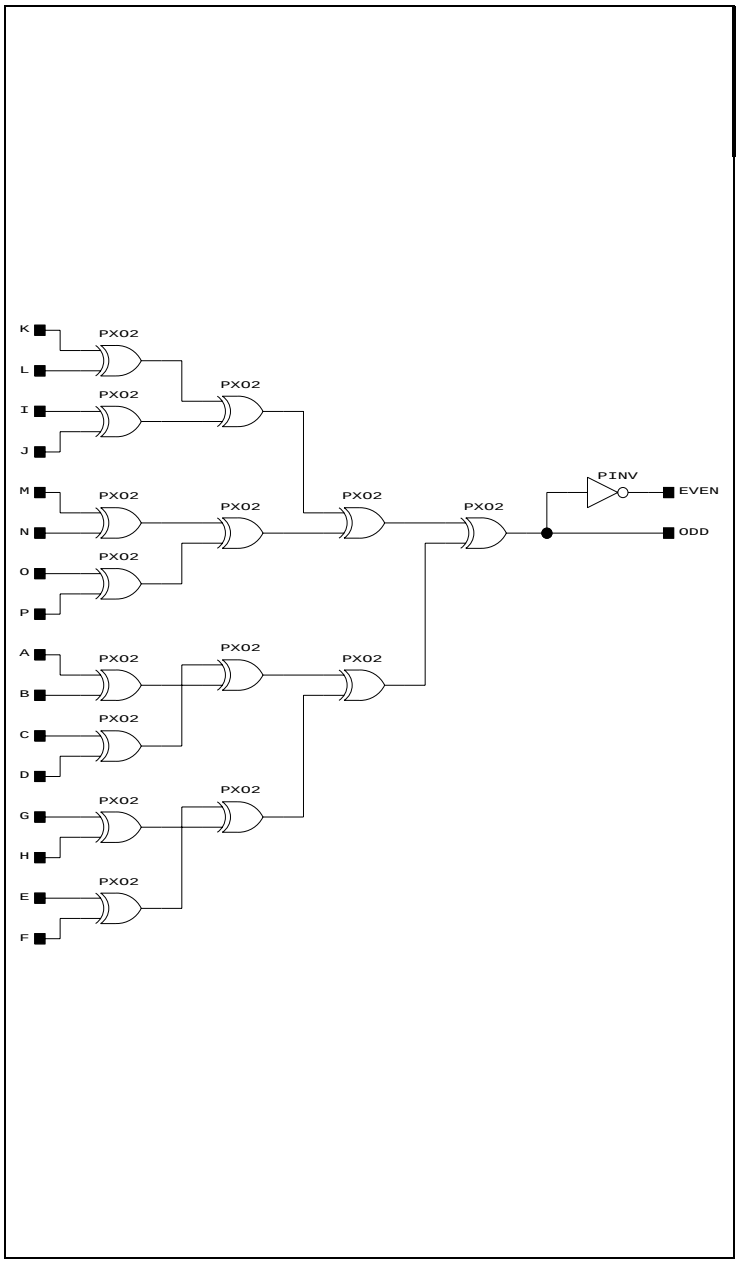
Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
P → EVEN.BUS	14.00	19.79	27.08	13.70	19.60	26.56
O → EVEN.BUS	14.00	19.79	27.08	13.70	19.60	26.56
N → EVEN.BUS	12.92	18.50	25.35	12.63	18.31	24.82
M → EVEN.BUS	12.92	18.50	25.35	12.63	18.31	24.82
L → EVEN.BUS	11.85	17.21	23.62	11.56	17.02	23.09
K → EVEN.BUS	11.85	17.21	23.62	11.56	17.02	23.09
J → EVEN.BUS	12.92	18.50	25.35	12.63	18.31	24.82
I → EVEN.BUS	12.92	18.50	25.35	12.63	18.31	24.82
H → EVEN.BUS	15.07	21.08	28.81	14.78	20.89	28.29
G → EVEN.BUS	15.07	21.08	28.81	14.78	20.89	28.29
F → EVEN.BUS	14.00	19.79	27.08	13.70	19.60	26.56
E → EVEN.BUS	14.00	19.79	27.08	13.70	19.60	26.56
D → EVEN.BUS	12.92	18.50	25.35	12.63	18.31	24.82
C → EVEN.BUS	12.92	18.50	25.35	12.63	18.31	24.82
B → EVEN.BUS	14.00	19.79	27.08	13.70	19.60	26.56
A → EVEN.BUS	14.00	19.79	27.08	13.70	19.60	26.56
P → EVEN	13.30	18.89	25.68	12.70	18.40	24.76
O → EVEN	13.30	18.89	25.68	12.70	18.40	24.76
N → EVEN	12.22	17.60	23.95	11.63	17.11	23.02
M → EVEN	12.22	17.60	23.95	11.63	17.11	23.02
L → EVEN	11.15	16.31	22.22	10.56	15.82	21.29
K → EVEN	11.15	16.31	22.22	10.56	15.82	21.29
J → EVEN	12.22	17.60	23.95	11.63	17.11	23.02
I → EVEN	12.22	17.60	23.95	11.63	17.11	23.02
H → EVEN	14.37	20.18	27.41	13.78	19.69	26.49
G → EVEN	14.37	20.18	27.41	13.78	19.69	26.49
F → EVEN	13.30	18.89	25.68	12.70	18.40	24.76
E → EVEN	13.30	18.89	25.68	12.70	18.40	24.76

D → EVEN	12.22	17.60	23.95	11.63	17.11	23.02
C → EVEN	12.22	17.60	23.95	11.63	17.11	23.02
B → EVEN	13.30	18.89	25.68	12.70	18.40	24.76
A → EVEN	13.30	18.89	25.68	12.70	18.40	24.76
P → ODD.BUS	10.26	15.32	20.93	11.26	16.42	22.43
O → ODD.BUS	10.26	15.32	20.93	11.26	16.42	22.43
N → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
M → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
L → ODD.BUS	8.12	12.74	17.46	9.12	13.84	18.96
K → ODD.BUS	8.12	12.74	17.46	9.12	13.84	18.96
J → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
I → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
H → ODD.BUS	11.33	16.61	22.66	12.33	17.71	24.16
G → ODD.BUS	11.33	16.61	22.66	12.33	17.71	24.16
F → ODD.BUS	10.26	15.32	20.93	11.26	16.42	22.43
E → ODD.BUS	10.26	15.32	20.93	11.26	16.42	22.43
D → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
C → ODD.BUS	9.19	14.03	19.19	10.19	15.13	20.69
B → ODD.BUS	10.26	15.32	20.93	11.26	16.42	22.43
A → ODD.BUS	10.26	15.32	20.93	11.26	16.42	22.43
P → ODD	9.63	14.51	19.64	10.32	15.30	20.75
O → ODD	9.63	14.51	19.64	10.32	15.30	20.75
N → ODD	8.56	13.22	17.90	9.25	14.01	19.02
M → ODD	8.56	13.22	17.90	9.25	14.01	19.02
L → ODD	7.49	11.93	16.17	8.18	12.72	17.28
K → ODD	7.49	11.93	16.17	8.18	12.72	17.28
J → ODD	8.56	13.22	17.90	9.25	14.01	19.02
I → ODD	8.56	13.22	17.90	9.25	14.01	19.02
H → ODD	10.70	15.80	21.37	11.40	16.59	22.48
G → ODD	10.70	15.80	21.37	11.40	16.59	22.48
F → ODD	9.63	14.51	19.64	10.32	15.30	20.75
E → ODD	9.63	14.51	19.64	10.32	15.30	20.75

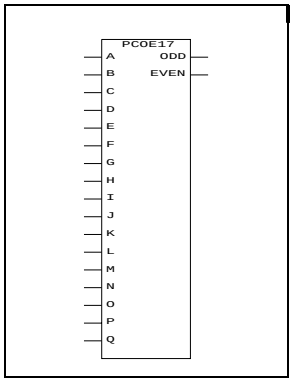
D → ODD	8.56	13.22	17.90	9.25	14.01	19.02
C → ODD	8.56	13.22	17.90	9.25	14.01	19.02
B → ODD	9.63	14.51	19.64	10.32	15.30	20.75
A → ODD	9.63	14.51	19.64	10.32	15.30	20.75

Schematic



PCOE17 - 17-Bit Parity Checker Odd/Even

Symbol



Rectangular Area: 6x5cells

Number of Cells: 24

Truth Table

Input A...Q	Output EVEN	ODD
even parity	1	0
odd parity	0	1

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
O → EVEN.BUS	6.49	11.56	16.73	6.49	11.36	16.53
P → EVEN.BUS	6.49	11.56	16.73	6.49	11.36	16.53
N → EVEN.BUS	6.02	10.78	15.54	6.02	10.58	15.34
M → EVEN.BUS	6.02	10.78	15.54	6.02	10.58	15.34
L → EVEN.BUS	6.49	11.56	16.73	6.49	11.36	16.53
K → EVEN.BUS	6.49	11.56	16.73	6.49	11.36	16.53
J → EVEN.BUS	6.96	12.34	17.92	6.96	12.14	17.72
I → EVEN.BUS	6.96	12.34	17.92	6.96	12.14	17.72
H → EVEN.BUS	6.49	11.56	16.73	6.49	11.36	16.53
G → EVEN.BUS	6.49	11.56	16.73	6.49	11.36	16.53
F → EVEN.BUS	6.02	10.78	15.54	6.02	10.58	15.34
E → EVEN.BUS	6.02	10.78	15.54	6.02	10.58	15.34
D → EVEN.BUS	5.55	10.00	14.35	5.55	9.80	14.15
C → EVEN.BUS	5.55	10.00	14.35	5.55	9.80	14.15
B → EVEN.BUS	6.02	10.78	15.54	6.02	10.58	15.34
A → EVEN.BUS	6.02	10.78	15.54	6.02	10.58	15.34
Q → EVEN.BUS	2.07	3.68	5.19	2.07	3.48	4.99
O → EVEN	6.09	11.06	16.13	5.99	10.76	15.83
P → EVEN	6.09	11.06	16.13	5.99	10.76	15.83
N → EVEN	5.62	10.28	14.94	5.52	9.98	14.64
M → EVEN	5.62	10.28	14.94	5.52	9.98	14.64
L → EVEN	6.09	11.06	16.13	5.99	10.76	15.83
K → EVEN	6.09	11.06	16.13	5.99	10.76	15.83
J → EVEN	6.56	11.84	17.32	6.46	11.54	17.02
I → EVEN	6.56	11.84	17.32	6.46	11.54	17.02
H → EVEN	6.09	11.06	16.13	5.99	10.76	15.83
G → EVEN	6.09	11.06	16.13	5.99	10.76	15.83
F → EVEN	5.62	10.28	14.94	5.52	9.98	14.64

E → EVEN	5.62	10.28	14.94	5.52	9.98	14.64
D → EVEN	5.15	9.50	13.75	5.05	9.20	13.45
C → EVEN	5.15	9.50	13.75	5.05	9.20	13.45
B → EVEN	5.62	10.28	14.94	5.52	9.98	14.64
A → EVEN	5.62	10.28	14.94	5.52	9.98	14.64
Q → EVEN	1.67	3.18	4.59	1.57	2.88	4.29
O → ODD.BUS	5.62	9.78	14.24	5.72	9.98	14.44
P → ODD.BUS	5.62	9.78	14.24	5.72	9.98	14.44
N → ODD.BUS	5.15	9.00	13.05	5.25	9.20	13.25
M → ODD.BUS	5.15	9.00	13.05	5.25	9.20	13.25
L → ODD.BUS	5.62	9.78	14.24	5.72	9.98	14.44
K → ODD.BUS	5.62	9.78	14.24	5.72	9.98	14.44
J → ODD.BUS	6.09	10.56	15.43	6.19	10.76	15.63
I → ODD.BUS	6.09	10.56	15.43	6.19	10.76	15.63
H → ODD.BUS	5.62	9.78	14.24	5.72	9.98	14.44
G → ODD.BUS	5.62	9.78	14.24	5.72	9.98	14.44
F → ODD.BUS	5.15	9.00	13.05	5.25	9.20	13.25
E → ODD.BUS	5.15	9.00	13.05	5.25	9.20	13.25
D → ODD.BUS	4.68	8.22	11.86	4.78	8.42	12.06
C → ODD.BUS	4.68	8.22	11.86	4.78	8.42	12.06
B → ODD.BUS	5.15	9.00	13.05	5.25	9.20	13.25
A → ODD.BUS	5.15	9.00	13.05	5.25	9.20	13.25
Q → ODD.BUS	1.20	1.90	2.70	1.30	2.10	2.90
O → ODD	5.29	9.36	13.73	5.29	9.46	13.83
P → ODD	5.29	9.36	13.73	5.29	9.46	13.83
N → ODD	4.82	8.58	12.54	4.82	8.68	12.64
M → ODD	4.82	8.58	12.54	4.82	8.68	12.64
L → ODD	5.29	9.36	13.73	5.29	9.46	13.83
K → ODD	5.29	9.36	13.73	5.29	9.46	13.83
J → ODD	5.76	10.14	14.92	5.76	10.24	15.02
I → ODD	5.76	10.14	14.92	5.76	10.24	15.02
H → ODD	5.29	9.36	13.73	5.29	9.46	13.83

G → ODD	5.29	9.36	13.73	5.29	9.46	13.8
F → ODD	4.82	8.58	12.54	4.82	8.68	12.64
E → ODD	4.82	8.58	12.54	4.82	8.68	12.64
D → ODD	4.35	7.80	11.35	4.35	7.90	11.45
C → ODD	4.35	7.80	11.35	4.35	7.90	11.45
B → ODD	4.82	8.58	12.54	4.82	8.68	12.64
A → ODD	4.82	8.58	12.54	4.82	8.68	12.64
Q → ODD	0.87	1.48	2.19	0.87	1.58	2.29

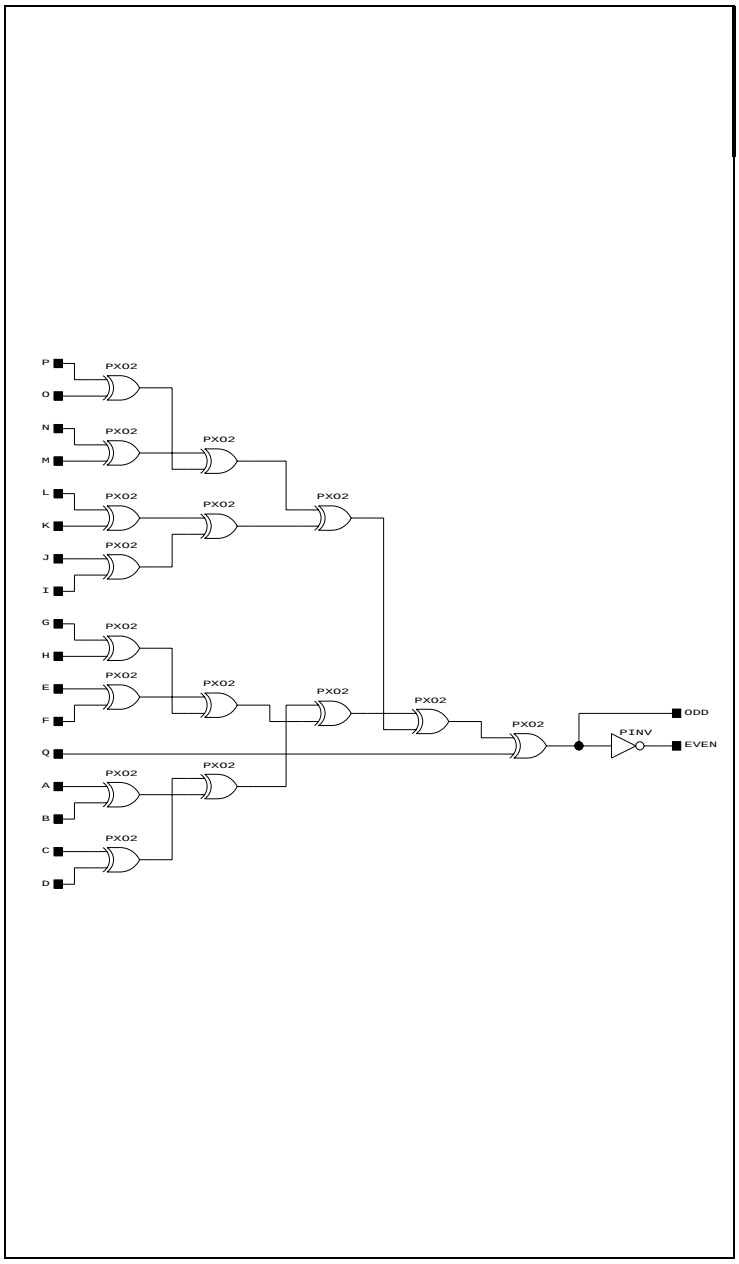
Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
O → EVEN.BUS	14.80	21.68	29.57	14.50	21.39	29.06
P → EVEN.BUS	14.80	21.68	29.57	14.50	21.39	29.06
N → EVEN.BUS	13.72	20.39	27.84	13.43	20.10	27.32
M → EVEN.BUS	13.72	20.39	27.84	13.43	20.10	27.32
L → EVEN.BUS	14.80	21.68	29.57	14.50	21.39	29.06
K → EVEN.BUS	14.80	21.68	29.57	14.50	21.39	29.06
J → EVEN.BUS	15.87	22.97	31.30	15.58	22.68	30.79
I → EVEN.BUS	15.87	22.97	31.30	15.58	22.68	30.79
H → EVEN.BUS	14.80	21.68	29.57	14.50	21.39	29.06
G → EVEN.BUS	14.80	21.68	29.57	14.50	21.39	29.06
F → EVEN.BUS	13.72	20.39	27.84	13.43	20.10	27.32
E → EVEN.BUS	13.72	20.39	27.84	13.43	20.10	27.32
D → EVEN.BUS	12.65	19.10	26.10	12.36	18.81	25.59
C → EVEN.BUS	12.65	19.10	26.10	12.36	18.81	25.59
B → EVEN.BUS	13.72	20.39	27.84	13.43	20.10	27.32
A → EVEN.BUS	13.72	20.39	27.84	13.43	20.10	27.32
Q → EVEN.BUS	5.16	6.38	8.82	4.87	6.09	8.31
O → EVEN	14.10	20.78	28.17	13.50	20.19	27.26
P → EVEN	14.10	20.78	28.17	13.50	20.19	27.26
N → EVEN	13.02	19.49	26.44	12.43	18.90	25.52
M → EVEN	13.02	19.49	26.44	12.43	18.90	25.52
L → EVEN	14.10	20.78	28.17	13.50	20.19	27.26
K → EVEN	14.10	20.78	28.17	13.50	20.19	27.26
J → EVEN	15.17	22.07	29.90	14.58	21.48	28.99
I → EVEN	15.17	22.07	29.90	14.58	21.48	28.99
H → EVEN	14.10	20.78	28.17	13.50	20.19	27.26
G → EVEN	14.10	20.78	28.17	13.50	20.19	27.26
F → EVEN	13.02	19.49	26.44	12.43	18.90	25.52

E → EVEN	13.02	19.49	26.44	12.43	18.90	25.52
D → EVEN	11.95	18.20	24.70	11.36	17.61	23.79
C → EVEN	11.95	18.20	24.70	11.36	17.61	23.79
B → EVEN	13.02	19.49	26.44	12.43	18.90	25.52
A → EVEN	13.02	19.49	26.44	12.43	18.90	25.52
Q → EVEN	4.46	5.48	7.42	3.87	4.89	6.51
O → ODD.BUS	12.13	18.50	25.25	13.13	19.60	26.75
P → ODD.BUS	12.13	18.50	25.25	13.13	19.60	26.75
N → ODD.BUS	11.06	17.21	23.52	12.06	18.31	25.02
M → ODD.BUS	11.06	17.21	23.52	12.06	18.31	25.02
L → ODD.BUS	12.13	18.50	25.25	13.13	19.60	26.75
K → ODD.BUS	12.13	18.50	25.25	13.13	19.60	26.75
J → ODD.BUS	13.20	19.79	26.98	14.20	20.89	28.48
I → ODD.BUS	13.20	19.79	26.98	14.20	20.89	28.48
H → ODD.BUS	12.13	18.50	25.25	13.13	19.60	26.75
G → ODD.BUS	12.13	18.50	25.25	13.13	19.60	26.75
F → ODD.BUS	11.06	17.21	23.52	12.06	18.31	25.02
E → ODD.BUS	11.06	17.21	23.52	12.06	18.31	25.02
D → ODD.BUS	9.99	15.92	21.78	10.99	17.02	23.28
C → ODD.BUS	9.99	15.92	21.78	10.99	17.02	23.28
B → ODD.BUS	11.06	17.21	23.52	12.06	18.31	25.02
A → ODD.BUS	11.06	17.21	23.52	12.06	18.31	25.02
Q → ODD.BUS	2.50	3.20	4.50	3.50	4.30	6.00
O → ODD	11.50	17.69	23.96	12.20	18.48	25.07
P → ODD	11.50	17.69	23.96	12.20	18.48	25.07
N → ODD	10.43	16.40	22.22	11.12	17.19	23.34
M → ODD	10.43	16.40	22.22	11.12	17.19	23.34
L → ODD	11.50	17.69	23.96	12.20	18.48	25.07
K → ODD	11.50	17.69	23.96	12.20	18.48	25.07
J → ODD	12.58	18.98	25.69	13.27	19.77	26.80
I → ODD	12.58	18.98	25.69	13.27	19.77	26.80
H → ODD	11.50	17.69	23.96	12.20	18.48	25.07

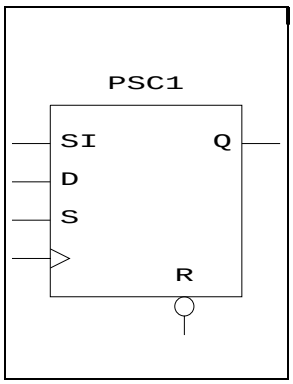
G → ODD	11.50	17.69	23.96	12.20	18.48	25.07
F → ODD	10.43	16.40	22.22	11.12	17.19	23.34
E → ODD	10.43	16.40	22.22	11.12	17.19	23.34
D → ODD	9.36	15.11	20.49	10.05	15.90	21.60
C → ODD	9.36	15.11	20.49	10.05	15.90	21.60
B → ODD	10.43	16.40	22.22	11.12	17.19	23.34
A → ODD	10.43	16.40	22.22	11.12	17.19	23.34
Q → ODD	1.87	2.39	3.21	2.56	3.18	4.32

Schematic



PSC1 - 1-Bit Parallel-to-Serial Converter

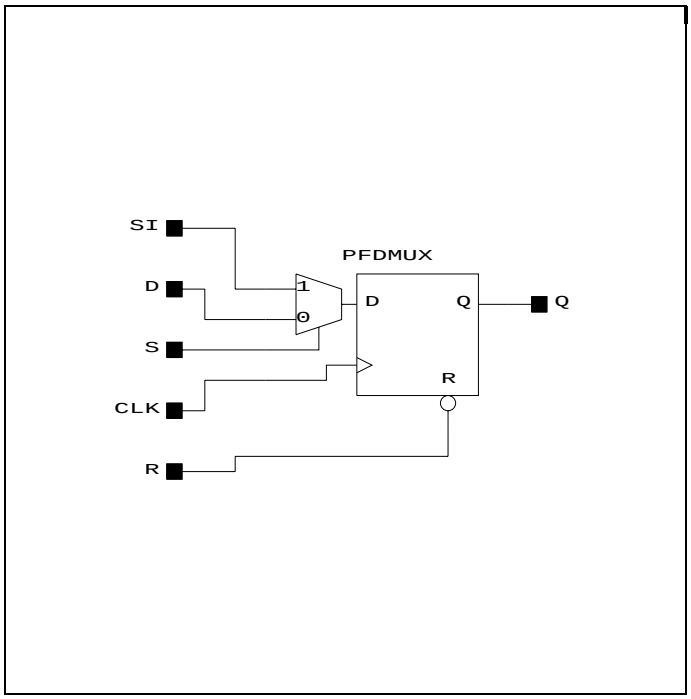
Symbol



Rectangular Area: 1x1cells

Number of Cells: 1

Schematic



Truth Table

Input					Output
R	CLK	S	SI	D	Q
0	x	x	x	x	0
1	r	1	si	x	si
1	r	0	x	d	d

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20
R → Q	0.00	0.00	0.00	1.40	1.60	1.80

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D	3.90	4.10	4.30	0.00	0.00	0.00
SI	3.90	4.10	4.30	0.00	0.00	0.00
S	3.80	4.00	4.30	0.00	0.00	0.00

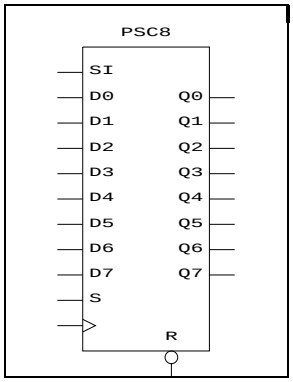
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60
R → Q	0.00	0.00	0.00	2.40	2.70	3.00

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D	6.30	6.60	6.90	0.00	0.00	0.00
SI	6.30	6.60	6.90	0.00	0.00	0.00
S	6.10	6.40	6.70	0.00	0.00	0.00

PSC8 - 8-Bit Parallel-to-Serial Converter

Symbol



Rectangular Area: 1x8cells

Number of Cells: 8

Truth Table

Input					Output
R	**CLK**	**S**	**SI**	**D7...D0**	**Q7...Q0**
0	x	x	x	x...x	0...0
1	r	0	x	d7...d0	d7...d0
1	r	1	si	x...x	q6...si

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q7	-	-	-	1.40	1.60	1.80
CLK → Q7	1.40	1.60	1.80	1.80	2.00	2.20
R → Q6	-	-	-	1.48	1.71	1.93
CLK → Q6	1.49	1.71	1.92	1.88	2.11	2.33
R → Q5	-	-	-	1.48	1.71	1.93
CLK → Q5	1.49	1.71	1.92	1.88	2.11	2.33
R → Q4	-	-	-	1.48	1.71	1.93
CLK → Q4	1.49	1.71	1.92	1.88	2.11	2.33
R → Q3	-	-	-	1.48	1.71	1.93
CLK → Q3	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

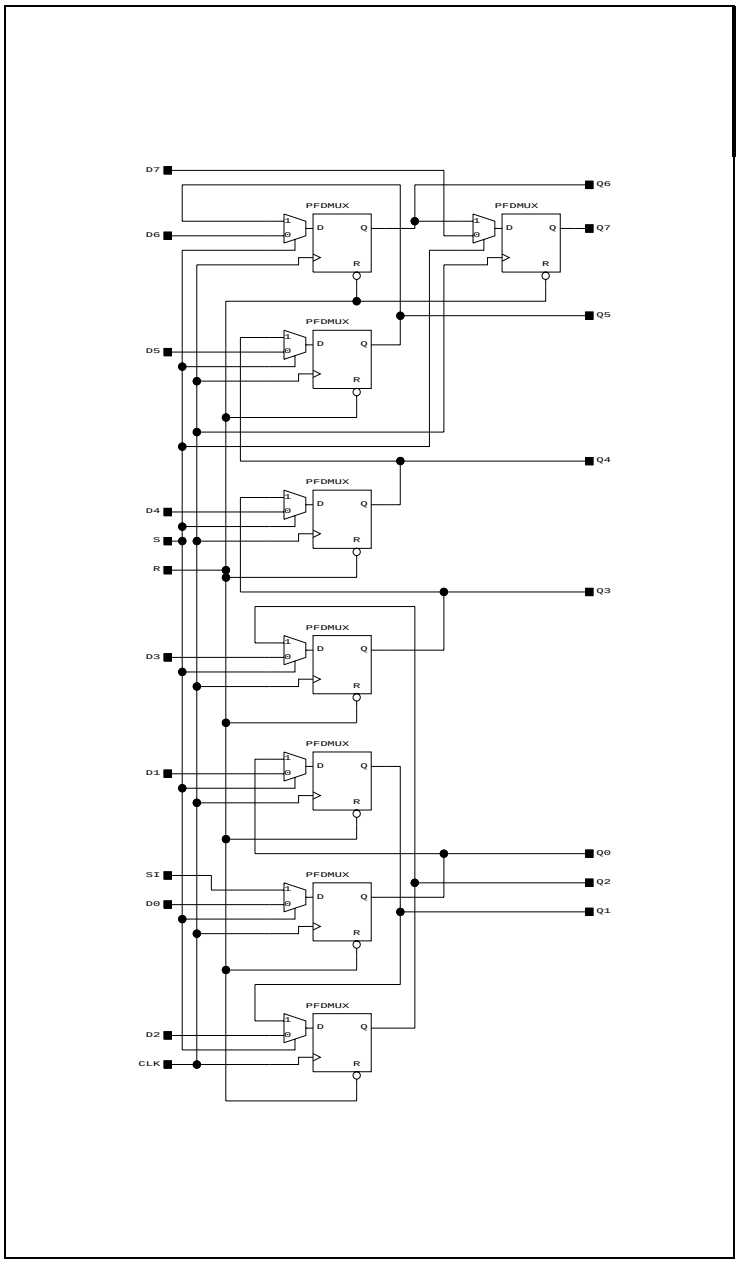
	Setup			Hold		
Pin	Min	Typ	Max	Min	Typ	Max
S	3.80	4.00	4.30	0.00	0.00	0.00
D7	3.90	4.10	4.30	0.00	0.00	0.00
D6	3.90	4.10	4.30	0.00	0.00	0.00
D5	3.90	4.10	4.30	0.00	0.00	0.00
D4	3.90	4.10	4.30	0.00	0.00	0.00
D3	3.90	4.10	4.30	0.00	0.00	0.00
D2	3.90	4.10	4.30	0.00	0.00	0.00
D1	3.90	4.10	4.30	0.00	0.00	0.00
D0	3.90	4.10	4.30	0.00	0.00	0.00
SI	3.90	4.10	4.30	0.00	0.00	0.00

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q7	-	-	-	2.40	2.70	3.00
CLK → Q7	2.40	2.70	3.00	3.00	3.30	3.60
R → Q6	-	-	-	2.48	2.81	3.15
CLK → Q6	2.47	2.79	3.12	3.08	3.41	3.75
R → Q5	-	-	-	2.48	2.81	3.15
CLK → Q5	2.47	2.79	3.12	3.08	3.41	3.75
R → Q4	-	-	-	2.48	2.81	3.15
CLK → Q4	2.47	2.79	3.12	3.08	3.41	3.75
R → Q3	-	-	-	2.48	2.81	3.15
CLK → Q3	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

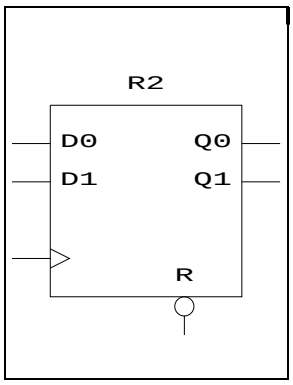
	Setup			Hold		
Pin	Min	Typ	Max	Min	Typ	Max
S	6.10	6.40	6.70	0.00	0.00	0.00
D7	6.30	6.60	6.90	0.00	0.00	0.00
D6	6.30	6.60	6.90	0.00	0.00	0.00
D5	6.30	6.60	6.90	0.00	0.00	0.00
D4	6.30	6.60	6.90	0.00	0.00	0.00
D3	6.30	6.60	6.90	0.00	0.00	0.00
D2	6.30	6.60	6.90	0.00	0.00	0.00
D1	6.30	6.60	6.90	0.00	0.00	0.00
D0	6.30	6.60	6.90	0.00	0.00	0.00
SI	6.30	6.60	6.90	0.00	0.00	0.00

Schematic


D7
D6
D5
D4
S
R
D3
D1
SI
D0
D2
CLK
PFDMUX
D
Q
R
1
0
Q6
Q7
Q5
Q4
Q3
Q0
Q2
Q1

R2 - 2-Bit Register File

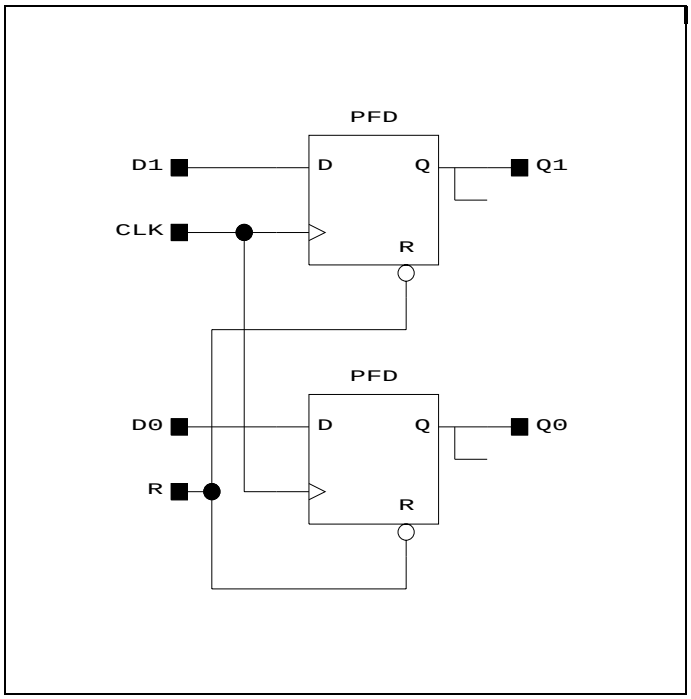
Symbol



Rectangular Area: 1x2cells

Number of Cells: 2

Schematic



Truth Table

Input				Output	
R	CLK	D1	D0	Q1	Q0
0	x	x	x	0	0
1	r	d1	d0	d1	d0

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.40	1.60	1.80
CLK → Q1	1.40	1.60	1.80	1.80	2.00	2.20
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.40	1.60	1.80
CLK → Q0	1.40	1.60	1.80	1.80	2.00	2.20

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D1	2.10	2.10	2.10	0.00	0.00	0.00
D0	2.10	2.10	2.10	0.00	0.00	0.00

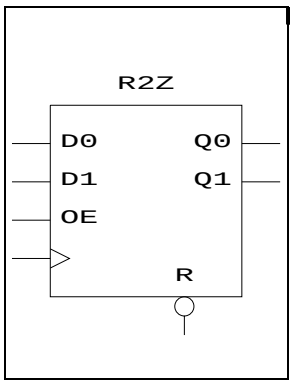
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.40	2.70	3.00
CLK → Q1	2.40	2.70	3.00	3.00	3.30	3.60
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.40	2.70	3.00
CLK → Q0	2.40	2.70	3.00	3.00	3.30	3.60

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D1	3.50	3.50	3.50	0.00	0.00	0.00
D0	3.50	3.50	3.50	0.00	0.00	0.00

R2Z - 2-Bit Register File with Tristate Out

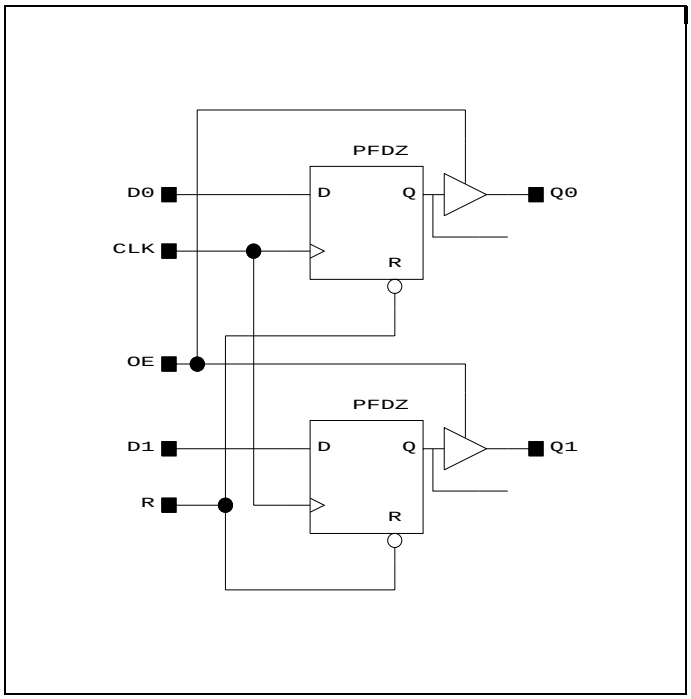
Symbol



Rectangular Area: 1x2cells

Number of Cells: 2

Schematic



Truth Table

Input					Output	
R	CLK	OE	D1	D0	Q1	Q0
0	x	x	x	x	0	0
1	r	0	x	x	z	z
1	r	1	d1	d0	d1	d0

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q0	1.40	1.51	1.68	1.34	1.47	1.63
R → Q0	-	-	-	2.04	2.37	2.73
CLK → Q0	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q1	1.40	1.51	1.68	1.34	1.47	1.63
R → Q1	-	-	-	2.04	2.37	2.73
CLK → Q1	2.10	2.41	2.78	2.44	2.77	3.13

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D1	2.10	2.10	2.10	0.00	0.00	0.00
D0	2.10	2.10	2.10	0.00	0.00	0.00

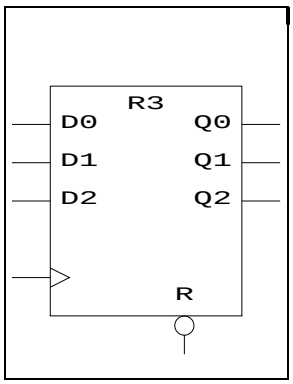
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q0	2.07	2.31	2.60	2.02	2.27	2.57
R → Q0	-	-	-	3.52	3.97	4.47
CLK → Q0	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q1	2.07	2.31	2.60	2.02	2.27	2.57
R → Q1	-	-	-	3.52	3.97	4.47
CLK → Q1	3.67	4.11	4.60	4.12	4.57	5.07

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D1	3.70	3.70	3.70	0.00	0.00	0.00
D0	3.70	3.70	3.70	0.00	0.00	0.00

R3 - 2-Bit Register File

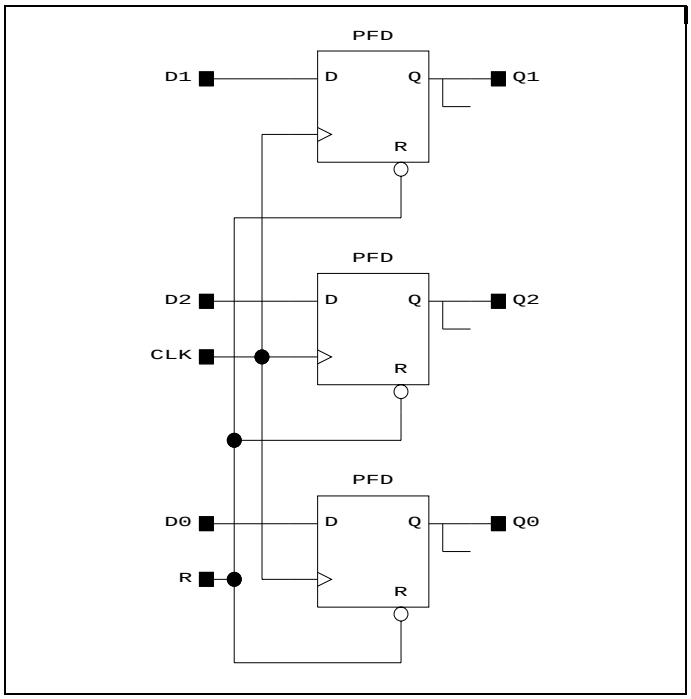
Symbol



Rectangular Area: 1x3cells

Number of Cells: 3

Schematic



Truth Table

Input					Output		
R	**CLK**	**D2**	**D1**	**D0**	**Q2**	**Q1**	**Q0**
0	x	x	x	x	0	0	0
1	r	d2	d1	d0	d2	d1	d0

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.40	1.60	1.80
CLK → Q2	1.40	1.60	1.80	1.80	2.00	2.20
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.40	1.60	1.80
CLK → Q1	1.40	1.60	1.80	1.80	2.00	2.20
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.40	1.60	1.80
CLK → Q0	1.40	1.60	1.80	1.80	2.00	2.20

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D2	2.10	2.10	2.10	0.00	0.00	0.00
D1	2.10	2.10	2.10	0.00	0.00	0.00
D0	2.10	2.10	2.10	0.00	0.00	0.00

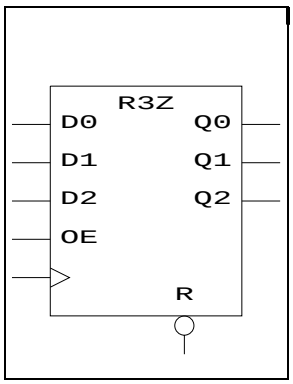
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.40	2.70	3.00
CLK → Q2	2.40	2.70	3.00	3.00	3.30	3.60
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.40	2.70	3.00
CLK → Q1	2.40	2.70	3.00	3.00	3.30	3.60
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.40	2.70	3.00
CLK → Q0	2.40	2.70	3.00	3.00	3.30	3.60

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D2	3.50	3.50	3.50	0.00	0.00	0.00
D1	3.50	3.50	3.50	0.00	0.00	0.00
D0	3.50	3.50	3.50	0.00	0.00	0.00

R3Z - 3-Bit Register File with Tristate Out

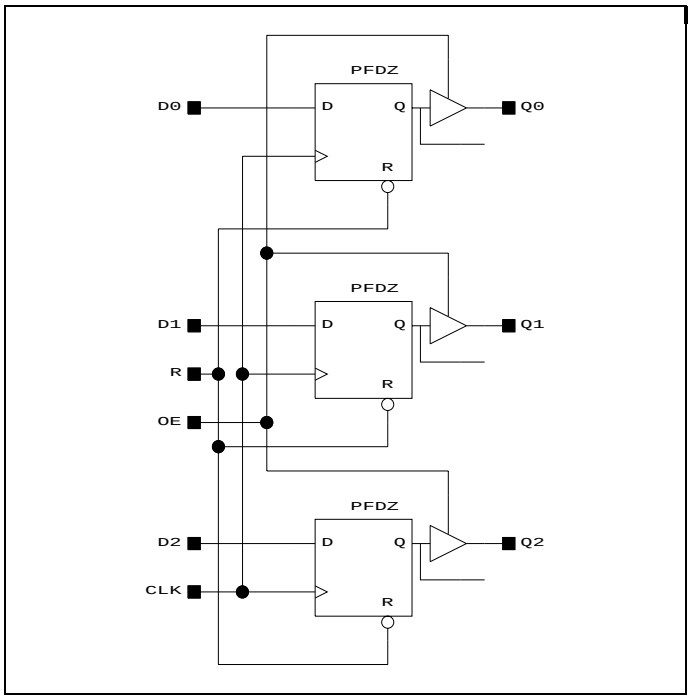
Symbol



Rectangular Area: 1x3cells

Number of Cells: 3

Schematic



Truth Table

Input						Output		
R	OE	CLK	D2	D1	D0	Q2	Q1	Q0
0	x	x	x	x	x	0	0	0
1	0	r	x	x	x	z	z	z
1	r	r	d2	d1	d0	d2	d1	d0

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q2	1.40	1.51	1.68	1.34	1.47	1.63
R → Q2	-	-	-	2.04	2.37	2.73
CLK → Q2	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q1	1.40	1.51	1.68	1.34	1.47	1.63
R → Q1	-	-	-	2.04	2.37	2.73
CLK → Q1	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q0	1.40	1.51	1.68	1.34	1.47	1.63
R → Q0	-	-	-	2.04	2.37	2.73
CLK → Q0	2.10	2.41	2.78	2.44	2.77	3.13

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D2	2.10	2.10	2.10	0.00	0.00	0.00
D1	2.10	2.10	2.10	0.00	0.00	0.00
D0	2.10	2.10	2.10	0.00	0.00	0.00

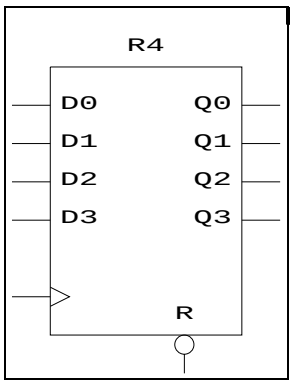
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q2	2.07	2.31	2.60	2.02	2.27	2.57
R → Q2	-	-	-	3.52	3.97	4.47
CLK → Q2	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q1	2.07	2.31	2.60	2.02	2.27	2.57
R → Q1	-	-	-	3.52	3.97	4.47
CLK → Q1	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q0	2.07	2.31	2.60	2.02	2.27	2.57
R → Q0	-	-	-	3.52	3.97	4.47
CLK → Q0	3.67	4.11	4.60	4.12	4.57	5.07

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D2	3.70	3.70	3.70	0.00	0.00	0.00
D1	3.70	3.70	3.70	0.00	0.00	0.00
D0	3.70	3.70	3.70	0.00	0.00	0.00

R4 - 4-Bit Register File

Symbol



Rectangular Area: 1x4cells

Number of Cells: 4

Truth Table

Input						Output			
R	**CLK**	**D3**	**D2**	**D1**	**D0**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	x	x	x	x	0	0	0	0
1	r	d3	d2	d1	d0	d3	d2	d1	d0

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.40	1.60	1.80
CLK → Q0	1.40	1.60	1.80	1.80	2.00	2.20
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.40	1.60	1.80
CLK → Q1	1.40	1.60	1.80	1.80	2.00	2.20
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.40	1.60	1.80
CLK → Q2	1.40	1.60	1.80	1.80	2.00	2.20
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.40	1.60	1.80
CLK → Q3	1.40	1.60	1.80	1.80	2.00	2.20

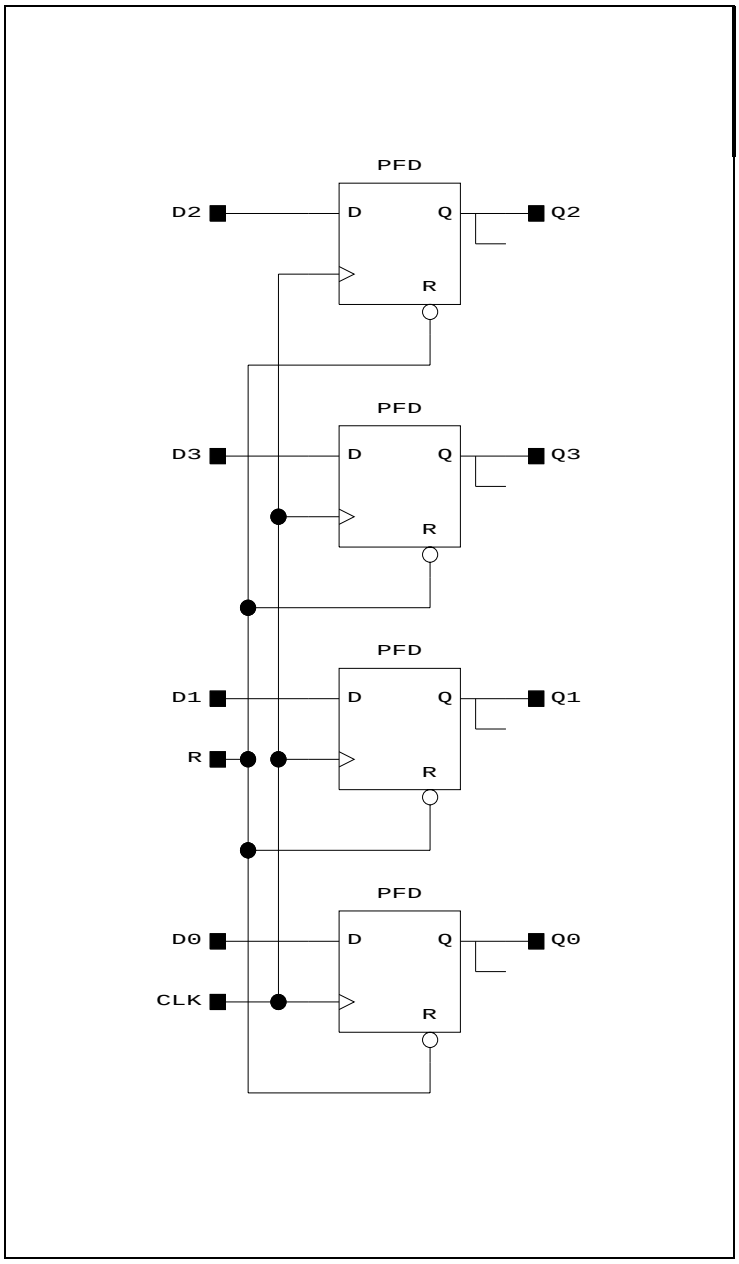
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D0	2.10	2.10	2.10	0.00	0.00	0.00
D1	2.10	2.10	2.10	0.00	0.00	0.00
D2	2.10	2.10	2.10	0.00	0.00	0.00
D3	2.10	2.10	2.10	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.40	2.70	3.00
CLK → Q0	2.40	2.70	3.00	3.00	3.30	3.60
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.40	2.70	3.00
CLK → Q1	2.40	2.70	3.00	3.00	3.30	3.60
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.40	2.70	3.00
CLK → Q2	2.40	2.70	3.00	3.00	3.30	3.60
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.40	2.70	3.00
CLK → Q3	2.40	2.70	3.00	3.00	3.30	3.60

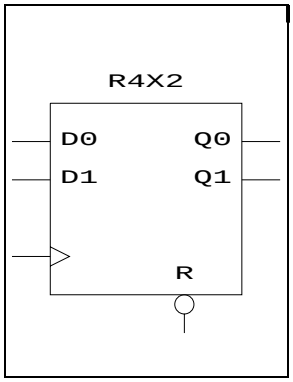
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D0	3.50	3.50	3.50	0.00	0.00	0.00
D1	3.50	3.50	3.50	0.00	0.00	0.00
D2	3.50	3.50	3.50	0.00	0.00	0.00
D3	3.50	3.50	3.50	0.00	0.00	0.00

Schematic



R4X2 - 4 Word x 2 Bit Register File

Symbol



Rectangular Area: 4x2cells

Number of Cells: 8

Truth Table

Input				Output	
R	**CLK**	**D1**	**D0**	**Q1**	**Q0**
0	x	x	x	0	0
1	r1	d1a	d0a	x	x
1	r2	d1b	d0b	x	x
1	r3	d1c	d0c	x	x
1	r4	d1d	d0d	d1a	d0a
1	r5	d1e	d0e	d1b	d0b

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.40	1.60	1.80
CLK → Q0	1.40	1.60	1.80	1.80	2.00	2.20
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.40	1.60	1.80
CLK → Q1	1.40	1.60	1.80	1.80	2.00	2.20

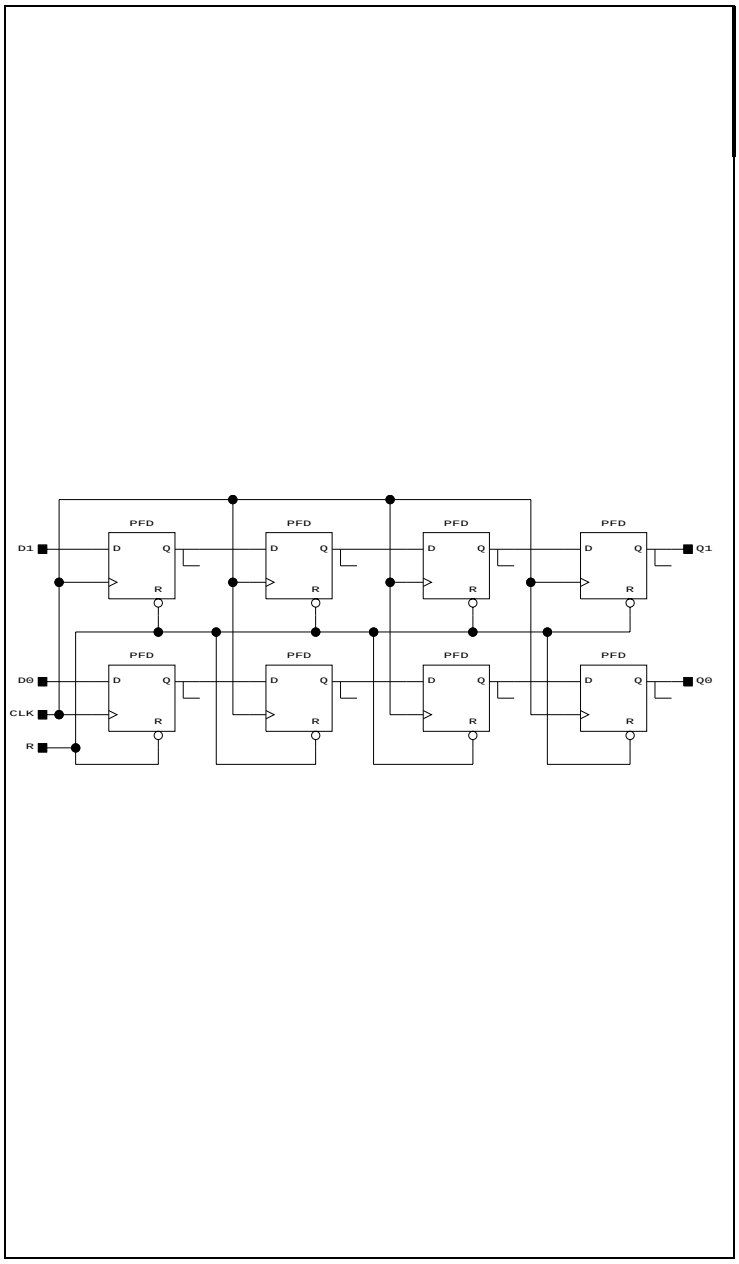
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D0	2.10	2.10	2.10	0.00	0.00	0.00
D1	2.10	2.10	2.10	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.40	2.70	3.00
CLK → Q0	2.40	2.70	3.00	3.00	3.30	3.60
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.40	2.70	3.00
CLK → Q1	2.40	2.70	3.00	3.00	3.30	3.60

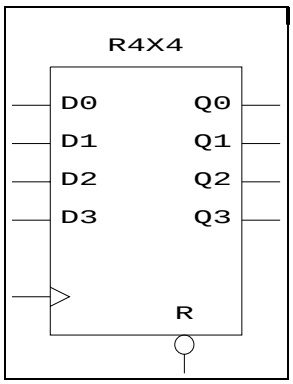
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D0	3.50	3.50	3.50	0.00	0.00	0.00
D1	3.50	3.50	3.50	0.00	0.00	0.00

Schematic



R4X4 - 4 Word x 4 Bit Register File

Symbol



Rectangular Area: 4x4cells

Number of Cells: 16

Truth Table

Input						Output			
R	**CLK**	**D3**	**D2**	**D1**	**D0**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	x	x	x	x	0	0	0	0
1	r1	d3a	d2a	d1a	d0a	x	x	x	x
1	r2	d3b	d2b	d1b	d0b	x	x	x	x
1	r3	d3c	d2c	d1c	d0c	x	x	x	x
1	r4	d3d	d2d	d1d	d0d	d3a	d2a	d1a	d0a
1	r5	d3e	d2e	d1e	d0e	d3b	d2b	d1b	d0b

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.40	1.60	1.80
CLK → Q0	1.40	1.60	1.80	1.80	2.00	2.20
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.40	1.60	1.80
CLK → Q1	1.40	1.60	1.80	1.80	2.00	2.20
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.40	1.60	1.80
CLK → Q2	1.40	1.60	1.80	1.80	2.00	2.20
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.40	1.60	1.80
CLK → Q3	1.40	1.60	1.80	1.80	2.00	2.20

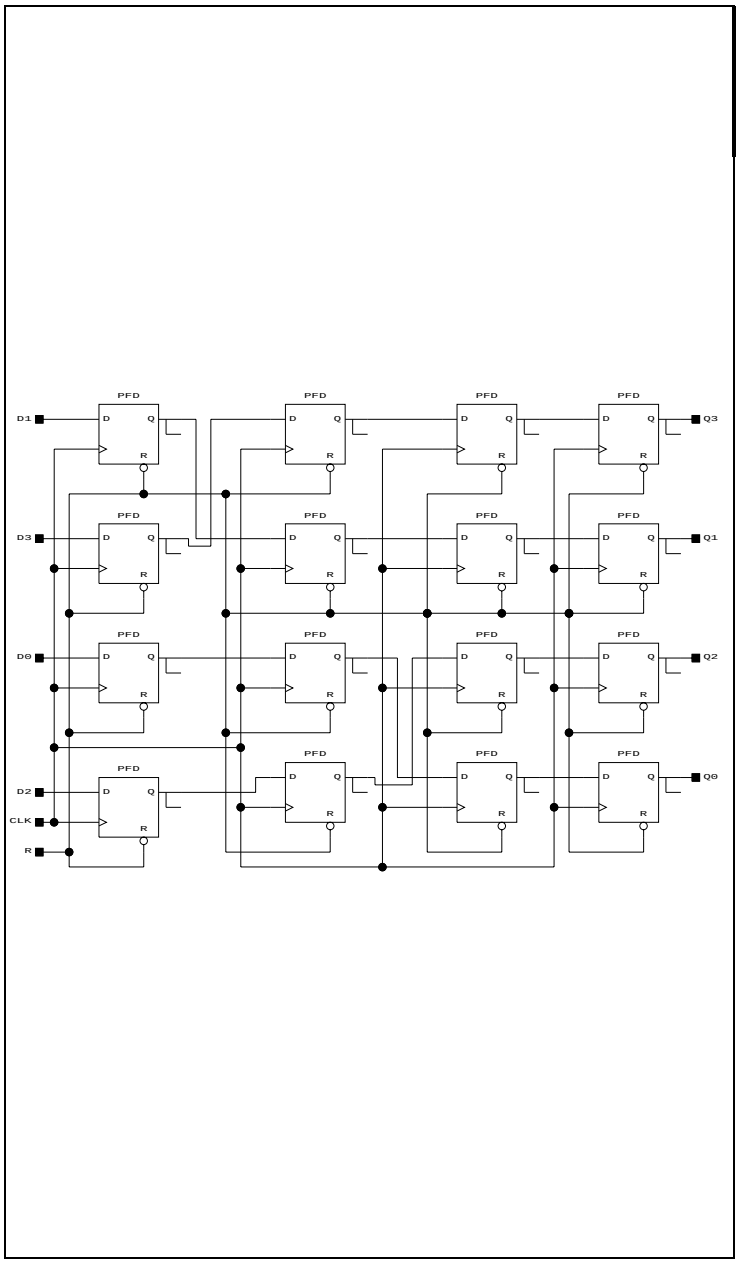
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D0	2.10	2.10	2.10	0.00	0.00	0.00
D1	2.10	2.10	2.10	0.00	0.00	0.00
D2	2.10	2.10	2.10	0.00	0.00	0.00
D3	2.10	2.10	2.10	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.40	2.70	3.00
CLK → Q0	2.40	2.70	3.00	3.00	3.30	3.60
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.40	2.70	3.00
CLK → Q1	2.40	2.70	3.00	3.00	3.30	3.60
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.40	2.70	3.00
CLK → Q2	2.40	2.70	3.00	3.00	3.30	3.60
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.40	2.70	3.00
CLK → Q3	2.40	2.70	3.00	3.00	3.30	3.60

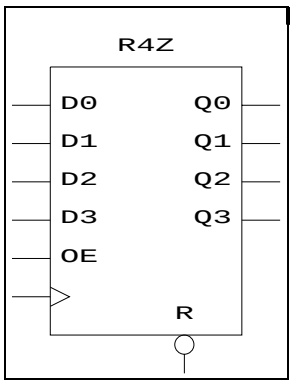
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D0	3.50	3.50	3.50	0.00	0.00	0.00
D1	3.50	3.50	3.50	0.00	0.00	0.00
D2	3.50	3.50	3.50	0.00	0.00	0.00
D3	3.50	3.50	3.50	0.00	0.00	0.00

Schematic



R4Z - 4 Bit Register File with Tristate Out

Symbol



Rectangular Area: 1x4cells

Number of Cells: 4

Truth Table

Input							Output			
R	**CLK**	**OE**	**D3**	**D2**	**D1**	**D0**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	x	x	x	x	x	0	0	0	0
1	r	0	x	x	x	x	z	z	z	z
1	r1	1	d3	d2	d1	d0	d3	d2	d1	d0

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q3	1.40	1.51	1.68	1.34	1.47	1.63
R → Q3	-	-	-	2.04	2.37	2.73
CLK → Q3	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q2	1.40	1.51	1.68	1.34	1.47	1.63
R → Q2	-	-	-	2.04	2.37	2.73
CLK → Q2	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q1	1.40	1.51	1.68	1.34	1.47	1.63
R → Q1	-	-	-	2.04	2.37	2.73
CLK → Q1	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q0	1.40	1.51	1.68	1.34	1.47	1.63
R → Q0	-	-	-	2.04	2.37	2.73
CLK → Q0	2.10	2.41	2.78	2.44	2.77	3.13

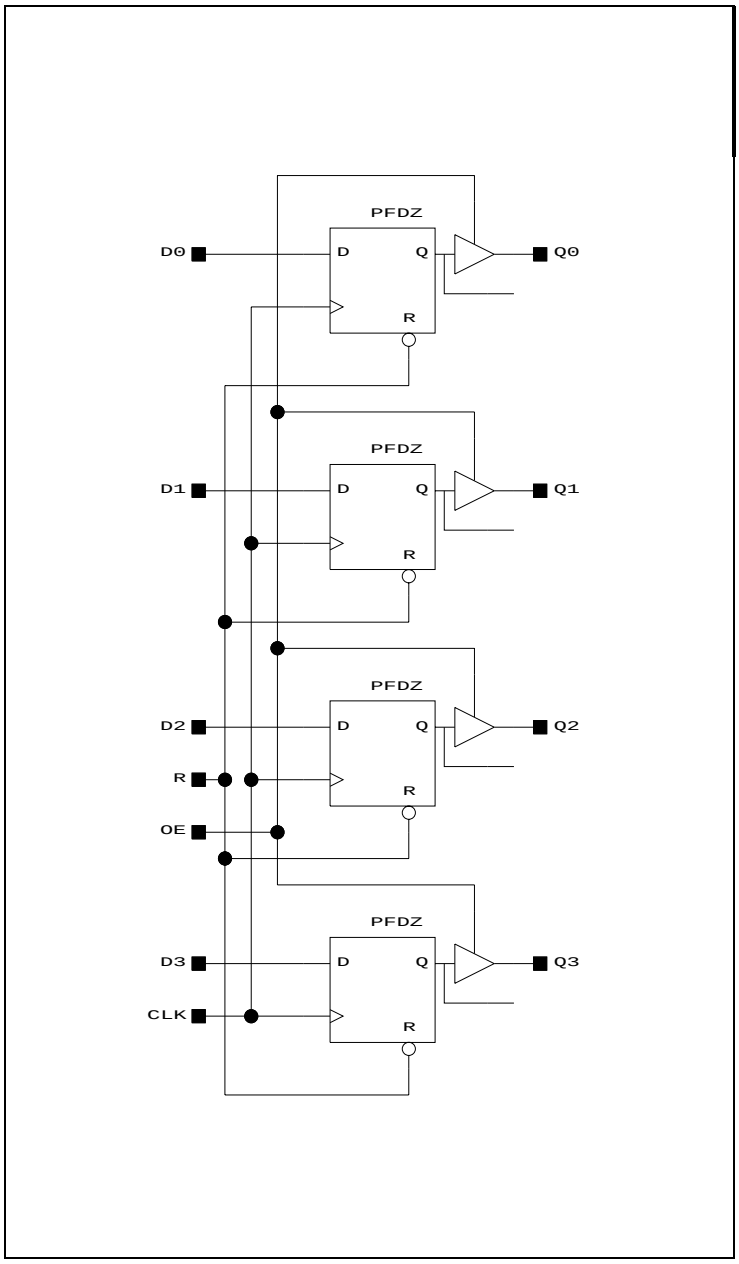
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D3	2.10	2.10	2.10	0.00	0.00	0.00
D2	2.10	2.10	2.10	0.00	0.00	0.00
D1	2.10	2.10	2.10	0.00	0.00	0.00
D0	2.10	2.10	2.10	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q3	2.07	2.31	2.60	2.02	2.27	2.57
R → Q3	-	-	-	3.52	3.97	4.47
CLK → Q3	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q2	2.07	2.31	2.60	2.02	2.27	2.57
R → Q2	-	-	-	3.52	3.97	4.47
CLK → Q2	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q1	2.07	2.31	2.60	2.02	2.27	2.57
R → Q1	-	-	-	3.52	3.97	4.47
CLK → Q1	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q0	2.07	2.31	2.60	2.02	2.27	2.57
R → Q0	-	-	-	3.52	3.97	4.47
CLK → Q0	3.67	4.11	4.60	4.12	4.57	5.07

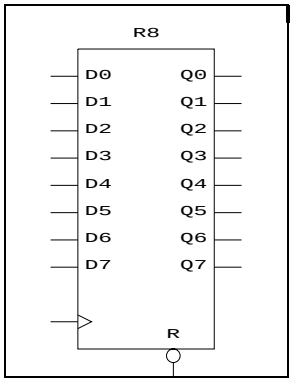
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D3	3.70	3.70	3.70	0.00	0.00	0.00
D2	3.70	3.70	3.70	0.00	0.00	0.00
D1	3.70	3.70	3.70	0.00	0.00	0.00
D0	3.70	3.70	3.70	0.00	0.00	0.00

Schematic


PFDZ
D0
D
Q
Q0
R
PFDZ
D1
D
Q
Q1
R
PFDZ
D2
D
Q
Q2
R
R
OE
PFDZ
D3
D
Q
Q3
CLK
R

R8 - 8-Bit Register File

Symbol



Rectangular Area: 1x8cells

Number of Cells: 8

Truth Table

Input			Output
R	**CLK**	**D7...D0**	**Q7...Q0**
0	x	x...x	0...0
1	r	d7...d0	d7...d0

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q7.BUS	-	-	-	1.90	2.20	2.50
CLK → Q7.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q7	-	-	-	1.40	1.60	1.80
CLK → Q7	1.40	1.60	1.80	1.80	2.00	2.20
R → Q6.BUS	-	-	-	1.90	2.20	2.50
CLK → Q6.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q6	-	-	-	1.40	1.60	1.80
CLK → Q6	1.40	1.60	1.80	1.80	2.00	2.20
R → Q5.BUS	-	-	-	1.90	2.20	2.50
CLK → Q5.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q5	-	-	-	1.40	1.60	1.80
CLK → Q5	1.40	1.60	1.80	1.80	2.00	2.20
R → Q4.BUS	-	-	-	1.90	2.20	2.50
CLK → Q4.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q4	-	-	-	1.40	1.60	1.80
CLK → Q4	1.40	1.60	1.80	1.80	2.00	2.20
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.40	1.60	1.80
CLK → Q3	1.40	1.60	1.80	1.80	2.00	2.20
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.40	1.60	1.80
CLK → Q2	1.40	1.60	1.80	1.80	2.00	2.20
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.40	1.60	1.80
CLK → Q1	1.40	1.60	1.80	1.80	2.00	2.20

R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.40	1.60	1.80
CLK → Q0	1.40	1.60	1.80	1.80	2.00	2.20

	Setup			Hold		
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D7	2.10	2.10	2.10	0.00	0.00	0.00
D6	2.10	2.10	2.10	0.00	0.00	0.00
D5	2.10	2.10	2.10	0.00	0.00	0.00
D4	2.10	2.10	2.10	0.00	0.00	0.00
D3	2.10	2.10	2.10	0.00	0.00	0.00
D2	2.10	2.10	2.10	0.00	0.00	0.00
D1	2.10	2.10	2.10	0.00	0.00	0.00
D0	2.10	2.10	2.10	0.00	0.00	0.00

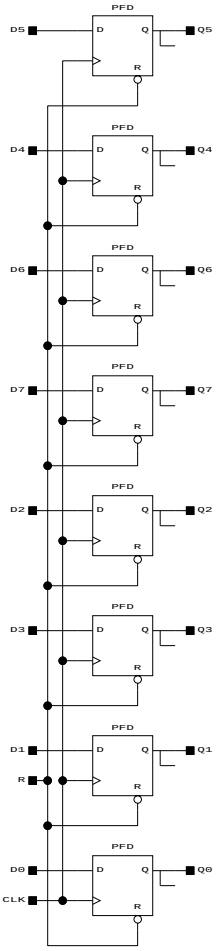
Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q7.BUS	-	-	-	3.40	3.90	4.80
CLK → Q7.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q7	-	-	-	2.40	2.70	3.00
CLK → Q7	2.40	2.70	3.00	3.00	3.30	3.60
R → Q6.BUS	-	-	-	3.40	3.90	4.80
CLK → Q6.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q6	-	-	-	2.40	2.70	3.00
CLK → Q6	2.40	2.70	3.00	3.00	3.30	3.60
R → Q5.BUS	-	-	-	3.40	3.90	4.80
CLK → Q5.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q5	-	-	-	2.40	2.70	3.00
CLK → Q5	2.40	2.70	3.00	3.00	3.30	3.60
R → Q4.BUS	-	-	-	3.40	3.90	4.80
CLK → Q4.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q4	-	-	-	2.40	2.70	3.00
CLK → Q4	2.40	2.70	3.00	3.00	3.30	3.60
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.40	2.70	3.00
CLK → Q3	2.40	2.70	3.00	3.00	3.30	3.60
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.40	2.70	3.00
CLK → Q2	2.40	2.70	3.00	3.00	3.30	3.60
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.40	2.70	3.00
CLK → Q1	2.40	2.70	3.00	3.00	3.30	3.60

R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.40	2.70	3.00
CLK → Q0	2.40	2.70	3.00	3.00	3.30	3.60

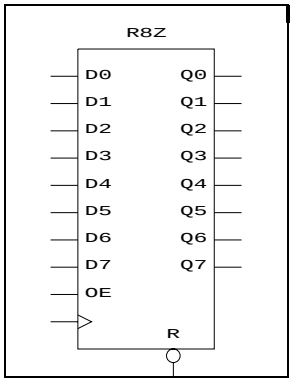
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D7	3.50	3.50	3.50	0.00	0.00	0.00
D6	3.50	3.50	3.50	0.00	0.00	0.00
D5	3.50	3.50	3.50	0.00	0.00	0.00
D4	3.50	3.50	3.50	0.00	0.00	0.00
D3	3.50	3.50	3.50	0.00	0.00	0.00
D2	3.50	3.50	3.50	0.00	0.00	0.00
D1	3.50	3.50	3.50	0.00	0.00	0.00
D0	3.50	3.50	3.50	0.00	0.00	0.00

Schematic


PFD
D5
Q
Q5
R
PFD
D4
Q
Q4
R
PFD
D6
Q
Q6
R
PFD
D7
Q
Q7
R
PFD
D2
Q
Q2
R
PFD
D3
Q
Q3
R
PFD
D1
R
Q
Q1
R
PFD
D0
CLK
Q
Q0
R

R8Z - 8 Bit Register File with Tristate Out

Symbol



Rectangular Area: 1x8cells

Number of Cells: 8

Truth Table

Input				Output
R	**OE**	**CLK**	**D7...D0**	**Q7...Q0**
0	x	x	x...x	0
1	0	x	x...x	z...z
1	1	r	d7...d0	d7...d0

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q7	1.40	1.51	1.68	1.34	1.47	1.63
R → Q7	-	-	-	2.04	2.37	2.73
CLK → Q7	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q6	1.40	1.51	1.68	1.34	1.47	1.63
R → Q6	-	-	-	2.04	2.37	2.73
CLK → Q6	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q5	1.40	1.51	1.68	1.34	1.47	1.63
R → Q5	-	-	-	2.04	2.37	2.73
CLK → Q5	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q4	1.40	1.51	1.68	1.34	1.47	1.63
R → Q4	-	-	-	2.04	2.37	2.73
CLK → Q4	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q3	1.40	1.51	1.68	1.34	1.47	1.63
R → Q3	-	-	-	2.04	2.37	2.73
CLK → Q3	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q2	1.40	1.51	1.68	1.34	1.47	1.63
R → Q2	-	-	-	2.04	2.37	2.73
CLK → Q2	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q1	1.40	1.51	1.68	1.34	1.47	1.63
R → Q1	-	-	-	2.04	2.37	2.73
CLK → Q1	2.10	2.41	2.78	2.44	2.77	3.13
OE → Q0	1.40	1.51	1.68	1.34	1.47	1.63
R → Q0	-	-	-	2.04	2.37	2.73
CLK → Q0	2.10	2.41	2.78	2.44	2.77	3.13

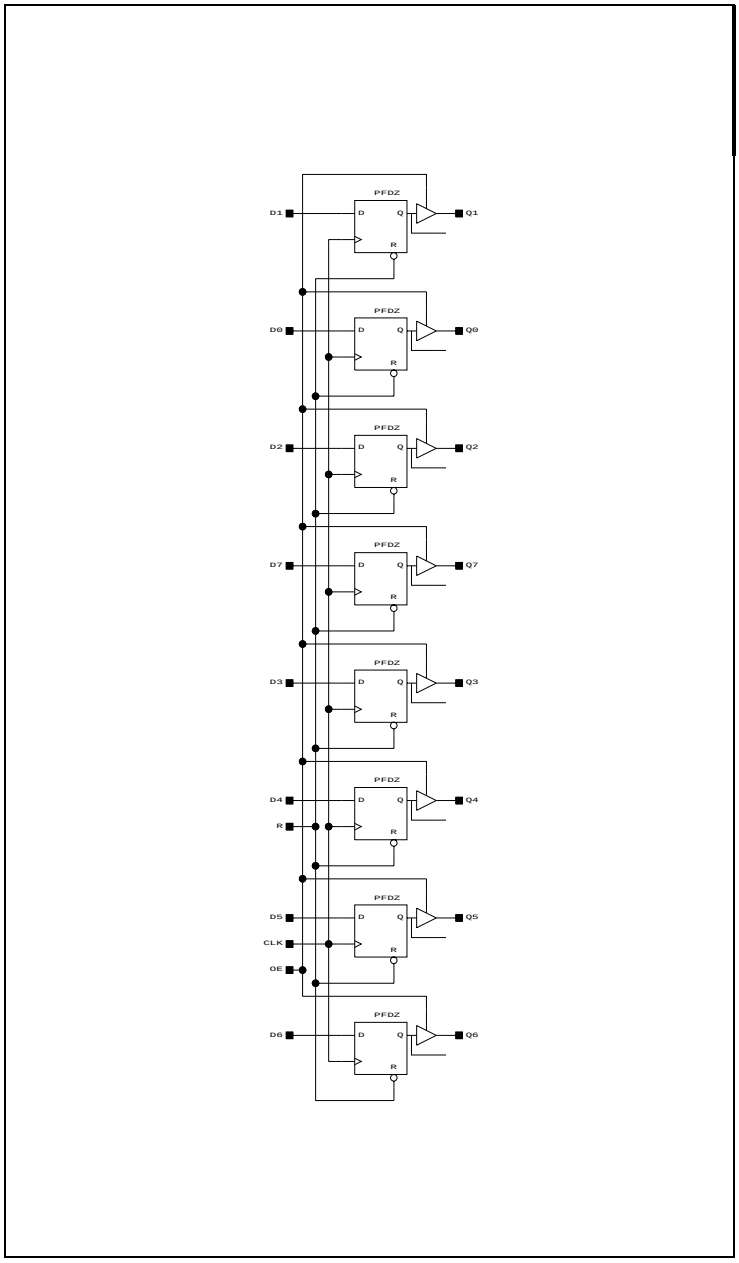
Pin	Setup			Hold		
	Min	Typ	Max	Min	Typ	Max
D7	2.10	2.10	2.10	0.00	0.00	0.00
D6	2.10	2.10	2.10	0.00	0.00	0.00
D5	2.10	2.10	2.10	0.00	0.00	0.00
D4	2.10	2.10	2.10	0.00	0.00	0.00
D3	2.10	2.10	2.10	0.00	0.00	0.00
D2	2.10	2.10	2.10	0.00	0.00	0.00
D1	2.10	2.10	2.10	0.00	0.00	0.00
D0	2.10	2.10	2.10	0.00	0.00	0.00

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
OE → Q7	2.07	2.31	2.60	2.02	2.27	2.57
R → Q7	-	-	-	3.52	3.97	4.47
CLK → Q7	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q6	2.07	2.31	2.60	2.02	2.27	2.57
R → Q6	-	-	-	3.52	3.97	4.47
CLK → Q6	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q5	2.07	2.31	2.60	2.02	2.27	2.57
R → Q5	-	-	-	3.52	3.97	4.47
CLK → Q5	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q4	2.07	2.31	2.60	2.02	2.27	2.57
R → Q4	-	-	-	3.52	3.97	4.47
CLK → Q4	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q3	2.07	2.31	2.60	2.02	2.27	2.57
R → Q3	-	-	-	3.52	3.97	4.47
CLK → Q3	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q2	2.07	2.31	2.60	2.02	2.27	2.57
R → Q2	-	-	-	3.52	3.97	4.47
CLK → Q2	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q1	2.07	2.31	2.60	2.02	2.27	2.57
R → Q1	-	-	-	3.52	3.97	4.47
CLK → Q1	3.67	4.11	4.60	4.12	4.57	5.07
OE → Q0	2.07	2.31	2.60	2.02	2.27	2.57
R → Q0	-	-	-	3.52	3.97	4.47
CLK → Q0	3.67	4.11	4.60	4.12	4.57	5.07

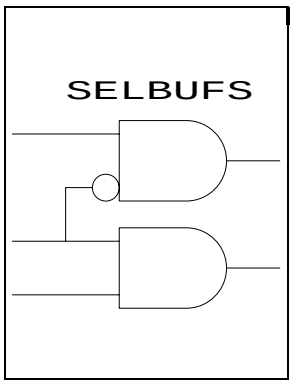
	Setup			Hold		
Pin	Min	Typ	Max	Min	Typ	Max
D7	3.70	3.70	3.70	0.00	0.00	0.00
D6	3.70	3.70	3.70	0.00	0.00	0.00
D5	3.70	3.70	3.70	0.00	0.00	0.00
D4	3.70	3.70	3.70	0.00	0.00	0.00
D3	3.70	3.70	3.70	0.00	0.00	0.00
D2	3.70	3.70	3.70	0.00	0.00	0.00
D1	3.70	3.70	3.70	0.00	0.00	0.00
D0	3.70	3.70	3.70	0.00	0.00	0.00

Schematic



SELBUFS - Select Buffer

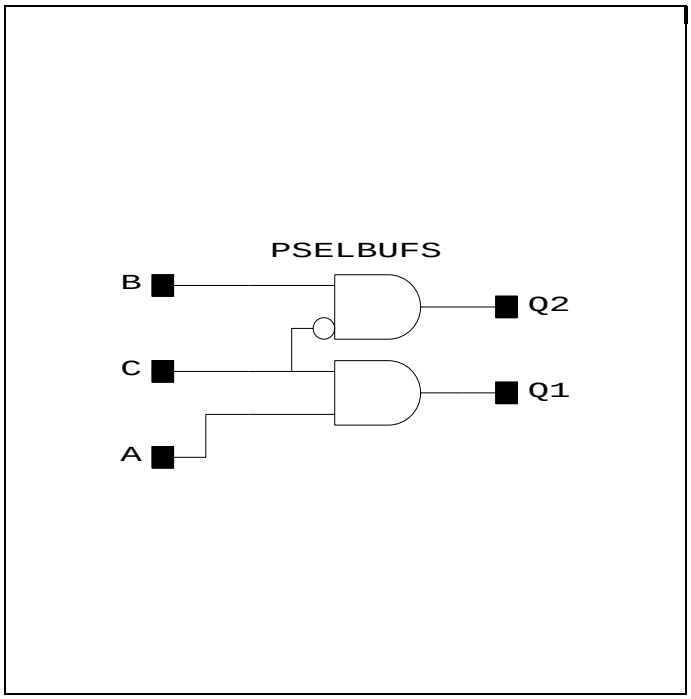
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input			Output	
A	B	C	Q1	Q2
x	b	0	0	b
a	x	1	a	0

Switching Speeds for -2ns Parts

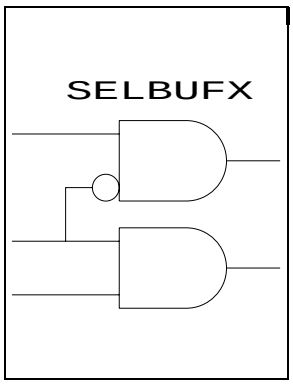
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q1	0.40	0.70	1.10	0.40	0.70	1.10
C → Q1	0.40	0.70	1.10	0.50	0.80	1.20
B → Q2	0.40	0.70	1.10	0.40	0.70	1.10
C → Q2	0.80	1.10	1.50	0.90	1.30	1.80

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q1	1.00	1.30	1.70	1.00	1.20	1.70
C → Q1	1.00	1.30	1.70	1.40	1.60	2.10
B → Q2	1.00	1.20	1.70	0.90	1.20	1.60
C → Q2	1.50	1.80	2.40	1.60	2.00	2.50

SELBUFX - Select Buffer

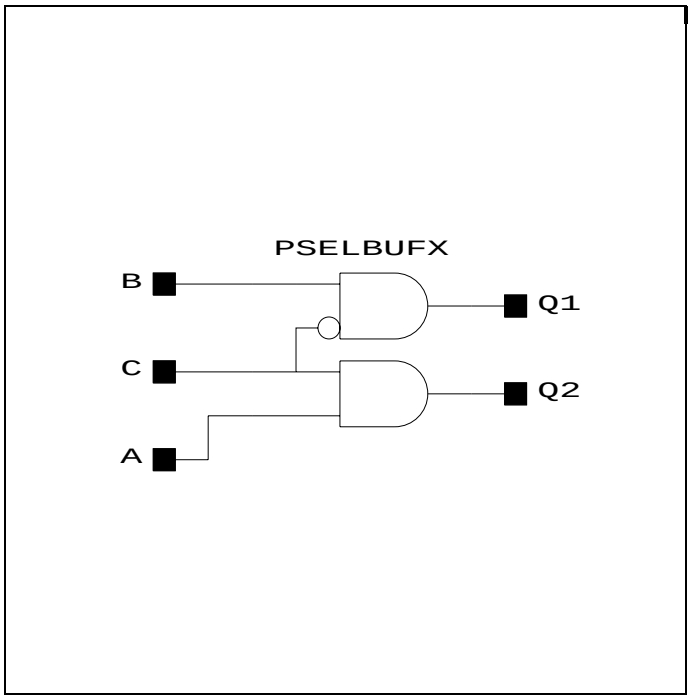
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input			Output	
A	B	C	Q1	Q2
x	b	0	b	0
a	x	1	0	a

Switching Speeds for -2ns Parts

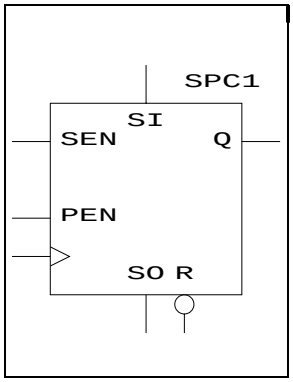
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q2	0.40	0.70	1.10	0.40	0.70	1.10
C → Q2	0.40	0.70	1.10	0.50	0.80	1.20
B → Q1	0.40	0.70	1.10	0.40	0.70	1.10
C → Q1	0.80	1.10	1.50	0.90	1.30	1.80

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q2	1.00	1.30	1.70	1.00	1.20	1.60
C → Q2	1.00	1.30	1.70	1.40	1.60	2.00
B → Q1	1.00	1.30	1.70	1.00	1.20	1.60
C → Q1	1.50	1.90	2.40	1.70	2.00	2.50

SPC1 - 1-Bit Serial-to-Parallel Converter

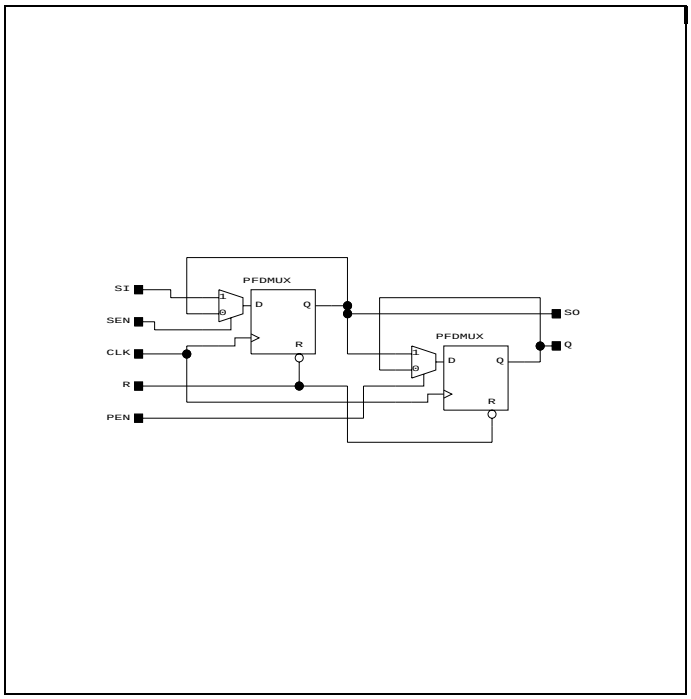
Symbol



Rectangular Area: 2x2 cells

Number of Cells: 4

Schematic



Truth Table

Input					Output	
R	CLK	SEN	PEN	SI	Q	SO
0	x	x	x	x	0	0
1	x	0	0	x	q	so
1	r	1	0	si	q	si
1	r	0	1	x	so	so
1	r	1	1	si	so	si

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q	-	-	-	1.48	1.71	1.93
CLK → Q	1.49	1.71	1.92	1.88	2.11	2.33
R → SO	-	-	-	1.56	1.82	2.06
CLK → SO	1.58	1.81	2.04	1.96	2.22	2.46

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
SI	3.90	4.10	4.30	0.00	0.00	0.00
PEN	3.80	4.00	4.30	0.00	0.00	0.00
SEN	3.80	4.00	4.30	0.00	0.00	0.00

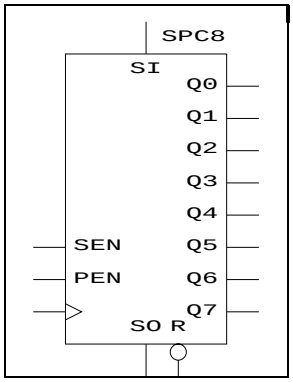
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q	-	-	-	2.48	2.81	3.15
CLK → Q	2.47	2.79	3.12	3.08	3.41	3.75
R → SO	-	-	-	2.56	2.92	3.31
CLK → SO	2.54	2.88	3.24	3.16	3.52	3.91

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
SI	6.30	6.60	6.90	0.00	0.00	0.00
PEN	6.10	6.40	6.70	0.00	0.00	0.00
SEN	6.10	6.40	6.70	0.00	0.00	0.00

SPC8 - 8-Bit Serial-to-Parallel Converter

Symbol



Rectangular Area: 4x8 cells

Number of Cells: 32

Truth Table

Input					Output	
A	**CLK**	**SEN**	**PEN**	**SI**	**Q7...Q0**	**SO**
0	x	x	x	x	0...0	0
1	r	0	0	si	q7...q0	so
1	r	0	1	x	si7...si1	so
1	r1	1	0	si	q7...q0	so
1	r2	1	0	si	q7...q0	si7
1	r3	1	0	si	q7...q0	si6
1	r4	1	0	si	q7...q0	si5
1	r5	1	0	si	q7...q0	si4
1	r6	1	0	si	q7...q0	si3
1	r7	1	0	si	q7...q0	si2
1	r8	1	0	si	q7...q0	si1
1	r1	1	1	si	q6...q0si7	si7
1	r2	1	1	si	q5...si6	si6
1	r3	1	1	si	q4...si5	si5
1	r4	1	1	si	q3...si4	si4
1	r5	1	1	si	q2...si3	si3
1	r6	1	1	si	q1...si2	si2
1	r7	1	1	si	q1...si1	si1

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q3	-	-	-	1.48	1.71	1.93
CLK → Q3	1.49	1.71	1.92	1.88	2.11	2.33
R → Q4	-	-	-	1.48	1.71	1.93
CLK → Q4	1.49	1.71	1.92	1.88	2.11	2.33
R → Q5	-	-	-	1.48	1.71	1.93
CLK → Q5	1.49	1.71	1.92	1.88	2.11	2.33
R → Q6	-	-	-	1.48	1.71	1.93
CLK → Q6	1.49	1.71	1.92	1.88	2.11	2.33
R → Q7	-	-	-	1.48	1.71	1.93
CLK → Q7	1.49	1.71	1.92	1.88	2.11	2.33
R → SO	-	-	-	1.56	1.82	2.06
CLK → SO	1.58	1.81	2.04	1.96	2.22	2.46

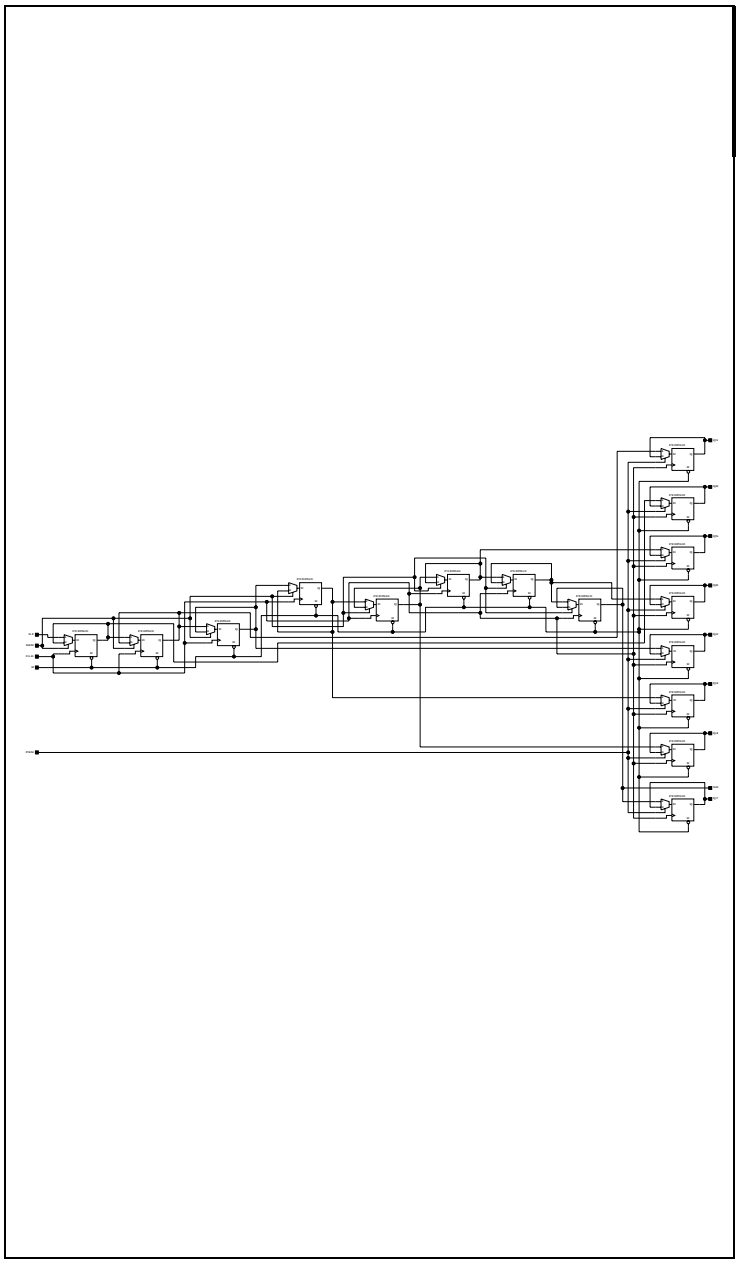
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
SI	3.90	4.10	4.30	0.00	0.00	0.00
PEN	3.80	4.00	4.30	0.00	0.00	0.00
SEN	3.80	4.00	4.30	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q3	-	-	-	2.48	2.81	3.15
CLK → Q3	2.47	2.79	3.12	3.08	3.41	3.75
R → Q4	-	-	-	2.48	2.81	3.15
CLK → Q4	2.47	2.79	3.12	3.08	3.41	3.75
R → Q5	-	-	-	2.48	2.81	3.15
CLK → Q5	2.47	2.79	3.12	3.08	3.41	3.75
R → Q6	-	-	-	2.48	2.81	3.15
CLK → Q6	2.47	2.79	3.12	3.08	3.41	3.75
R → Q7	-	-	-	2.48	2.81	3.15
CLK → Q7	2.47	2.79	3.12	3.08	3.41	3.75
R → SO	-	-	-	2.56	2.92	3.31
CLK → SO	2.54	2.88	3.24	3.16	3.52	3.91

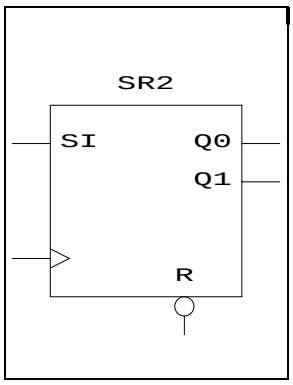
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
SI	6.30	6.60	6.90	0.00	0.00	0.00
PEN	6.10	6.40	6.70	0.00	0.00	0.00
SEN	6.10	6.40	6.70	0.00	0.00	0.00

Schematic



SR2 - 2-Bit Shift Register

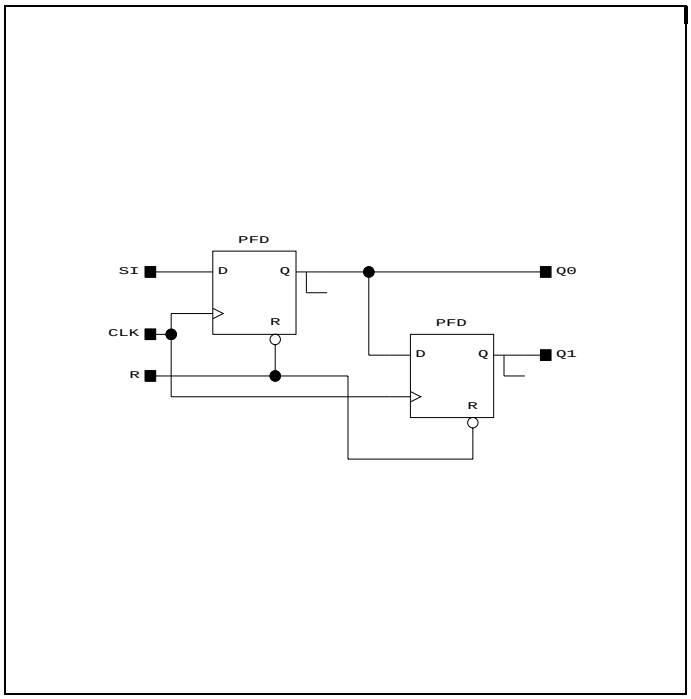
Symbol



Rectangular Area: 1x2 cells

Number of Cells: 2

Schematic



Truth Table

Input			Output	
A	CLK	SI	Q1	Q0
0	x	x	0	0
1	r	si	q0	si

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.40	1.60	1.80
CLK → Q1	1.40	1.60	1.80	1.80	2.00	2.20
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
SI	2.10	2.10	2.10	0.00	0.00	0.00

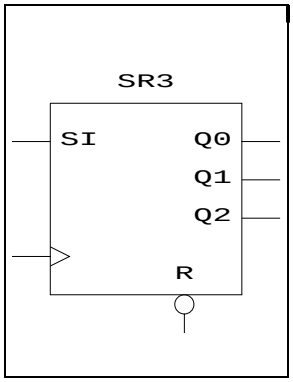
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.40	2.70	3.00
CLK → Q1	2.40	2.70	3.00	3.00	3.30	3.60
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
SI	3.50	3.50	3.50	0.00	0.00	0.00

SR3 - 3-Bit Shift Register

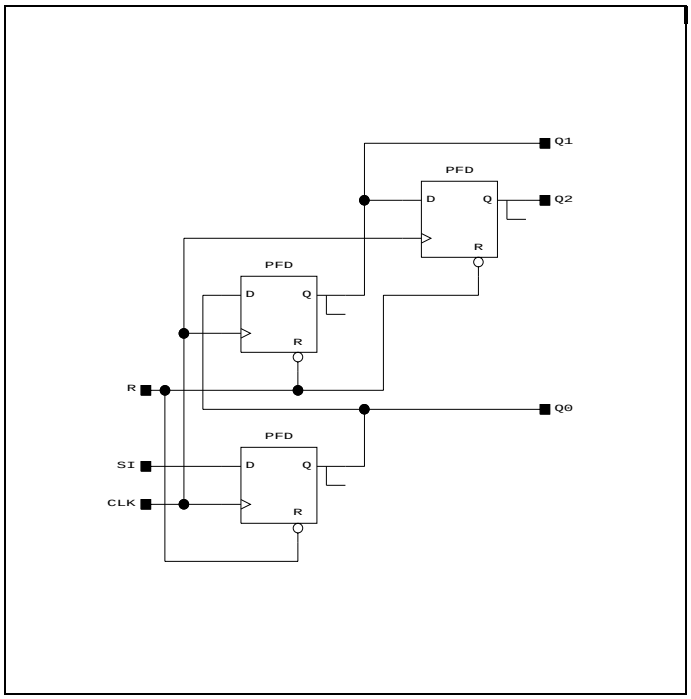
Symbol



Rectangular Area: 1x3 cells

Number of Cells: 3

Schematic



Truth Table

Input			Output		
A	CLK	SI	Q2	Q1	Q0
0	x	x	0	0	0
1	r	si	q1	q0	si

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.40	1.60	1.80
CLK → Q2	1.40	1.60	1.80	1.80	2.00	2.20
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
SI	2.10	2.10	2.10	0.00	0.00	0.00

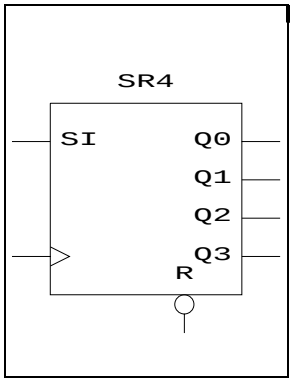
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.40	2.70	3.00
CLK → Q3	2.40	2.70	3.00	3.00	3.30	3.60
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
SI	3.50	3.50	3.50	0.00	0.00	0.00

SR4 - 4-Bit Shift Register

Symbol



Rectangular Area: 1x4 cells

Number of Cells: 4

Truth Table

Input			Output			
A	**CLK**	**SI**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	x	0	0	0	0
1	r	si	q2	q1	q0	si

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.40	1.60	1.80
CLK → Q3	1.40	1.60	1.80	1.80	2.00	2.20
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

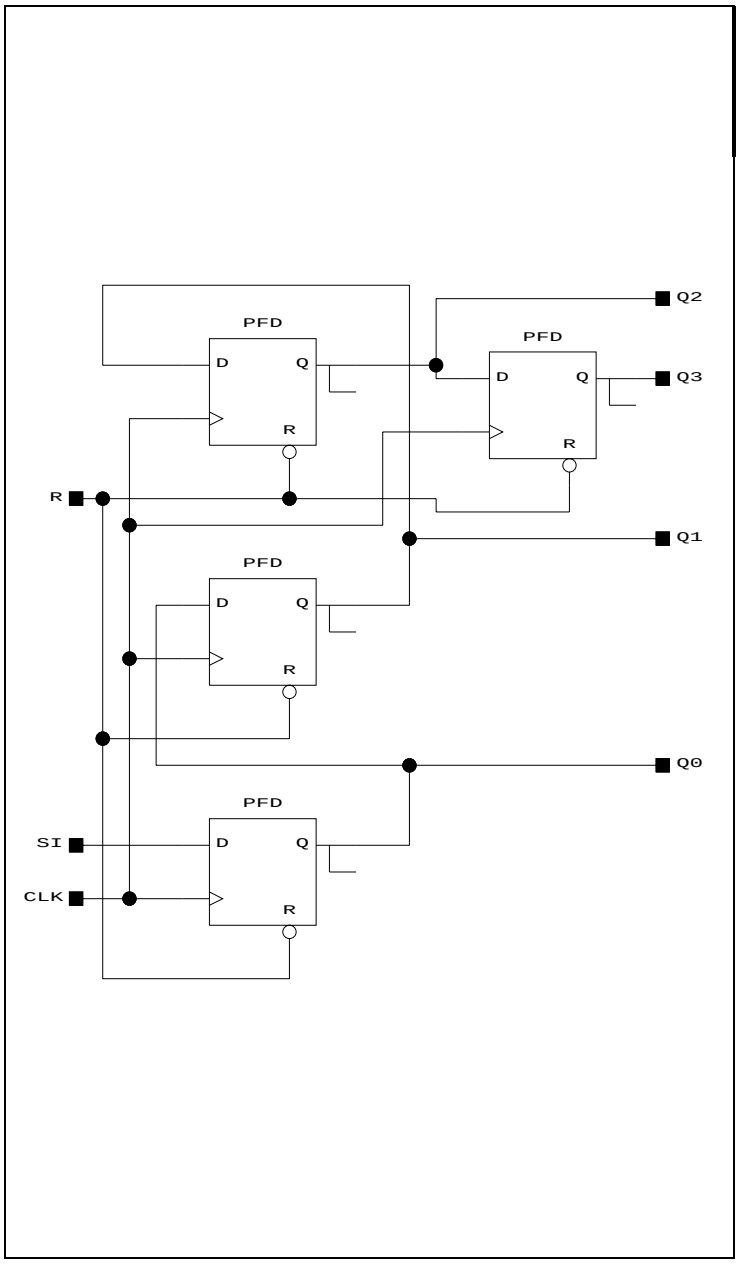
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
SI	2.10	2.10	2.10	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.40	2.70	3.00
CLK → Q3	2.40	2.70	3.00	3.00	3.30	3.60
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

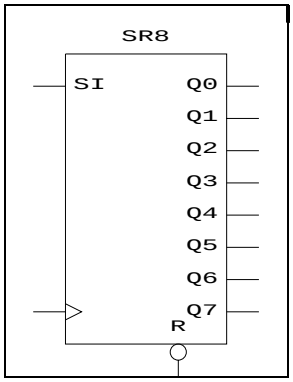
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
SI	3.50	3.50	3.50	0.00	0.00	0.00

Schematic



SR8 - 8-Bit Shift Register

Symbol



Rectangular Area: 1x8 cells

Number of Cells: 8

Truth Table

Input			Output							
A	CLK	SI	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	x	x	0	0	0	0	0	0	0	0
1	r	si	q6	q5	q4	q3	q2	q1	q0	si

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q7.BUS	-	-	-	1.90	2.20	2.50
CLK → Q7.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q7	-	-	-	1.40	1.60	1.80
CLK → Q7	1.40	1.60	1.80	1.80	2.00	2.20
R → Q6.BUS	-	-	-	1.90	2.20	2.50
CLK → Q6.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q6	-	-	-	1.48	1.71	1.93
CLK → Q6	1.49	1.71	1.92	1.88	2.11	2.33
R → Q5.BUS	-	-	-	1.90	2.20	2.50
CLK → Q5.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q5	-	-	-	1.48	1.71	1.93
CLK → Q5	1.49	1.71	1.92	1.88	2.11	2.33
R → Q4.BUS	-	-	-	1.90	2.20	2.50
CLK → Q4.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q4	-	-	-	1.48	1.71	1.93
CLK → Q4	1.49	1.71	1.92	1.88	2.11	2.33
R → Q3.BUS	-	-	-	1.90	2.20	2.50
CLK → Q3.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q3	-	-	-	1.48	1.71	1.93
CLK → Q3	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2.BUS	-	-	-	1.90	2.20	2.50
CLK → Q2.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1.BUS	-	-	-	1.90	2.20	2.50
CLK → Q1.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33

R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
SI	2.10	2.10	2.10	0.00	0.00	0.00

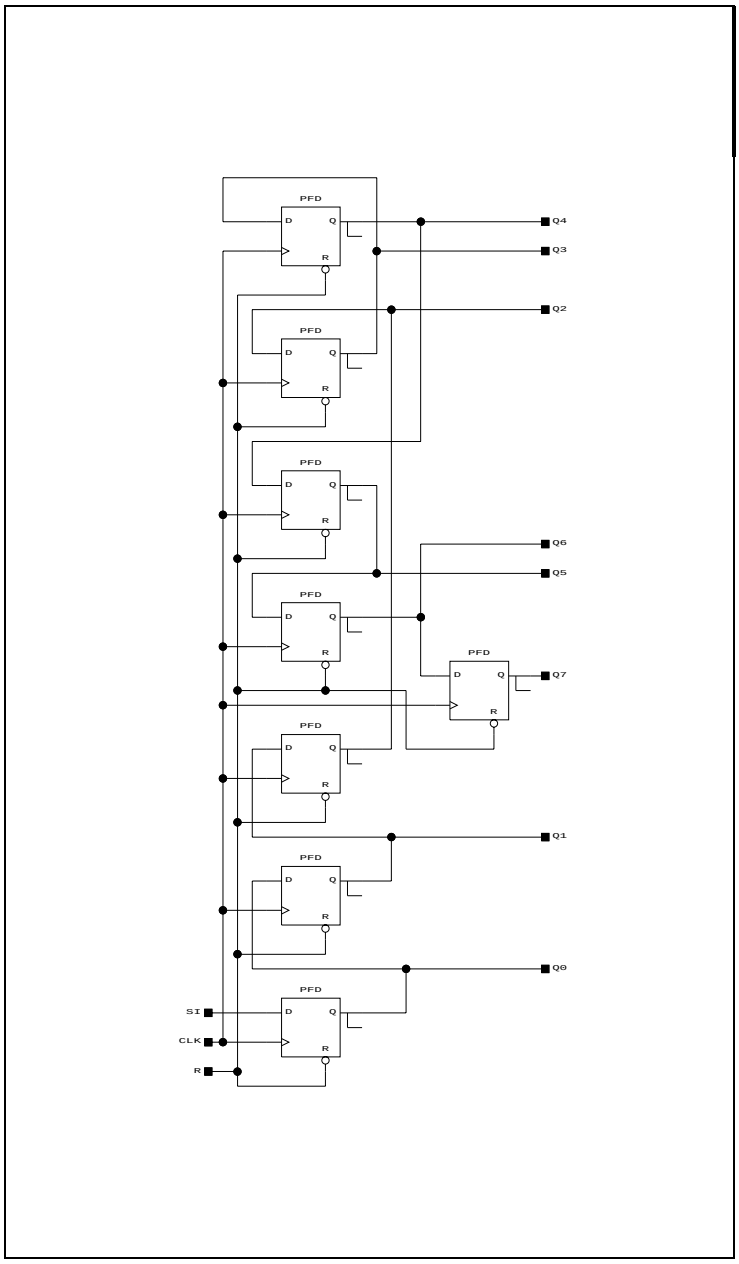
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q7.BUS	-	-	-	3.40	3.90	4.80
CLK → Q7.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q7	-	-	-	2.40	2.70	3.00
CLK → Q7	2.40	2.70	3.00	3.00	3.30	3.60
R → Q6.BUS	-	-	-	3.40	3.90	4.80
CLK → Q6.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q6	-	-	-	2.48	2.81	3.15
CLK → Q6	2.47	2.79	3.12	3.08	3.41	3.75
R → Q5.BUS	-	-	-	3.40	3.90	4.80
CLK → Q5.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q5	-	-	-	2.48	2.81	3.15
CLK → Q5	2.47	2.79	3.12	3.08	3.41	3.75
R → Q4.BUS	-	-	-	3.40	3.90	4.80
CLK → Q4.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q4	-	-	-	2.48	2.81	3.15
CLK → Q4	2.47	2.79	3.12	3.08	3.41	3.75
R → Q3.BUS	-	-	-	3.40	3.90	4.80
CLK → Q3.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q3	-	-	-	2.48	2.81	3.15
CLK → Q3	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2.BUS	-	-	-	3.40	3.90	4.80
CLK → Q2.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1.BUS	-	-	-	3.40	3.90	4.80
CLK → Q1.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75

R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

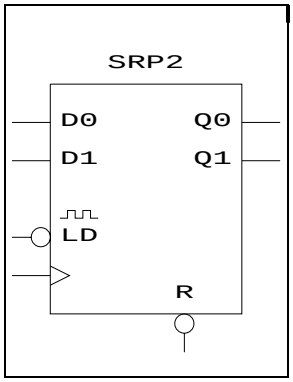
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
SI	3.50	3.50	3.50	0.00	0.00	0.00

Schematic



SRP2 - 2-Bit Shift Register with Parallel Load

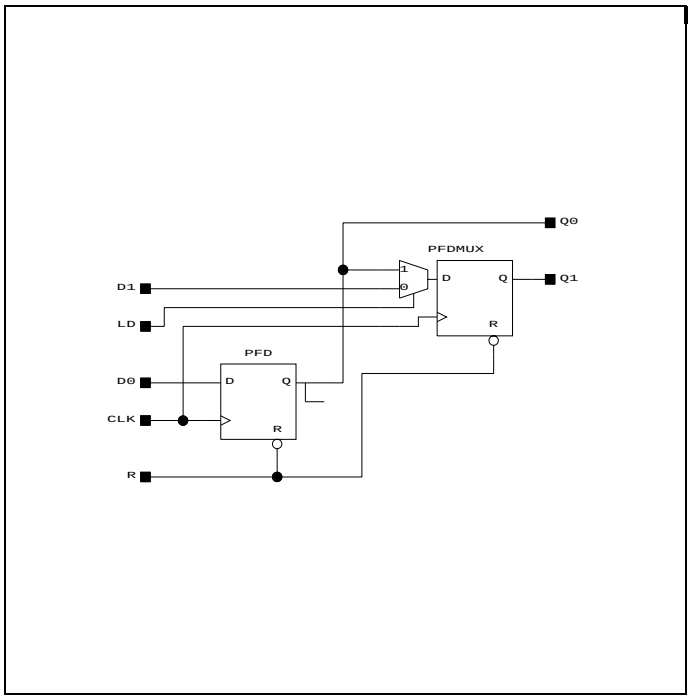
Symbol



Rectangular Area: 1x2 cells

Number of Cells: 2

Schematic



Truth Table

Input					Output	
R	CLK	LD	D1	D0	Q1	Q0
0	x	x	x	x	0	0
1	r	0	d1	d0	d1	d0
1	r	1	x	d0	q0	d0

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1	-	-	-	1.40	1.60	1.80
CLK → Q1	1.40	1.60	1.80	1.80	2.00	2.20

		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
LD	3.80	4.00	4.30	0.00	0.00	0.00
D1	3.90	4.10	4.30	0.00	0.00	0.00
D0	2.10	2.10	2.10	0.00	0.00	0.00

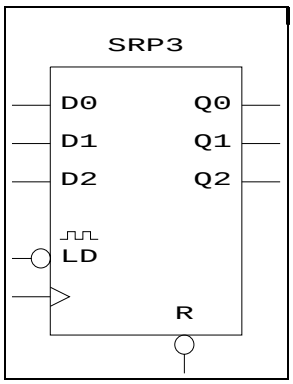
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1	-	-	-	2.40	2.70	3.00
CLK → Q1	2.40	2.70	3.00	3.00	3.30	3.60

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
LD	6.10	6.40	6.70	0.00	0.00	0.00
D1	6.30	6.60	6.90	0.00	0.00	0.00
D0	3.50	3.50	3.50	0.00	0.00	0.00

SRP3 - 3-Bit Shift Register with Parallel Load

Symbol



Rectangular Area: 1x3 cells

Number of Cells: 3

Truth Table

Input						Output		
A	CLK	LD	D2	D1	D0	Q2	Q1	Q0
0	x	x	x	x	x	0	0	0
1	r	0	d2	d1	d0	d2	d1	d0
1	r	1	x	x	d0	q1	q0	d0

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2	-	-	-	1.40	1.60	1.80
CLK → Q2	1.40	1.60	1.80	1.80	2.00	2.20

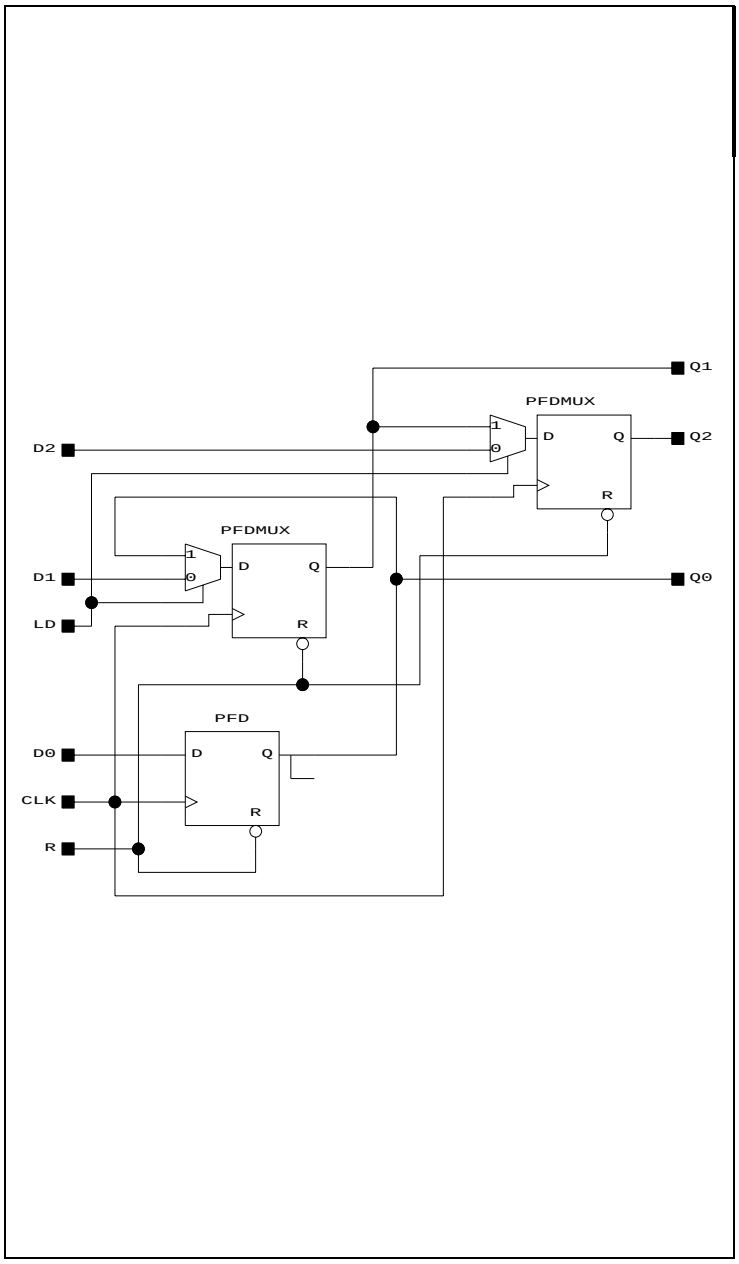
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
LD	3.80	4.00	4.30	0.00	0.00	0.00
D1	3.90	4.10	4.30	0.00	0.00	0.00
D2	3.90	4.10	4.30	0.00	0.00	0.00
D0	2.10	2.10	2.10	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2	-	-	-	2.40	2.70	3.00
CLK → Q2	2.40	2.70	3.00	3.00	3.30	3.60

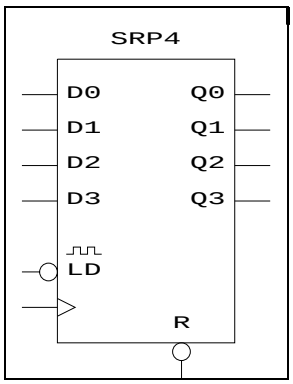
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
LD	6.10	6.40	6.70	0.00	0.00	0.00
D1	6.30	6.60	6.90	0.00	0.00	0.00
D2	6.30	6.60	6.90	0.00	0.00	0.00
D0	3.50	3.50	3.50	0.00	0.00	0.00

Schematic



SRP4 - 4-Bit Shift Register with Parallel Load

Symbol



Rectangular Area: 1x4 cells

Number of Cells: 4

Truth Table

Input							Output			
A	**CLK**	**LD**	**D3**	**D2**	**D1**	**D0**	**Q3**	**Q2**	**Q1**	**Q0**
0	x	x	x	x	x	x	0	0	0	0
1	r	0	d3	d2	d1	d0	d3	d2	d1	d0
1	r	1	x	x	x	d0	q2	q1	q0	d0

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q3	-	-	-	1.40	1.60	1.80
CLK → Q3	1.40	1.60	1.80	1.80	2.00	2.20

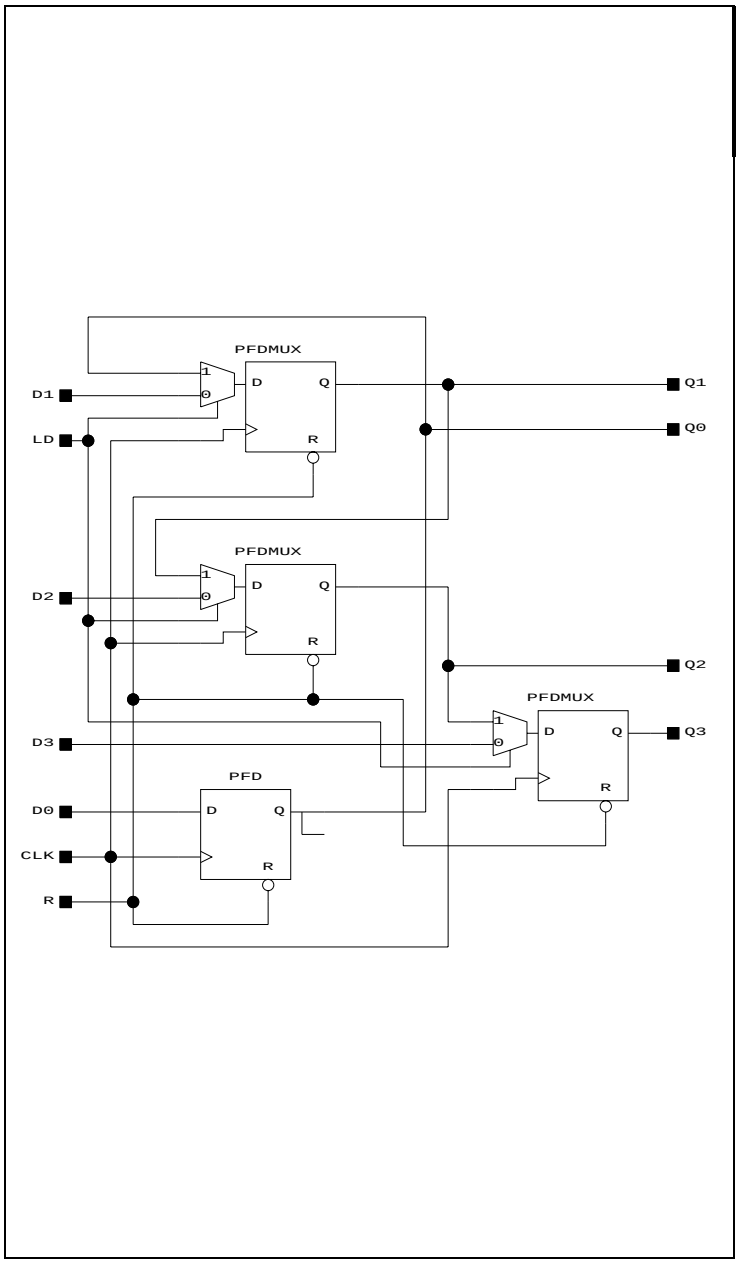
		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D0	2.10	2.10	2.10	0.00	0.00	0.00
D1	3.90	4.10	4.30	0.00	0.00	0.00
D2	3.90	4.10	4.30	0.00	0.00	0.00
D3	3.90	4.10	4.30	0.00	0.00	0.00
LD	3.80	4.00	4.30	0.00	0.00	0.00

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q3	-	-	-	2.40	2.70	3.00
CLK → Q3	2.40	2.70	3.00	3.00	3.30	3.60

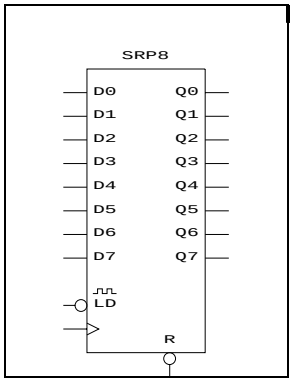
		Setup			Hold	
Pin	Min	Typ	Max	Min	Typ	Max
D0	3.50	3.50	3.50	0.00	0.00	0.00
D1	6.30	6.60	6.90	0.00	0.00	0.00
D2	6.30	6.60	6.90	0.00	0.00	0.00
D3	6.30	6.60	6.90	0.00	0.00	0.00
LD	6.10	6.40	6.70	0.00	0.00	0.00

Schematic



SRP8 - 8-Bit Shift Register with Parallel Load

Symbol



Rectangular Area: 1x8 cells

Number of Cells: 8

Truth Table

Input				Output
A	**CLK**	**LD**	**D7...D0**	**Q7...Q0**
0	x	x	x...x	0...0
1	r	0	d7...d0	d7...d0
1	r	1	d7...d0	q6,q5,q4...d0

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
R → Q7	-	-	-	1.40	1.60	1.80
CLK → Q7	1.40	1.60	1.80	1.80	2.00	2.20
R → Q6	-	-	-	1.48	1.71	1.93
CLK → Q6	1.49	1.71	1.92	1.88	2.11	2.33
R → Q5	-	-	-	1.48	1.71	1.93
CLK → Q5	1.49	1.71	1.92	1.88	2.11	2.33
R → Q4	-	-	-	1.48	1.71	1.93
CLK → Q4	1.49	1.71	1.92	1.88	2.11	2.33
R → Q3	-	-	-	1.48	1.71	1.93
CLK → Q3	1.49	1.71	1.92	1.88	2.11	2.33
R → Q2	-	-	-	1.48	1.71	1.93
CLK → Q2	1.49	1.71	1.92	1.88	2.11	2.33
R → Q1	-	-	-	1.48	1.71	1.93
CLK → Q1	1.49	1.71	1.92	1.88	2.11	2.33
R → Q0.BUS	-	-	-	1.90	2.20	2.50
CLK → Q0.BUS	1.80	2.10	2.40	2.30	2.60	2.90
R → Q0	-	-	-	1.48	1.71	1.93
CLK → Q0	1.49	1.71	1.92	1.88	2.11	2.33

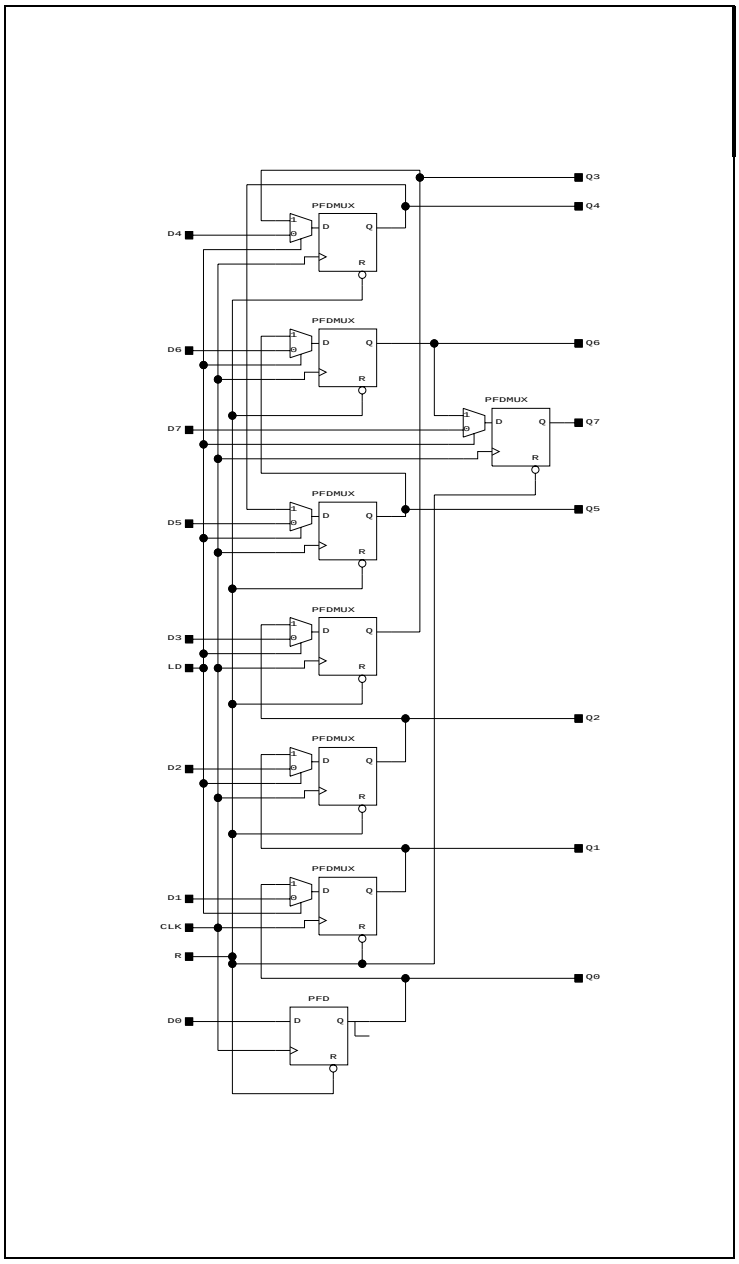
	Setup			Hold		
Pin	Min	Typ	Max	Min	Typ	Max
LD	3.80	4.00	4.30	0.00	0.00	0.00
D7	3.90	4.10	4.30	0.00	0.00	0.00
D6	3.90	4.10	4.30	0.00	0.00	0.00
D5	3.90	4.10	4.30	0.00	0.00	0.00
D4	3.90	4.10	4.30	0.00	0.00	0.00
D3	3.90	4.10	4.30	0.00	0.00	0.00
D2	3.90	4.10	4.30	0.00	0.00	0.00
D1	3.90	4.10	4.30	0.00	0.00	0.00
D0	2.10	2.10	2.10	0.00	0.00	0.00

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
R → Q7	-	-	-	2.40	2.70	3.00
CLK → Q7	2.40	2.70	3.00	3.00	3.30	3.60
R → Q6	-	-	-	2.48	2.81	3.15
CLK → Q6	2.47	2.79	3.12	3.08	3.41	3.75
R → Q5	-	-	-	2.48	2.81	3.15
CLK → Q5	2.47	2.79	3.12	3.08	3.41	3.75
R → Q4	-	-	-	2.48	2.81	3.15
CLK → Q4	2.47	2.79	3.12	3.08	3.41	3.75
R → Q3	-	-	-	2.48	2.81	3.15
CLK → Q3	2.47	2.79	3.12	3.08	3.41	3.75
R → Q2	-	-	-	2.48	2.81	3.15
CLK → Q2	2.47	2.79	3.12	3.08	3.41	3.75
R → Q1	-	-	-	2.48	2.81	3.15
CLK → Q1	2.47	2.79	3.12	3.08	3.41	3.75
R → Q0.BUS	-	-	-	3.40	3.90	4.80
CLK → Q0.BUS	3.10	3.60	4.40	4.00	4.50	5.40
R → Q0	-	-	-	2.48	2.81	3.15
CLK → Q0	2.47	2.79	3.12	3.08	3.41	3.75

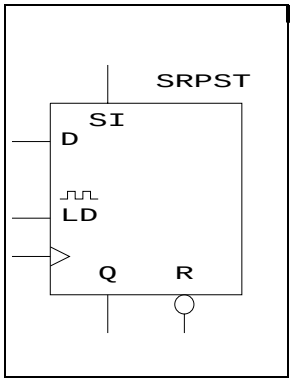
	Setup			Hold		
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
LD	6.10	6.40	6.70	0.00	0.00	0.00
D7	6.30	6.60	6.90	0.00	0.00	0.00
D6	6.30	6.60	6.90	0.00	0.00	0.00
D5	6.30	6.60	6.90	0.00	0.00	0.00
D4	6.30	6.60	6.90	0.00	0.00	0.00
D3	6.30	6.60	6.90	0.00	0.00	0.00
D2	6.30	6.60	6.90	0.00	0.00	0.00
D1	6.30	6.60	6.90	0.00	0.00	0.00
D0	3.50	3.50	3.50	0.00	0.00	0.00

Schematic


PFDMUX
PFDMUX
PFDMUX
PFDMUX
PFDMUX
PFDMUX
PFDMUX
PFDMUX
PFD
D4
D6
D7
D5
D3
LD
D2
D1
CLK
R
D0
Q3
Q4
Q6
Q7
Q5
Q2
Q1
Q0

SRPST - Bit Stage Shift Register w/ Parallel Load

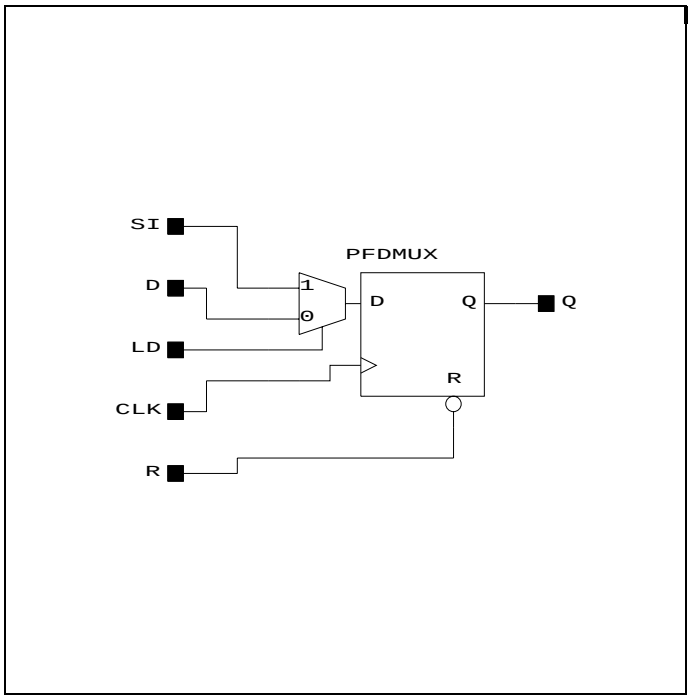
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	CLK	LD	SI	D	Output Q
0	x	x	x	x	0
1	r	0	x	d	d
1	r	1	si	x	si

Switching Speeds for -2ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
CLK → Q	1.40	1.60	1.80	1.80	2.00	2.20
R → Q	0.00	0.00	0.00	1.40	1.60	1.80

	Setup			Hold		
Pin	Min	Typ	Max	Min	Typ	Max
D	3.90	4.10	4.30	0.00	0.00	0.00
SI	3.90	4.10	4.30	0.00	0.00	0.00
LD	3.80	4.00	4.30	0.00	0.00	0.00

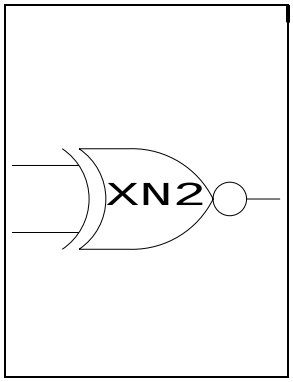
Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
CLK → Q	2.40	2.70	3.00	3.00	3.30	3.60
R → Q	0.00	0.00	0.00	2.40	2.70	3.00

		Setup			Hold	
Pin	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
D	6.30	6.60	6.90	0.00	0.00	0.00
SI	6.30	6.60	6.90	0.00	0.00	0.00
LD	6.10	6.40	6.70	0.00	0.00	0.00

XN2 - 2-Input XNOR

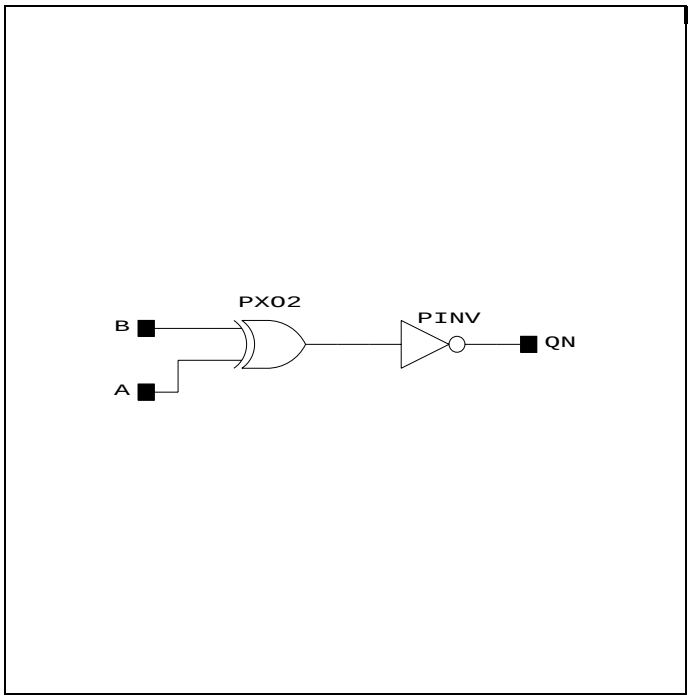
Symbol



Rectangular Area: 2x1 cells

Number of Cells: 2

Schematic



Truth Table

Input A	Input B	Output QN
0	0	1
0	1	0
1	0	0

Switching Speeds for -2ns Parts

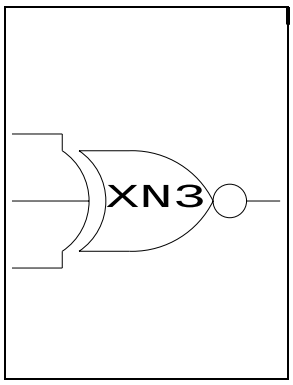
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN.BUS	2.07	3.68	5.19	2.07	3.68	5.19
B → QN.BUS	1.97	3.58	5.09	2.07	3.68	5.19
A → QN	1.67	3.18	4.59	1.57	3.08	4.49
B → QN	1.57	3.08	4.49	1.57	3.08	4.49

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → QN.BUS	5.06	6.18	8.32	4.97	6.09	8.31
B → QN.BUS	4.66	5.78	7.92	4.97	6.09	8.31
A → QN	4.36	5.28	6.92	3.97	4.89	6.51
B → QN	3.96	4.88	6.52	3.97	4.89	6.51

XN3 - 3-Input XNOR

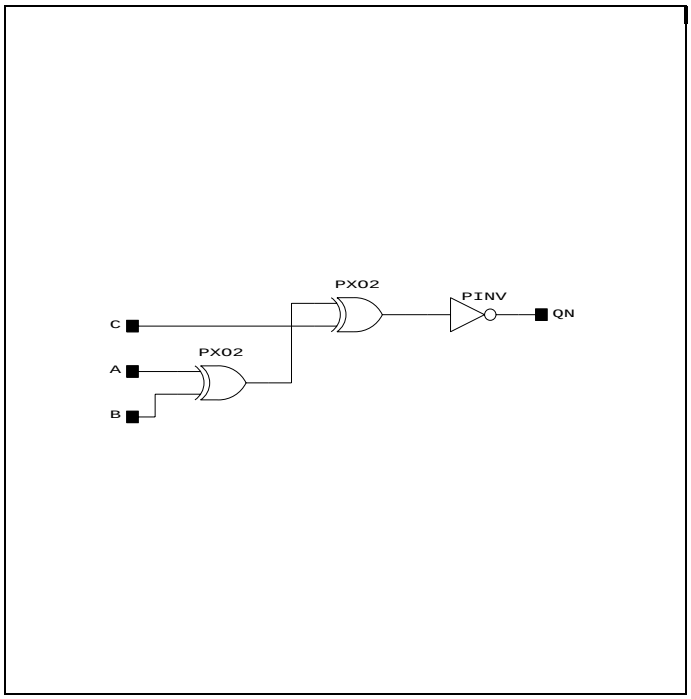
Symbol



Rectangular Area: 3x1 cells

Number of Cells: 3

Schematic



Truth Table

Input			Output
A	B	C	QN
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Switching Speeds for -2ns Parts

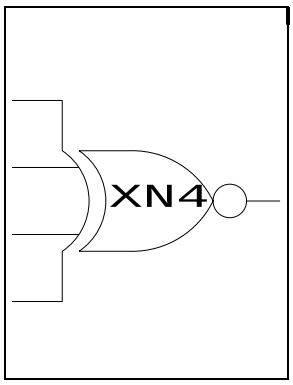
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
C → QN.BUS	2.07	3.68	5.19	2.07	3.48	4.99
B → QN.BUS	2.94	5.26	7.48	2.94	5.06	7.28
A → QN.BUS	2.94	5.26	7.48	2.94	5.06	7.28
C → QN	1.67	3.18	4.59	1.57	2.88	4.29
B → QN	2.54	4.76	6.88	2.44	4.46	6.58
A → QN	2.54	4.76	6.88	2.44	4.46	6.58

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
C → QN.BUS	5.16	6.38	8.82	4.87	6.09	8.31
B → QN.BUS	7.04	9.56	13.14	6.74	9.27	12.63
A → QN.BUS	7.04	9.56	13.14	6.74	9.27	12.63
C → QN	4.46	5.48	7.42	3.87	4.89	6.51
B → QN	6.34	8.66	11.74	5.74	8.07	10.83
A → QN	6.34	8.66	11.74	5.74	8.07	10.83

XN4 - 4-Input XNOR

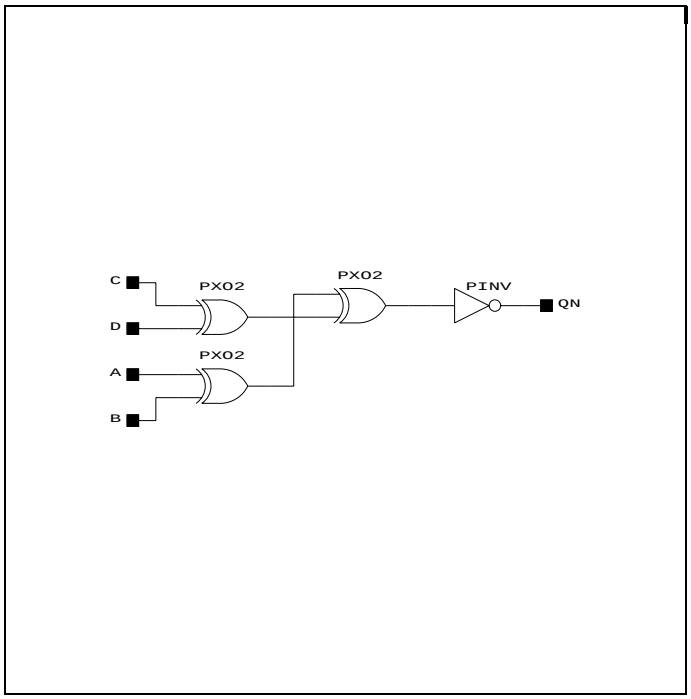
Symbol



Rectangular Area: 3x2 cells

Number of Cells: 5

Schematic



Truth Table

Input				Output
A	B	C	D	QN
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Switching Speeds for -2ns Parts

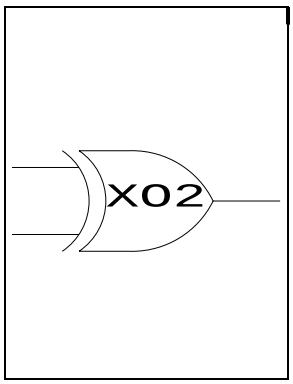
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D → QN.BUS	3.41	6.04	8.67	3.41	5.84	8.47
C → QN.BUS	3.41	6.04	8.67	3.41	5.84	8.47
B → QN.BUS	2.94	5.26	7.48	2.94	5.06	7.28
A → QN.BUS	2.94	5.26	7.48	2.94	5.06	7.28
D → QN	3.01	5.54	8.07	2.91	5.24	7.77
C → QN	3.01	5.54	8.07	2.91	5.24	7.77
B → QN	2.54	4.76	6.88	2.44	4.46	6.58
A → QN	2.54	4.76	6.88	2.44	4.46	6.58

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D → QN.BUS	8.11	10.85	14.87	7.82	10.56	14.36
C → QN.BUS	8.11	10.85	14.87	7.82	10.56	14.36
B → QN.BUS	7.04	9.56	13.14	6.74	9.27	12.63
A → QN.BUS	7.04	9.56	13.14	6.74	9.27	12.63
D → QN	7.41	9.95	13.47	6.82	9.36	12.56
C → QN	7.41	9.95	13.47	6.82	9.36	12.56
B → QN	6.34	8.66	11.74	5.74	8.07	10.83
A → QN	6.34	8.66	11.74	5.74	8.07	10.83

XO2 - 2-Input XOR

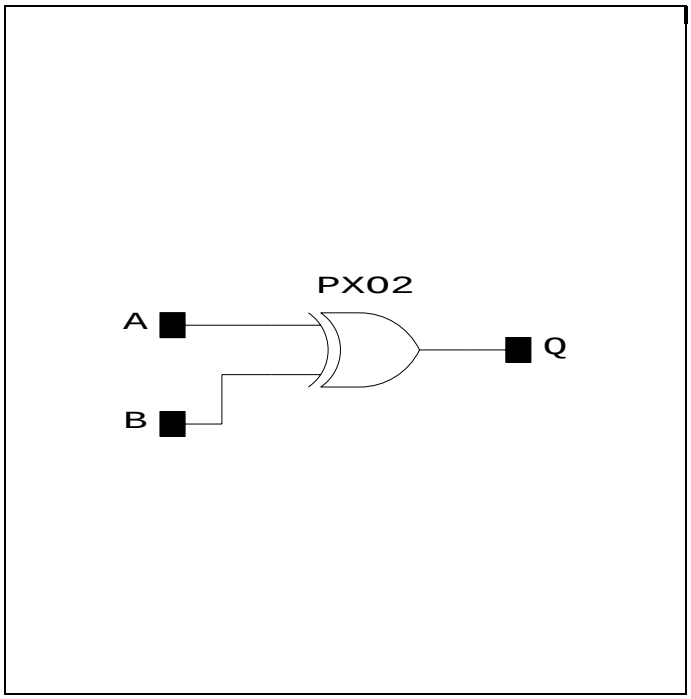
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input A	Input B	Output Q
0	0	0
0	1	1
1	0	1
1	1	0

Switching Speeds for -2ns Parts

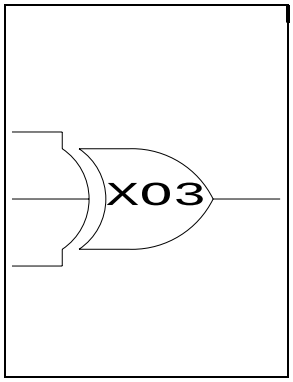
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	0.80	1.60	2.30	0.70	1.40	2.10
B → Q	0.80	1.60	2.30	0.80	1.50	2.20

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q	1.90	2.30	3.10	2.00	2.50	3.30
B → Q	1.90	2.30	3.10	2.40	2.90	3.70

XO3 - 3-Input XOR

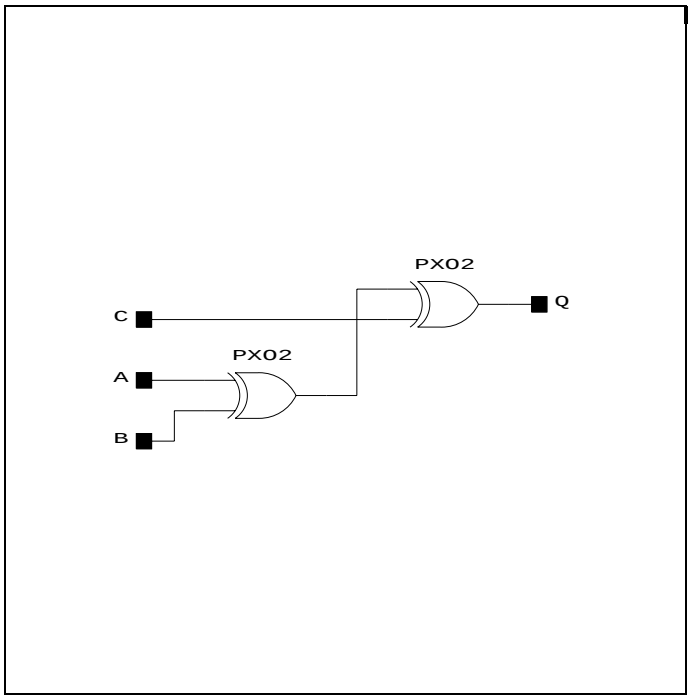
Symbol



Rectangular Area: 2x1 cells

Number of Cells: 2

Schematic



Truth Table

Input			Output
A	B	C	Q
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Switching Speeds for -2ns Parts

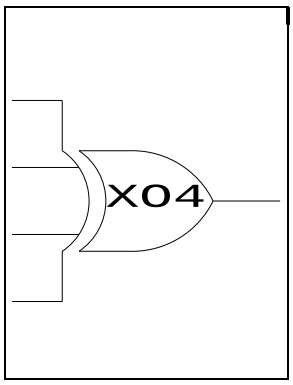
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
C → Q.BUS	1.20	1.90	2.70	1.30	2.10	2.90
B → Q.BUS	2.07	3.48	4.99	2.17	3.68	5.19
A → Q.BUS	2.07	3.48	4.99	2.17	3.68	5.19
C → Q	0.80	1.40	2.10	0.80	1.50	2.20
B → Q	1.67	2.98	4.39	1.67	3.08	4.49
A → Q	1.67	2.98	4.39	1.67	3.08	4.49

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
C → Q.BUS	2.50	3.20	4.50	3.50	4.30	6.00
B → Q.BUS	4.37	6.38	8.82	5.37	7.48	10.32
A → Q.BUS	4.37	6.38	8.82	5.37	7.48	10.32
C → Q	1.80	2.30	3.10	2.50	3.10	4.20
B → Q	3.67	5.48	7.42	4.37	6.28	8.52
A → Q	3.67	5.48	7.42	4.37	6.28	8.52

XO4 - 4-Input XOR

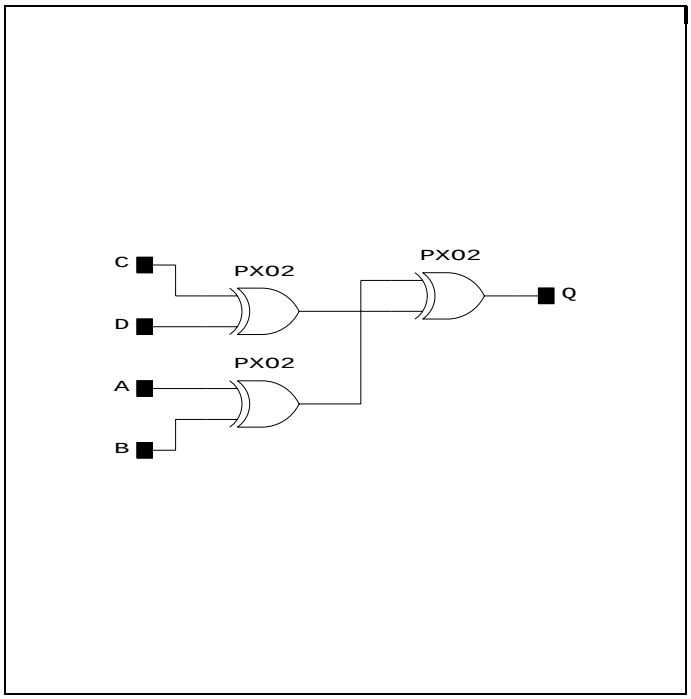
Symbol



Rectangular Area: 2x2 cells

Number of Cells: 4

Schematic



Truth Table

Input				Output
A	B	C	D	Q
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	1	0

Switching Speeds for -2ns Parts

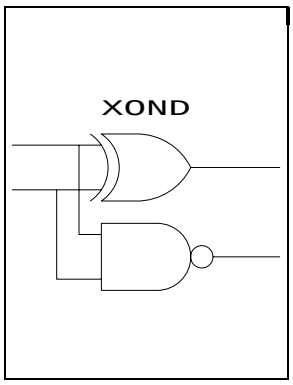
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D → Q.BUS	2.54	4.26	6.18	2.64	4.46	6.38
C → Q.BUS	2.54	4.26	6.18	2.64	4.46	6.38
B → Q.BUS	2.07	3.48	4.99	2.17	3.68	5.19
A → Q.BUS	2.07	3.48	4.99	2.17	3.68	5.19
D → Q	2.14	3.76	5.58	2.14	3.86	5.68
C → Q	2.14	3.76	5.58	2.14	3.86	5.68
B → Q	1.67	2.98	4.39	1.67	3.08	4.49
A → Q	1.67	2.98	4.39	1.67	3.08	4.49

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
D → QN.BUS	8.11	10.85	14.87	7.82	10.56	14.36
C → QN.BUS	8.11	10.85	14.87	7.82	10.56	14.36
B → QN.BUS	7.04	9.56	13.14	6.74	9.27	12.63
A → QN.BUS	7.04	9.56	13.14	6.74	9.27	12.63
D → QN	7.41	9.95	13.47	6.82	9.36	12.56
C → QN	7.41	9.95	13.47	6.82	9.36	12.56
B → QN	6.34	8.66	11.74	5.74	8.07	10.83
A → QN	6.34	8.66	11.74	5.74	8.07	10.83

XOND - 2-Input XOR/NAND

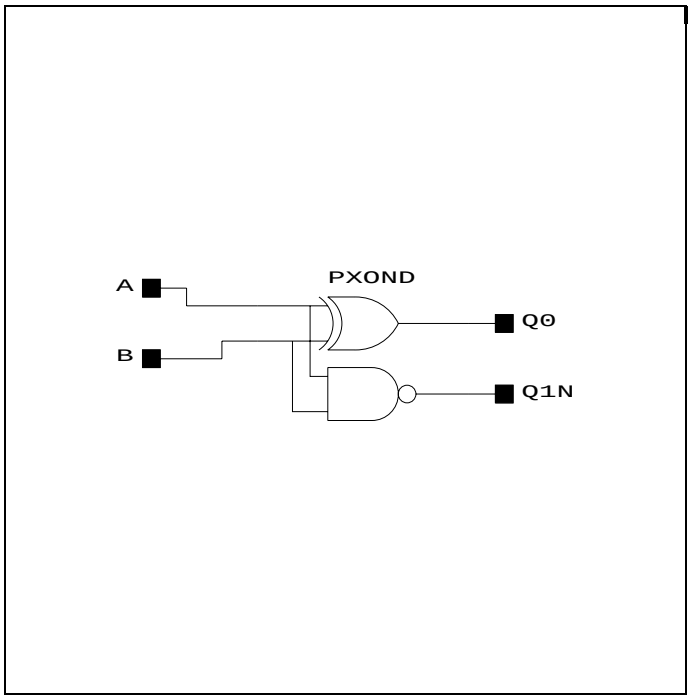
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output	
A	B	Q0	Q1N
0	0	0	1
0	1	1	1
1	0	1	1
1	1	0	0

Switching Speeds for -2ns Parts

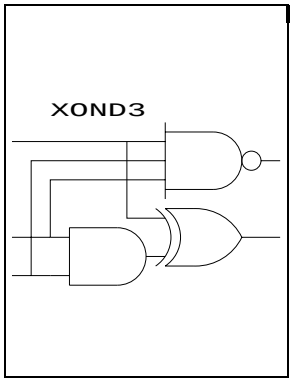
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q0	0.80	1.60	2.30	0.70	1.40	2.10
B → Q0	0.80	1.60	2.30	0.80	1.50	2.20
A → Q1N	0.80	1.40	2.10	0.80	1.40	2.10
B → Q1N	0.80	1.40	2.10	0.90	1.50	2.20

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q0	1.90	2.30	3.10	2.00	2.50	3.30
B → Q0	1.90	2.30	3.10	2.40	2.90	3.70
A → Q1N	1.80	2.20	3.00	1.80	2.20	3.00
B → Q1N	2.20	2.60	3.40	1.80	2.20	3.00

XOND3 - 2-Input XOR with 3-Input NAND

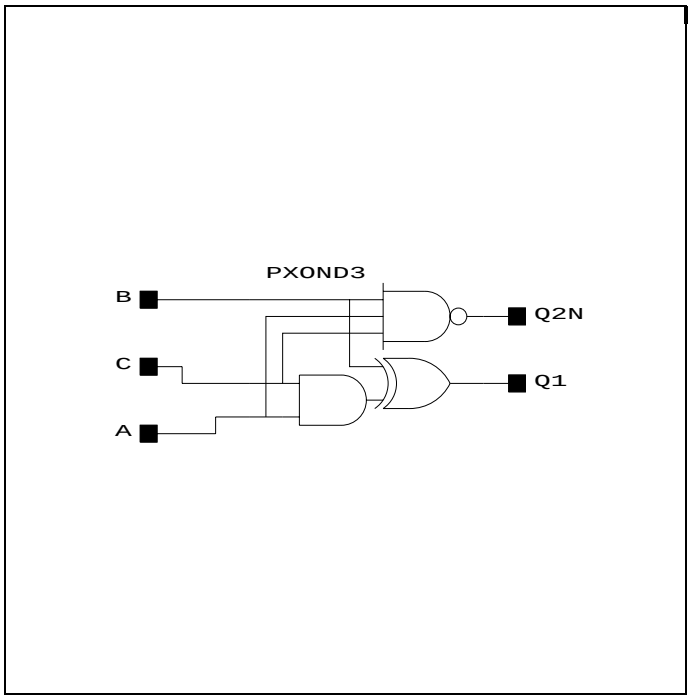
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Input		Output		
A	B	C	Q1	Q2N
0	0	0	0	1
0	0	1	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

Switching Speeds for -2ns Parts

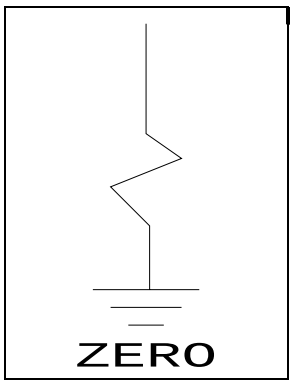
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max
A → Q1	0.80	1.40	2.10	0.80	1.50	2.20
B → Q1	0.80	1.40	2.10	0.80	1.50	2.20
C → Q1	0.80	1.40	2.10	0.90	1.60	2.30
A → Q2N	0.80	1.40	2.20	0.70	1.40	2.10
B → Q2N	0.80	1.40	2.20	0.70	1.40	2.10
C → Q2N	0.90	1.50	2.30	0.70	1.40	2.10

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max
A → Q1	1.80	2.30	3.10	2.50	3.10	4.20
B → Q1	1.80	2.30	3.10	2.50	3.10	4.20
C → Q1	1.80	2.30	3.10	2.90	3.50	4.60
A → Q2N	1.70	2.10	2.90	1.80	2.30	3.00
B → Q2N	1.70	2.10	2.90	1.80	2.30	3.00
C → Q2N	1.70	2.10	2.90	2.20	2.70	3.40

ZERO/ZEROB - Logic Zero

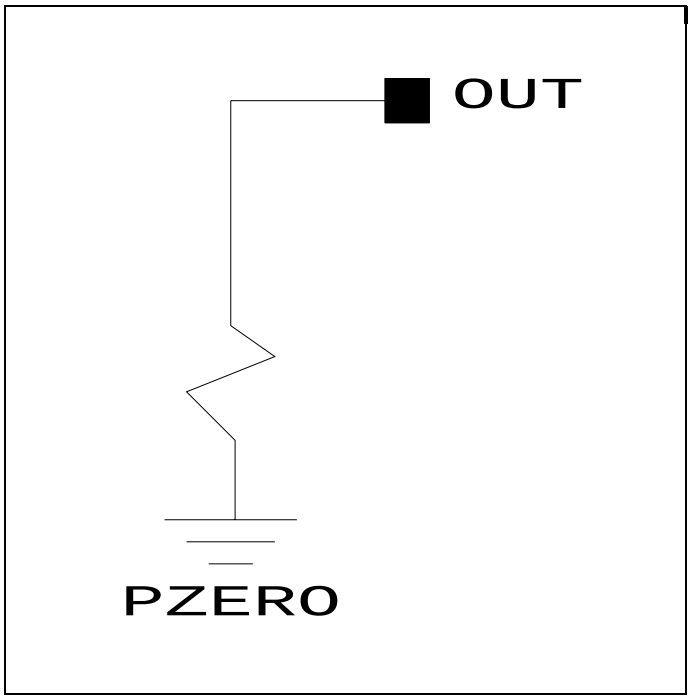
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Output OUT/OUTB
0

Switching Speeds for -2ns Parts

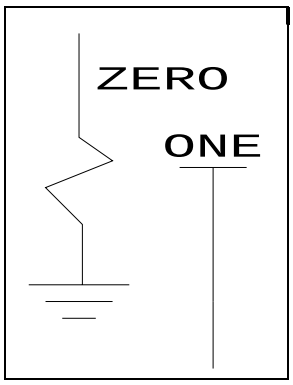
	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max

Switching Speeds for -4ns Parts

	Rise			Fall		
Pin	Min	Typ	Max	Min	Typ	Max

ZEROONE - Logic One and Logic Zero

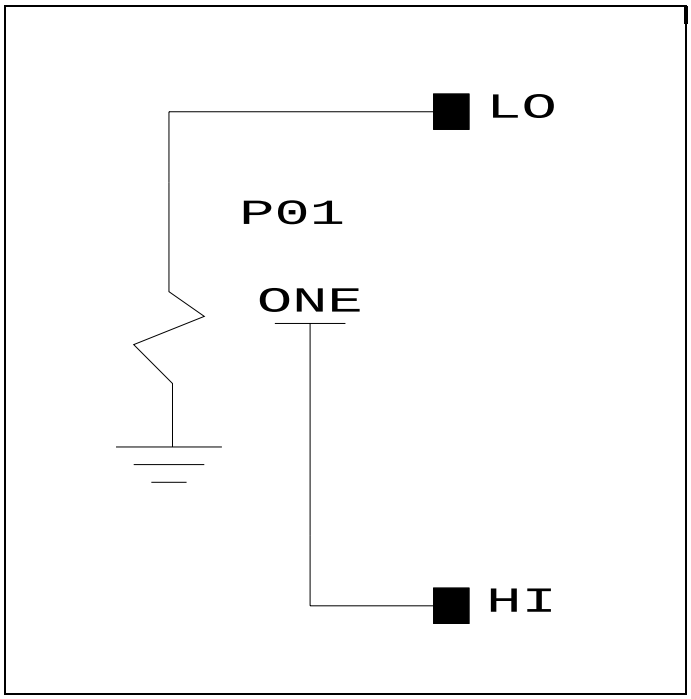
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Output	
LO	HI
0	1

Switching Speeds for -2ns Parts

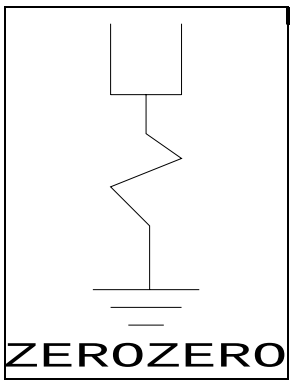
		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max

ZEROZERO - Twin Logic Zeros

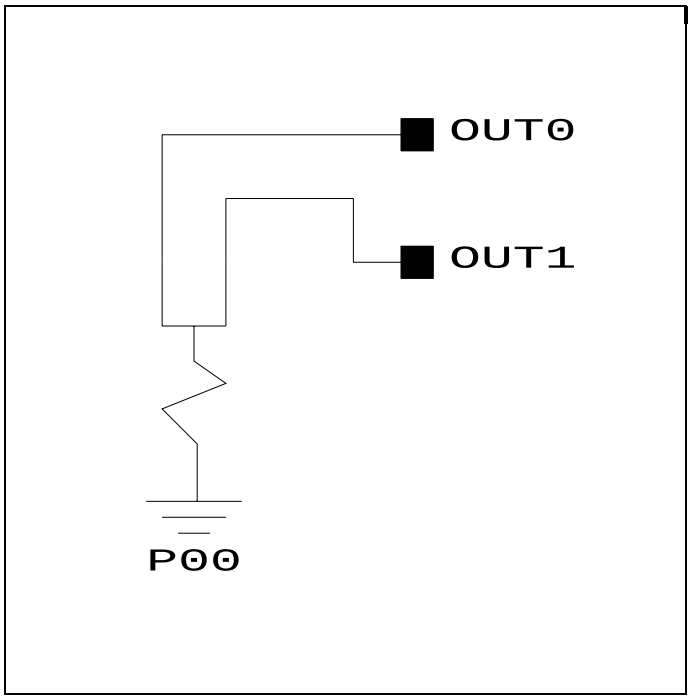
Symbol



Rectangular Area: 1x1 cells

Number of Cells: 1

Schematic



Truth Table

Output	
OUT0	OUT1
0	0

Switching Speeds for -2ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max

Switching Speeds for -4ns Parts

		Rise			Fall	
Pin	Min	Typ	Max	Min	Typ	Max