AVR109: Self Programming

8-bit AVR® RISC Microcontroller

Application Note

Features

- C-code sample application for Self Programming
- Read and Write Both Flash and EEPROM Memories
- Read and Write Lock Bits
- Read Fuse Bits
- Designed to work with AVR911 Open Source Programmer
- Compatible with AVRProg
- Protocol optimized for efficient programming

Introduction

This application note describes how an AVR with the Store Program Memory (SPM) instruction can be configured for Self-programming. The sample application communicates via the UART with a PC running the AVR Open Source Programmer (AVROSP) from Application note AVR911. This enables Flash and EEPROM programming without the need for an external programmer. The code is also compatible with AVRProg (only for devices supported by AVRProg).

A Boot Loader program is placed inside the Boot Section of the Flash memory. This program handles communication with the host PC, and facilitates programming of both Flash and EEPROM. Once programmed, different levels of protection can be individually applied to both the boot and application portion of the Flash memory. The AVR thus offers a unique flexibility, allowing the user extensive degrees of memory protection.

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SPM Explained

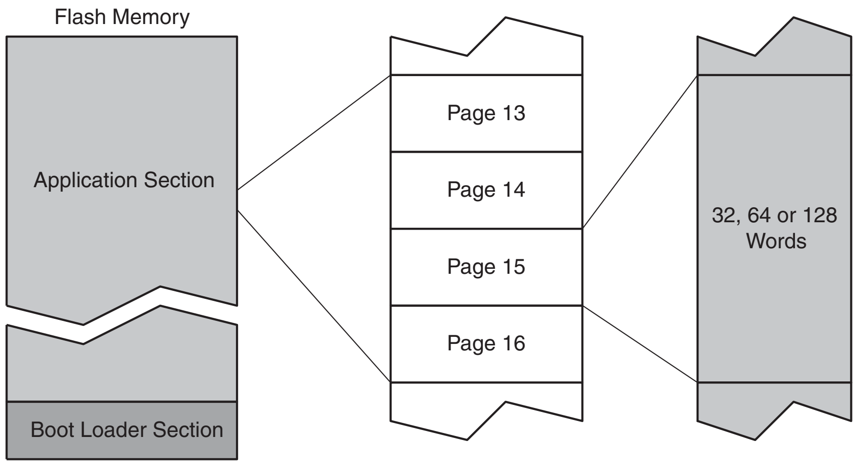
To get a better understanding of the AVRs' Self-programming capabilities, the basics of this feature are explained below.

Memory Organization

The Flash memory is divided into two sections, one Application section and one Boot Loader section. The Application section contains the main code for the application, while the Boot Loader section contains the code for the actual Self-programming. The SPM instruction can only be executed from the Boot Loader section. (Note: The Boot Loader section can also be used for ordinary application code.)

The Flash memory is divided into pages containing 32, 64, or 128 words each. The usage of pages is explained later. The entire memory span, both Application and Boot Loader sections, is divided into pages. For instance, a device with 8 KB of Flash and page size of 32 words (64 bytes) will therefore have a total of 128 pages. The memory organization is shown in Figure 1.

Figure 1. Memory Organization



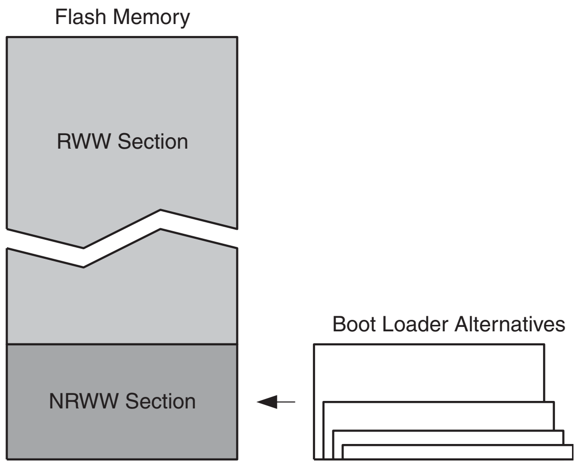
The size of the Boot Loader section can be selected using the two BOOTSZx Fuses. The fuses select one of four predefined sizes. The BOOTSZx Fuses can be changed using Serial or Parallel Programming. Refer to the devices' data sheet for details.

If a Boot Loader is implemented, it can be called either directly from the Application code using calls or jumps, or by programming the BOOTRST Fuse. When the BOOTRST Fuse is programmed, the CPU will start execution in the Boot Loader section on Reset, instead of starting at address 0. The BOOTRST Fuse can be changed using Serial or Parallel Programming.

Read-While-Write Capabilities

In addition to the selectable division between the application and Boot Loader sections, the Flash is also divided into two fixed-size sections. The first section is the Read-While-Write (RWW) section. The second is the No-Read-While-Write (NRWW) section. The NRWW section size always equals the largest selectable Boot Loader section size, thus the Boot Loader section occupies all or part of the NRWW section. This is illustrated in Figure 2.

Figure 2. RWW and NRWW Sections



The difference between the sections is that the NRWW section is accessible while updating the RWW section. It is not possible to access the RWW section when it's being updated. When the NRWW is updated (e.g., updating the Boot Loader code itself), the CPU is halted during the whole operation. In other words, No-Read-While-Writing to the NRWW section, but possible to Read-While-Writing to the RWW section. Refer to the devices' data sheet for details.

This functionality makes it possible to continue execution of critical code while updating the RWW section. Note that this critical code must be contained within the NRWW section (not necessarily in the Boot Loader section). See the section on interrupts below for more information.

The ATmega163 and ATmega323 devices don't have NRWW and RWW sections, only the selectable division into application and Boot Loader sections. Any updates to Flash memory on these devices halt the CPU during the whole operation.

Using the SPM Instruction

All Self-programming operations are performed using the SPM instruction. The operation is selected using the SPMCR Register (SPMCSR in some devices). The register is organized as shown in Figure 3.

Figure 3. The SPMCR Register

Bit 7							Bit 0
SPMIE	RWWSB	-	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN

When using the SPM function, the SPMEN bit must always be set within four cycles prior to executing the SPM instruction. This is to prevent unintentional Flash updates. The software must ensure that no interrupt routines are called between setting the SPMEN bit and executing the SPM instruction, thus exceeding the 4-cycle limit. The other four highlighted bits choose between the different SPM functions. The SPMEN bit is automatically cleared together with the function bit when the operation is completed.

The SPM functions are described below.

Page Erase

All Flash memory updates are done page by page. Before writing new data to a page, the page must be erased.

The Z-register is used to select the page to be erased. Set up the Z-register to point to a byte in the page to be erased. The lower bits selecting the byte within the page are ignored. For instance, on a device with a page size of 32 words (64 bytes), the lower six bits of the Z-register are ignored.

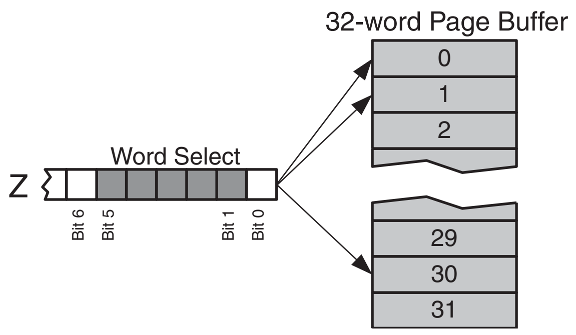
To erase a page, set the PGERS and SPMEN bits in the SPMCR Register and execute the SPM instruction.

Loading Page Buffer

To write new data to a page, the Page Buffer must be filled first. The Page Buffer is a separate (not SRAM) write-only buffer holding one temporary page. This buffer must be filled word by word. The buffer is copied to Flash memory in one operation.

The Z-register is used to select the word to be written into the buffer. The LSB of Z is ignored, as an entire word is always written in one operation. Single byte access is thus not possible. The higher bits of Z selecting the page are ignored when writing to the Page Buffers. The Z-register bit structure for a 32-word (64-byte) page is shown in Figure 4. Larger page sizes use more bits for word selection.

Figure 4. Writing to Page Buffer

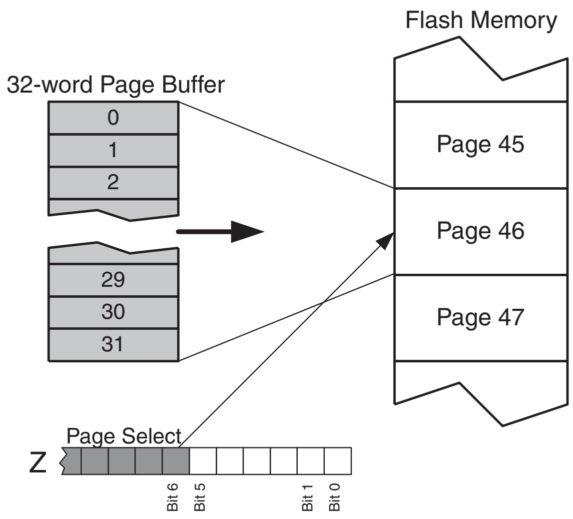


To write a word to the Page Buffer, load the word into the R1:R0 Registers. Set the Z-register to point to the correct word and set only the SPMEN bit in the SPMCR Register. The SPM instruction must then be executed within four cycles.

Page Write

When the Page Buffer is loaded with new data, it must be written to Flash memory. To do this, set up the Z-register the same way as described in the section regarding Page Erase. Then set the PGWRT and SPMEN bits in the SPMCR Register and execute the SPM instruction within four cycles. The R1:R0 Register contents are ignored. The use of the Z-register for 32-word (64-byte) page write is shown in Figure 5.

Figure 5. Writing a Page to Flash



The SPMEN bit can be polled to find out when the CPU is ready for further page updates. The update procedure can also be interrupt controlled. See the section on interrupts below for more information.

The RWW Section Busy Flag

When performing a Page Erase or Page Write operation on the RWW section, the RWWSB Flag is set by hardware, indicating that the section is inaccessible. The RWWSB Flag should be cleared in software when the SPM operation is completed. This is done by setting the RWWSRE and SPMEN bits in the SPMCR Register, followed by an SPM instruction within four cycles. Alternatively, the flag is automatically cleared by starting to load the Page Buffers. The RWWSB Flag can be used by other parts of the application to check the RWW section's current accessibility. Refer to the devices' data sheet for more details.

Note that the contents of the Z-register and the R1:R0 Registers are ignored when using the RWWSRE function.

Note that if the RWW section accessed without re-enabling it after an erase or write operation, all addresses in the RRW section read 0xFFFF. This applies both when reading the Flash using LPM and if performing calls or jumps into the RWW section. The consequence of performing a jump into the RWW section without enabling it will therefore be that the program code "0xFFFF" is executed, eventually leading to that the program counter "falls" through the code space until it meets the first executable code. The first executable code would in that case be encountered on the first address of the NRWW section.

The Boot Lock Bits

The application and Boot Loader section can be protected on different levels. There are four levels of protection for both sections. A short description of the modes follows.

Table 1. Boot Lock Modes

Mode	Bits	Description
Mode 1	11	Full read/write access

Table 1. Boot Lock Modes

Mode	Bits	Description
Mode 2	10	No write access
Mode 3	00	No write access and no read access (data or interrupt execution) from the other section.
Mode 4	01	No read access (data or interrupt execution) from the other section.

Note that once programmed (cleared), it is impossible to unprogram the bits again without using serial or parallel programming. For instance, to implement an application that is to be updated once, set Boot Lock mode 1 on the Application section, and mode 4 on the Boot Loader section. This prevents the application from accessing the Boot Loader, while giving the Boot Loader full access to update the application section. Once updated, the Boot Loader would set mode 3 on the Application section, thus blocking all further access.

To program the Boot Lock bits, load the R0 Register with the correct bits, set the BLBSET and SPMEN bits in the SPMCR Register and execute the SPM instruction within four cycles. The contents of the Z-register are ignored.

Using the LPM instruction instead of the SPM instruction will read the bits.

Interrupt Considerations

It is possible to use interrupts while writing to the RWW section, but the software must prevent any other access to the RWW section. In other words, interrupt service routines to be executed while updating the RWW section must be placed in the NRWW section, including the Interrupt Vectors.

Using the IVSEL bit in the GICR Register, the application can be used to implement two separate Interrupt Vector tables. One in the Application section, and one in the Boot Loader section to be used when updating the RWW section. This enables the application to continue critical processes, e.g., safety monitoring, during Self-programming. Refer to the devices' data sheet for more details on interrupts and the IVSEL Flag.

If the secondary Interrupt Vectors are not used, the interrupts must be disabled during RWW section updates.

The SPM Interrupt

On all devices supporting Self-programming, except the ATmega163 and ATmega323 devices, it is possible to control the Flash update operations using interrupts. Setting the SPMIE bit in the SPMCR Register will enable the SPM ready interrupt. This can be used to indicate when the current SPM operation is finished.

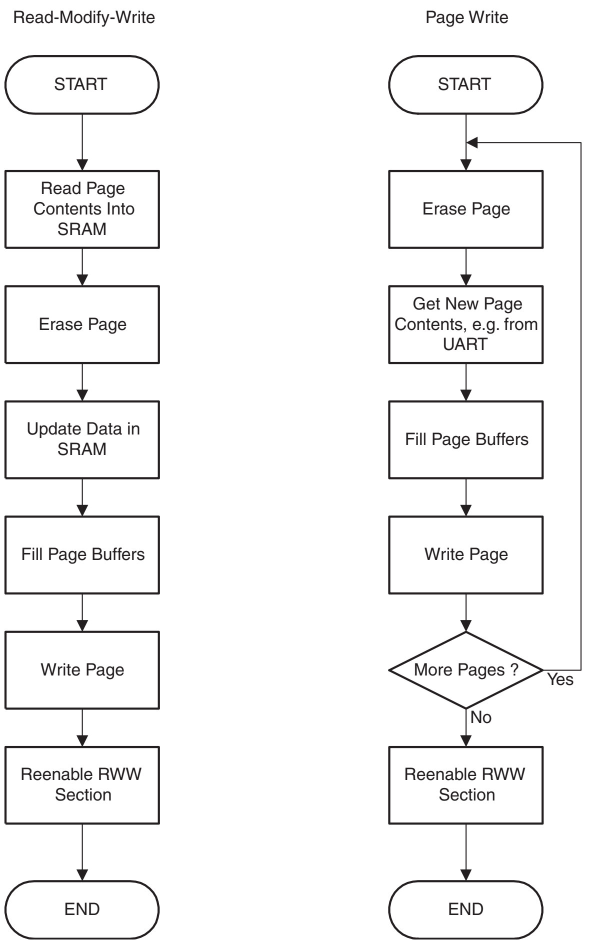
EEPROM Conflicts

Note that all write operations to the EEPROM must be finished before executing the SPM instruction and vice versa. Write/erase of the Flash and EEPROM cannot occur simultaneously.

Typical Update Procedures

Two common update procedures are shown in Figure 6. The flowchart to the left describes a Read-Modify-Write operation used to update small parts of the Flash, e.g., a constant string contained in Flash memory. The flowchart to the right describes a Page Write operation used to write whole pages without reading previous contents, e.g., write data received from an UART.

Figure 6. Typical Update Flowcharts



Boot Loader Example

The Boot Loader software presented in this application note uses the AVR Open Source Programmer (AVROSP) as the user interface. The example application implements functions to read or update the Flash and EEPROM memories on the target device. It is also possible to read and update the Lock bits and read the Fuse bits of the device.

AVRProg Compatibility

AVRProg compatibility relies upon device codes, which are not defined for all devices. The preprocessor.xls file contains the defined device codes, but some are not yet implemented in the AVRProg executable. In this case, use a code from a device with the same memory sizes. AVROSP, on the other hand, relies on signature bytes only, and accepts all devices with self-programming capabilities.

Protocol

The protocol used by the Boot Loader program is a subset of the protocol defined for AVR-Prog. A list of supported commands is shown in Table 2 on page 8. All commands start with a single letter. The programmer returns 13d (carriage return) or the requested data after the command is finished. Unknown commands are replied with a "?".

Table 2. AVRProg Commands

	Host Writes		Host Reads	
	ID	**Data**	**Data**	
Enter Programming Mode	"P"			13d
Auto Increment Address	"a"		dd	
Set Address	"A"	ah al		13d
Write Program Memory, Low Byte	"c"	dd		13d
Write Program Memory, High Byte	"C"	dd		13d
Issue Page Write	"m"			13d
Read Lock Bits	""r"		dd	
Read Program Memory	"R"		2*dd	
Read Data Memory	"d"		dd	
Write Data Memory	"D"	dd		13d
Chip Erase	"e"			13d
Write Lock Bits	"l"	dd		13d
Read Fuse Bits	"F"		dd	
Read High Fuse Bits	"N"		dd	
Read Extended Fuse Bits	"Q"		dd	
Leave Programming Mode	"L"			13d
Select Device Type	"T"	dd		13d
Read Signature Bytes	"s"		3*dd	
Return Supported Device Codes	"t"		n*dd	00d
Return Software Identifier	"S"		s[7]	
Return Software Version	"V"		dd dd	
Return Programmer Type	"p"		dd	
Set LED	"x"	dd		13d

Table 2. AVRProg Commands (Continued)

	Host Writes		Host Reads	
	ID	**Data**	**Data**	
Clear LED	“y”	dd		13d
Exit Bootloader	“E”			13d
Check Block Support	“b”		“Y” 2*dd	
Start Block Flash Load	“B”	2*dd “F” n*dd		13d
Start Block EEPROM Load	“B”	2*dd “E” n*dd		13d
Start Block Flash Read	“g”	2*dd “F”	n*dd	
Start Block EEPROM Read	“g”	2*dd “E”	n*dd	

Program Description

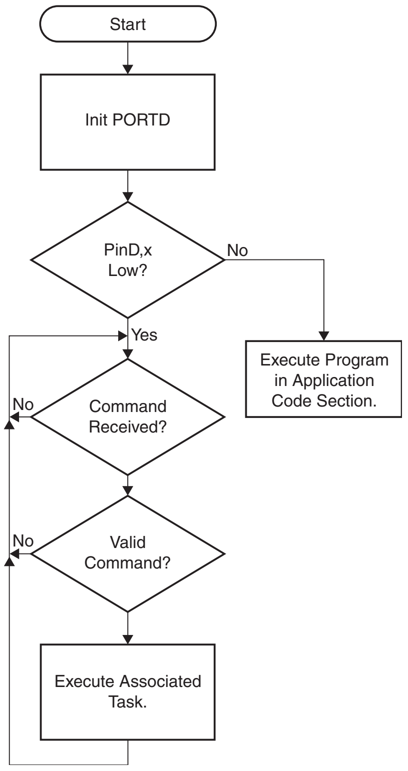
The main program starts by checking if programming is to be done, or if the program in the Application code section is to be executed. In this application, this is indicated by the value of PIND. If a user-specified pin on port D is held low during reset, the program will enter Programming mode. If this pin is high, program execution starts from address $0000 (as if an ordinary reset had occurred).

In Programming mode, the program receives commands from AVROSP via the UART. Each command executes an associated task. Any command not recognized by the boot loader program results in a “?” being sent back to AVROSP. For instructions on how to customize the bootloader for different AVR devices and boot section sizes, refer to the step-by-step instructions in the preprocessor.xls Microsoft Excel file.

Main.c

The main.c program handles communication with the host PC and executes the received commands. Figure 7 shows a flowchart illustrating the operation.

Figure 7. Main Program Execution[1]



Note: 1. As shown in Figure 7, once the Boot Loader routine is entered, the only way to exit is through a reset of the device.

Serial.c

The UART routine (serial.c) implements simple polled UART routines. As described earlier, the reason for doing this polled is that interrupts are not permitted in the Boot section for certain Boot Lock bit settings.

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