Features

- High-performance, Low-power AVR 8-bit XMEGA Microcontroller
- Non-volatile Program and Data Memories
  - 64K/128K/256K Bytes of In-System Self-Programmable Flash
  - 4K/8K/8K Boot Code Section with Independent Lock Bits
  - 2K/2K/4K Bytes EEPROM
  - 4K/8K/16K Bytes Internal SRAM
    - External Bus Interface for SRAM (16 MByte)
    - External Bus Interface for SDRAM (128 Mbit)
- Peripheral Features
  - Four-channel DMA Controller with support for external requests
  - Eight 16-bit Timer/Counters
    - 4 Timer/Counters with 4 Output Compare or Input Capture channels
    - 4 Timer/Counters with 2 Output Compare or Input Capture channels
    - High Resolution Extension on all Timer/Counters
    - Advanced Waveform Extension on 2 Timer/Counters
  - Eight USARTs
  - Four 2-wire Interfaces (I^2C and SMBus compliant)
  - Four SPIs (Serial Peripheral Interfaces)
  - 16-bit Real Time Counter with Separate Oscillator
  - Two Eight-channel, 12-bit, 2 Msps ADCs
  - Two Two-channel, 12-bit, 1 Msps DACs
  - Four Analog Comparators
  - External Interrupts on all General Purpose I/O pins
  - Programmable Watchdog Timer with Separate On-chip Oscillator
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal and External Clock Options with PLL
  - Programmable Multi-level Interrupt Controller
  - Sleep Modes: Idle, Power-down, Standby, Power-save, Extended Standby
  - Advanced Programming, Test and Debugging Interfaces
    - JTAG (IEEE 1149.1 Compliant) Interface for test, debug and programming
    - PDI (Program and Debug Interface) for programming, test and debugging
- I/O and Packages
  - 78 Programmable I/O Lines
  - 100 - lead TQFP
  - 100 - ball CBGA
- Operating Voltage
  - 1.8 – 3.6V
- Speed performance
  - 0 – 12 MHz @ 1.8 – 2.7V
  - 0 – 32 MHz @ 2.7 – 3.6V

Typical Applications

- Industrial control
- Factory automation
- Building control
- Board control
- White Goods
- Climate control
- ZigBee
- Motor control
- Networking
- Hand-held battery applications
- Power tools
- HVAC
- Metering

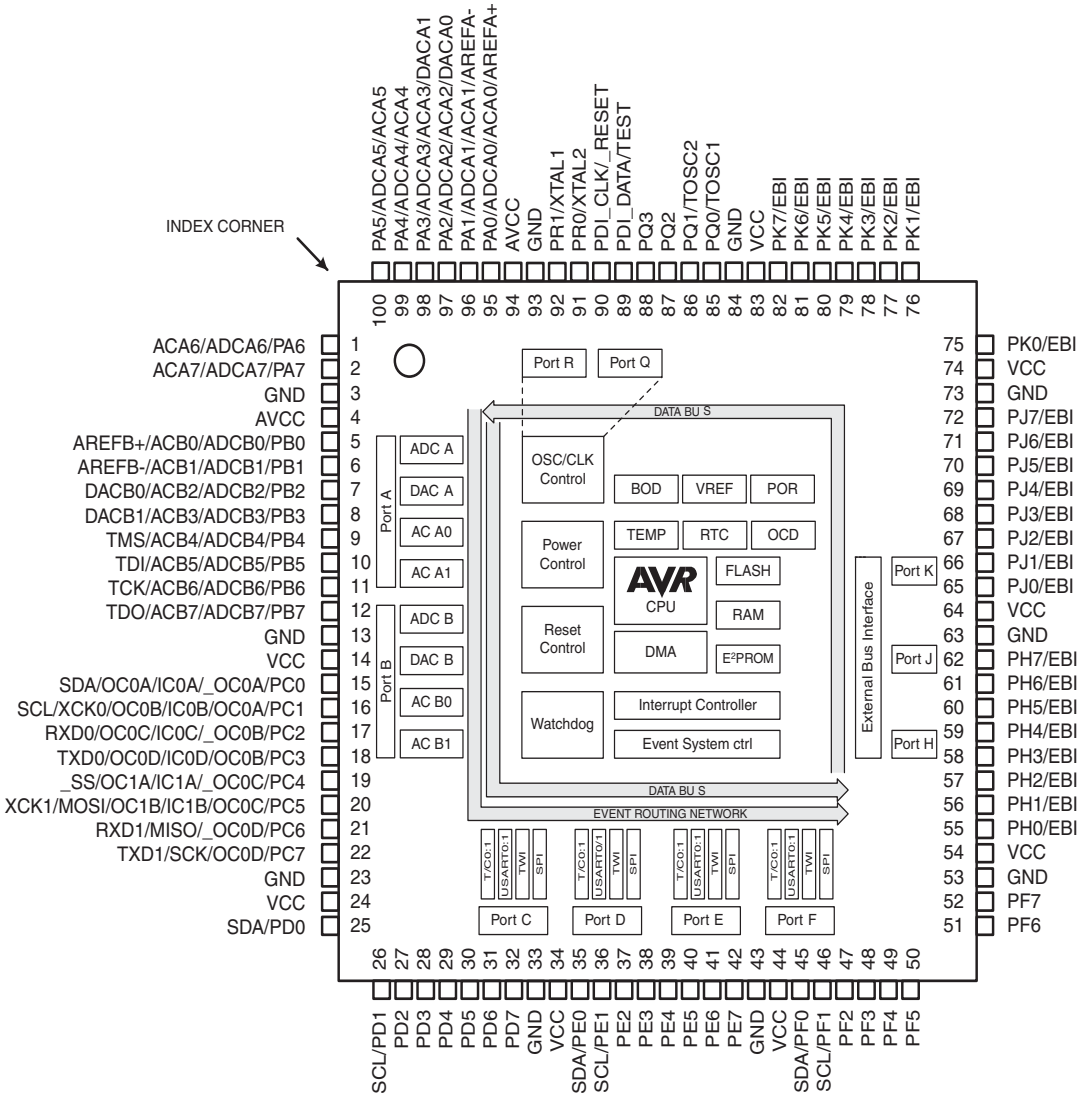
8-bit AVR® XMEGA Microcontroller

ATXMEGA256A1
ATXMEGA128A1
ATXMEGA64A1

Advance Information

8067A–AVR–10/07

Block Diagram/Pinout



Note: 1. The I/O functionalities of Port C, D, E, and F are similar, where Port C is used as a reference in the Pinout figure.

Ordering Information

For packaging information, see “Packaging information” on page 45.

Ordering Code	Flash (B)	E^2 (B)	SRAM (B)	Speed (MHz)	Power Supply	Package[1][2]	Temp
ATXMEGA256A1-AU	256K + 8K	4K	16K	32	1.8 - 3.6V	100A	-40° - 85°
ATXMEGA128A1-AU	128K + 8K	2K	8K	32	1.8 - 3.6V		
ATXMEGA64A1-AU	64K + 4K	2K	4K	32	1.8 - 3.6V		
ATXMEGA256A1-CU	256K + 8K	4K	16K	32	1.8 - 3.6V	100C	
ATXMEGA128A1-CU	128K + 8K	2K	8K	32	1.8 - 3.6V		
ATXMEGA64A1-CU	64K + 4K	2K	4K	32	1.8 - 3.6V		

Note: 1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information.

2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.

1. Overview

The XMEGA A1 is a family of low power, high performance and peripheral rich CMOS 8-bit microcontrollers based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the XMEGA A1 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2. Resources

A comprehensive set of development tools, application notes, and datasheets are available for download on http://www.atmel.com.

2.1 Recommended reading - TBD

- **XMEGA Manual**
- **Application Notes**

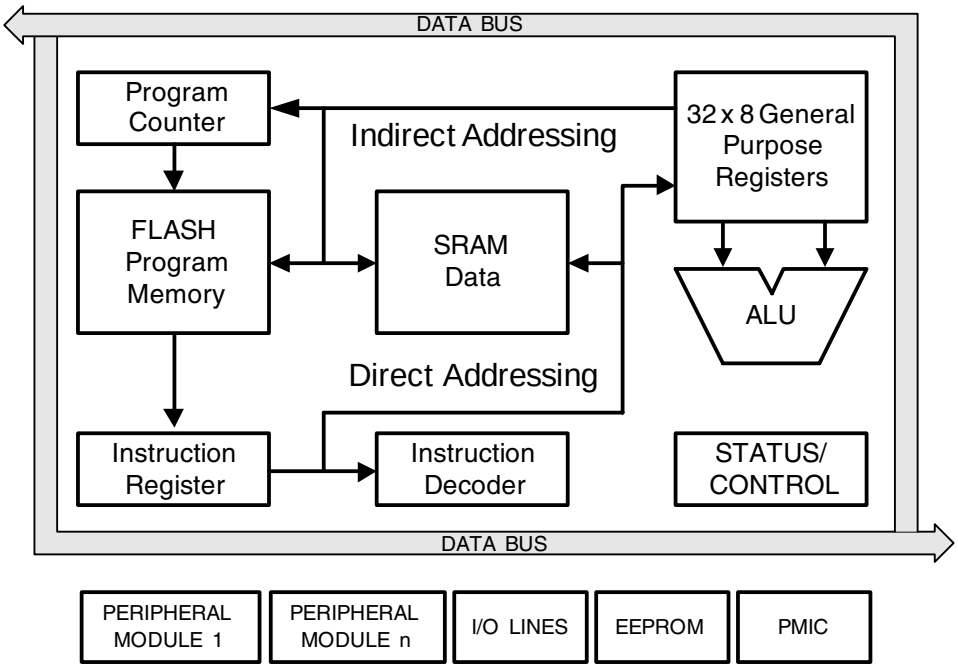
This document contains part specific information only. The XMEGA Manual describes the peripherals in-depth. The application notes contains example code and show applied use of the peripherals.

3. CPU Core

3.1 Overview

The XMEGA A1 uses the 8-bit AVR core. The main function of the CPU core is to ensure correct program execution. The CPU must therefore be able to access memories, perform calculations and control peripherals. Interrupt handling is described in a separate section. Figure 3-1 on page 5 shows the CPU block diagram.

Figure 3-1. CPU block diagram



The AVR uses a Harvard architecture - with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Re-programmable Flash memory.

3.2 Register File

The fast-access Register File contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows single-cycle Arithmetic Logic Unit (ALU) operation. In a typical ALU operation, two operands are output from the Register File, the operation is executed, and the result is stored back in the Register File - in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing - enabling efficient address calculations. One of these address pointers can also be used as an address pointer for look up tables in Flash program memory.

3.3 ALU - Arithmetic Logic Unit

The Arithmetic Logic Unit (ALU) supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic or logic operation, the Status Register is updated to reflect information about the result of the operation.

3.4 Program Flow

Program flow is provided by conditional and unconditional jump and call instructions, able to address the whole address space directly. Most AVR instructions use a 16-bit word format. Some instructions also use a 32-bit format.

The Program Flash memory space is divided in two sections, the Boot section and the Application section. Both sections have dedicated Lock bits for write and read/write protection. The Store Program Memory (SPM) instruction used to access the Application section must reside in the Boot section.

A third section exists inside the Application section. This section, the Application Table section, has separate Lock bits for write and read/write protection. The Application Table section can be used for storing non-volatile data or application software.

The Program Counter (PC) addresses the location from where the instructions are fetched. After a reset, the PC is set to location ‘0’.

During interrupts and subroutine calls, the return address PC is stored on the Stack. The Stack is effectively allocated in the general data SRAM, and consequently the Stack size is only limited by the total SRAM size and the usage of the SRAM. The Stack Pointer (SP) is default reset to the highest address of the internal SRAM. The SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

4. Memories

4.1 Overview

The AVR architecture has two main memory spaces, the Program Memory and the Data Memory. In addition, the XMEGA A1 features an EEPROM Memory for non-volatile data storage. All three memory spaces are linear and require no paging. The memory configurations are shown in "Ordering Information" on page 2.

Non-volatile memory spaces can be locked for further write and read/write operations. This prevents unrestricted access to the application software.

4.2 In-system Programmable Flash Program Memory

The XMEGA A1 contains On-chip In-System Re-programmable Flash memory for program storage, see Table 4-1 on page 7. Since all AVR instructions are 16- or 32-bits wide, each Flash address location is 16 bits.

The XMEGA A1 has additional Boot section for bootloader applications. The Store Program Memory (SPM) instruction used to write to the Flash will only operate from this section. Operation of the SPM is also associated with Boot Lock bits for software protection.

The XMEGA A1 has an Application Table section inside the Application section for storage of Non-volatile data.

Table 4-1. Flash Program Memory (Hexadecimal address)

Word Address				
			0	Application Section (256K/128K/64K)
				...
1EFFF	/ EFFF	/ 77FF		
1F000	/ F000	/ 7800		Application Table Section (8K/8K/4K)
1FFFF	/ FFFF	/ 7FFF		
20000	/ 10000	/ 8000		Boot Section (8K/8K/4K)
20FFF	/ 10FFF	/ 87FF		

The Application Table- and Boot sections can also be used for general application software.

4.3 SRAM Data Memory

The XMEGA A1 has SRAM memory for data storage. The Memory Map for the devices in the family resemble each other, see Table 4-2 on page 8.

4.4 EEPROM Data Memory

The XMEGA A1 has EEPROM memory for non-volatile data storage. It is addressable either in a separate data space or it can be memory mapped the normal data space. The EEPROM memory supports both byte and page access.

The Internal SRAM and EEPROM memory spaces start at the same address in all devices, see Table 4-2 on page 8. The Reserved memory space is empty.

Table 4-2. Data Memory Map (Hexadecimal address)

Byte Address	ATXMEGA256A1	Byte Address	ATXMEGA128A1	Byte Address	ATXMEGA64A1
0	I/O Registers (4KB)	0	I/O Registers (4KB)	0	I/O Registers (4KB)
FFF		FFF		FFF	
1000	EEPROM (4K)	1000	EEPROM (2K)	1000	EEPROM (2K)
1FFF		17FF		17FF	
2000	Internal SRAM (16K)		RESERVED		RESERVED
5FFF		2000	Internal SRAM (8K)	2000	Internal SRAM (4K)
6000	External Memory (0 to 16 MB)	3FFF		2FFF	
FFFFFF		4000	External Memory (0 to 16 MB)	3000	External Memory (0 to 16 MB)
		FFFFFF		FFFFFF	

4.5 I/O Memory

All XMEGA A1 I/Os and peripherals are addressable through I/O memory locations in the data memory space. All I/O locations may be accessed by the LD/LDS/LDD and ST/STS/STD instructions, transferring data between the 32 general purpose registers and the I/O memory.

IN and OUT instructions can address I/O memory locations in the range 0x00 - 0x3F directly.

I/O registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. The value of single bits can be checked by using the SBIS and SBIC instructions in these registers.

The I/O space definition of the XMEGA A1 is shown in “Register Summary - TBD” on page 43.

4.6 EBI - External Bus Interface

- **Supports SRAM up to**
  - **512 KB using 2-port EBI**
  - **16 MB using 3-port EBI**
- **Supports SDRAM up to**
  - **128 Mbit using 3-port EBI (4-bit wide)**
- **Simultaneous support of SRAM and SDRAM**
- **Software configurable Chip Selects**
- **Software configurable Wait State insertion**

The External Bus Interface (EBI) makes it possible to access external memory devices. The XMEGA A1 has 3 ports dedicated to the EBI, making it suited to interface external SRAM, SDRAM, and peripherals such as LCD displays or other memory mapped devices.

5. DMA - Direct Memory Access Controller

5.1 Features

- **Allows High-speed data transfer**
  - **From memory to peripheral**
  - **From memory to memory**
  - **From peripheral to memory**
  - **From peripheral to peripheral**
- **4 Channels**
- **Up to 64K transfers**
- **Multiple addressing modes**
- **1, 2, 4, or 8 bytes Burst Transfers**
- **Programmable priority between channels**

5.2 Overview

The XMEGA A1 has a Direct Memory Access (DMA) controller to move data between memories and peripherals in the data space. The DMA controller uses the same data bus as the CPU to transfer data.

The XMEGA A1 has 4 DMA channels that may be configured independently. The DMA controller supports transfer of up to 64K data blocks and can be configured to access memory with incrementing, decrementing or static addressing.

Since the DMA can access all the peripherals through the I/O memory, the DMA may be used for automatic transfer of data to/from communication modules, as well as automatic data retrieval from ADC conversions or data transfer to DAC conversions.

The DMA controller cannot write to the EEPROM or access the Flash.

6. Event System

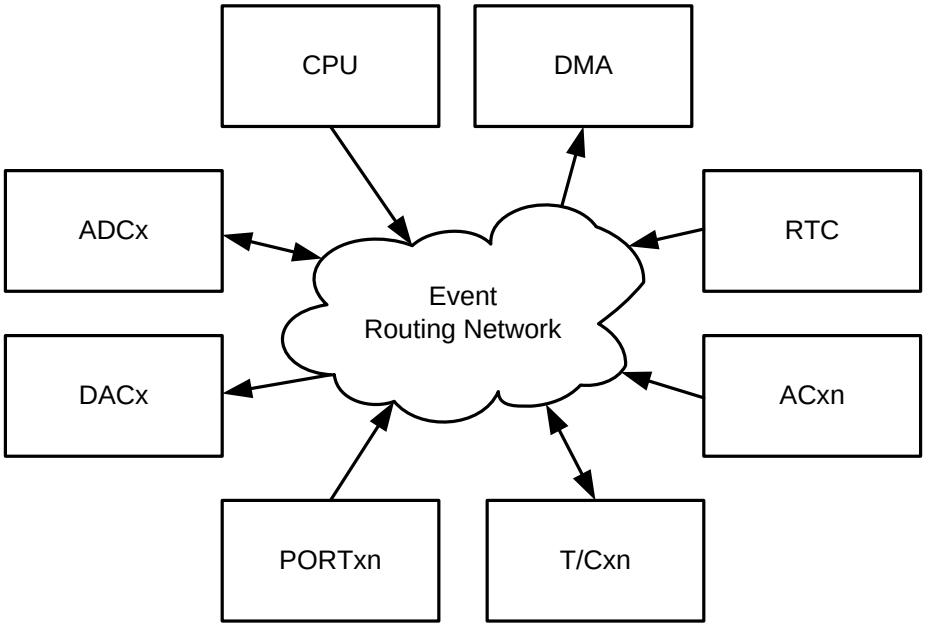
6.1 Overview

The Event System makes connections between the different peripherals. This enables the possibility for one peripheral to trigger actions in other peripherals. It also enables routing of signals between peripherals.

Figure 6-1 on page 11 shows a block diagram of the components that combined form the Eevent system. The event system is not a single entity, but a set of features for inter peripheral communication. This highly flexible system can be used for simple rerouting of pin functions or for sequencing of events.

The event system is functional in both Active- and Idle mode.

Figure 6-1. Event system block diagram.



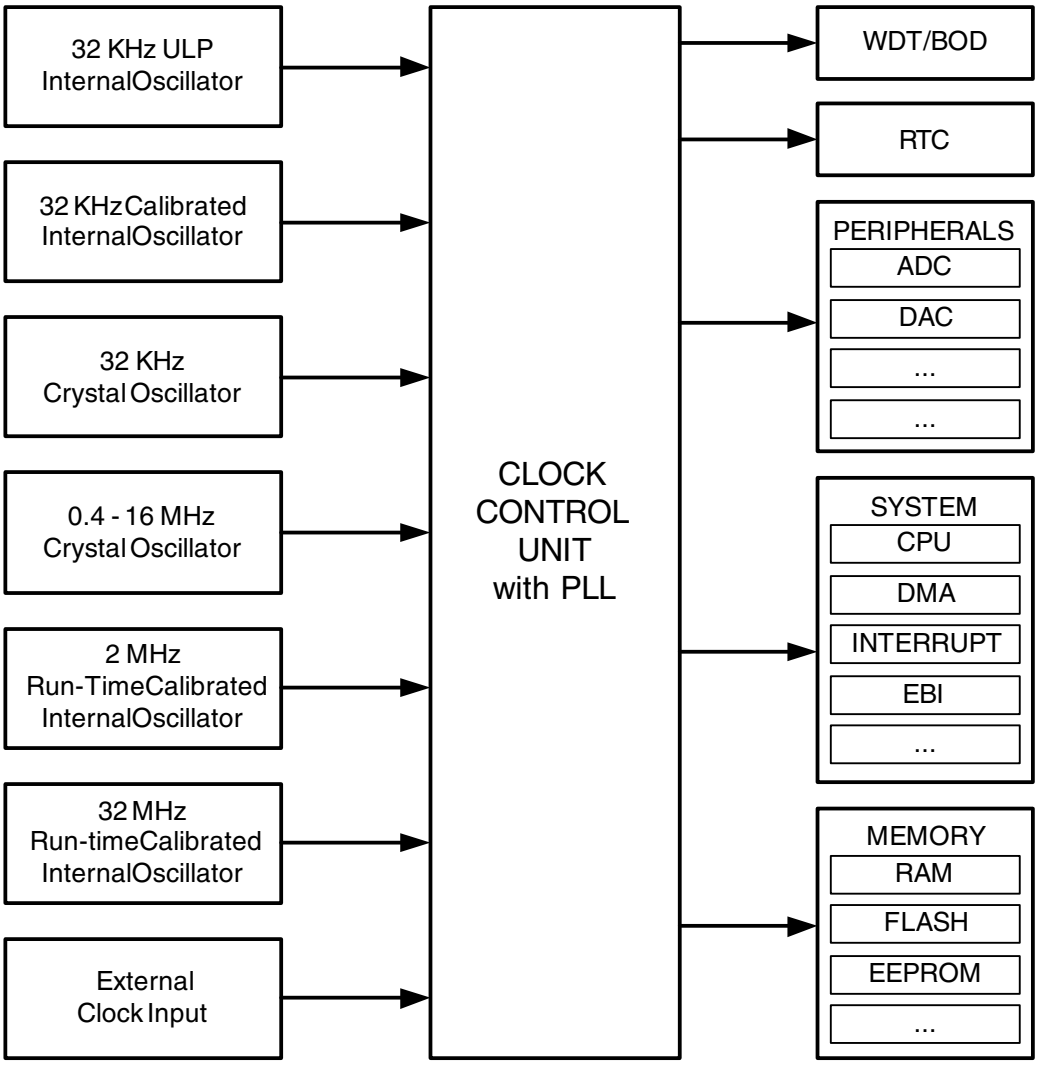
The centerpiece of the event system is the event routing network, which allows events to be passed between peripherals. The the event routing network can directly connect together ADCs, DACs, Analog Comparators (AC), I/O ports (PORT), the Real-time Counter (RTC), and Timer/Counters (T/C). Events can also be generated from software (CPU).

7. System Clock and Clock options

7.1 Overview

The XMEGA A1 has an advanced clock system with multiple clock sources. It incorporates both completely integrated oscillators and external crystal oscillators - and an advanced distribution of the different clock signals. The clock distribution enables the possibility to switch between clock sources from software during run-time. Figure 7-1 on page 12 shows the principal clock system in XMEGA A1.

Figure 7-1. Clock system overview



Each clock source is briefly described in the following sub-sections.

7.2 Clock Options

7.2.1 32 kHz Ultra Low Power Internal Oscillator

The 32 kHz Ultra Low Power (ULP) Internal Oscillator is a very low power consumption clock source based on internal components only. As it is intended mainly for system functions, it should not be used when an accurate clock is required.

7.2.2 32 kHz Calibrated Internal Oscillator

Compared to the internal ULP oscillator, the 32 kHz Calibrated Internal Oscillator is a high accuracy clock source based on internal components only.

7.2.3 32 kHz Crystal Oscillator

The 32 kHz Crystal Oscillator is a low power driver for an external watch crystal.

7.2.4 0.4 - 16 MHz Crystal Oscillator

The 0.4 - 16 MHz Crystal Oscillator is a driver intended both for driving resonators and crystals from 400 kHz to 16 MHz.

7.2.5 2 MHz Run-time Calibrated Internal Oscillator

The 2 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator based on internal components only. The oscillator may use any of the 32 kHz oscillators to calibrate the frequency run-time to compensate for temperature and voltage drift, optimizing the accuracy of the oscillator.

The 2 MHz Clock source can be adjusted between 1.8 - 2.2 MHz and will in combination with the PLL, “PLL with Multiplication factor 2 - 31x” on page 13, provide a wide range of frequencies.

7.2.6 32 MHz Run-time Calibrated Internal Oscillator

The 32 MHz Run-time Calibrated Internal Oscillator is a high frequency oscillator based on internal components only. The oscillator may use any of the 32 kHz oscillators to calibrate the frequency run-time to compensate for temperature and voltage drift, optimizing the accuracy of the oscillator.

7.2.7 External Clock input

The external clock input gives the possibility to connect to a clock from an external source.

7.2.8 PLL with Multiplication factor 2 - 31x

The PLL provides the possibility of multiplying a frequency with any real number from 2 to 31. In combination with some prescalers, this gives a numerous number of clock frequency options to use.

7.2.9 Clock Considerations

In general crystal oscillators provide a more accurate clock source than the internal oscillators. With no external components, the internal oscillators provide a basic clock source for the microcontroller. After characterization of the internal oscillators, typical frequency and performance over temperature and voltage is determined. This data is found in the Electrical Characteristics.

8. Power Management and Sleep Modes

8.1 Introduction

The XMEGA A1 provides various sleep modes tailored to reduce power consumption to a minimum. All sleep modes are accessible from Active mode. In Active mode the CPU is executing application code. The application code decides when and what sleep mode to enter.

Various sources can restore the microcontroller from sleep to Active mode. This is called a wake-up.

8.2 Sleep Modes

The XMEGA A1 has the following sleep modes:

- **Idle**
- **Power-down**
- **Power-save**
- **Standby**
- **Extended Standby**

8.2.1 Idle mode

Halts the CPU and Non-volatile Memories, allowing all peripherals, including the Event System and DMA to run. The device wakes up from any interrupt.

8.2.2 Power-down mode

Halts all clock sources allowing operation of asynchronous modules only. The device wakes up by Pin Change Interrupts, TWI Address-match, Watchdog Reset, Watchdog Interrupt and External Reset.

8.2.3 Power-save mode

The same as Power-down with the exception that if the Real Time Counter is enabled, it will keep running during sleep. Wake-up is identical to Power-down mode, in addition to Real Time Counter interrupts.

8.2.4 Standby mode

Identical with Power-down with the exception that the oscillator oscillators in use are kept running. This ensures fast wake-up.

8.2.5 Extended Standby mode

Identical with Power-save mode with the exception that the oscillators in use are kept running. This ensures fast wake-up.

9. System Control and Reset

9.1 Resetting the AVR

During reset, all I/O Registers are set to their initial values. Application execution starts from the Reset Vector. The instruction placed at the Reset Vector should be a JMP - Absolute Jump - instruction to the reset handling routine. If the application never enables an interrupt source, the Interrupt Vectors are not used. The regular application code can then be placed at these locations. This is also the case if the Reset Vector is in the Application section while the Interrupt Vectors are in the Boot section or vice versa.

The I/O ports of the AVR are immediately tri-stated when a reset source goes active. This does not require any clock source to be running.

9.2 Reset Sources

The reset source can be determined by the application. The XMEGA A1 has the following sources of reset:

- **Power-on Reset**
- **External Reset**
- **Watchdog Reset**
- **Brown-out Reset**
- **JTAG AVR Reset**
- **PDI reset**
- **Software reset**

9.2.1 Power-on Reset

The MCU is reset when the supply voltage VCC is below the Power-on Reset threshold voltage.

9.2.2 External Reset

The MCU is reset when a low level is present on the RESET pin.

9.2.3 Watchdog Reset

The MCU is reset when the Watchdog Timer period expires and the Watchdog Reset is enabled.

9.2.4 Brown-out Reset

The MCU is reset when the supply voltage VCC is below the Brown-out Reset threshold voltage and the Brown-out Detector is enabled.

9.2.5 JTAG AVR Reset

The MCU is reset as long as there is a logic one in the Reset Register, one of the scan chains of the JTAG system. Refer to IEEE 1149.1 (JTAG) Boundary-scan for details.

9.2.6 PDI reset

The MCU may be reset through the Program and Debug Interface (PDI).

9.2.7 Software reset

The MCU may be reset by the CPU writing to a special I/O register.

9.3 WDT - Watchdog Timer

9.3.1 Features

- **Clocked from dedicated on-chip 1 kHz oscillator**
- **Selectable time-out periods from 8 ms to 8s**
- **Protected mechanism for turning on, off or changing settings**
- **Fuse configurable Always-on mode**
- **Window mode**

9.3.2 Overview

The XMEGA A1 has a Watchdog Timer (WDT) that will run continuously when turned on. If the Watchdog Timer is not reset within a software configurable time-out period, the microcontroller will reset. To prevent this reset, a Watchdog Reset (WDR) instruction must be run by software to reset the WDT.

The WDT has a Window mode. In this mode the WDR instruction must be run within a specified period called a window. Application software can set the minimum and maximum limits for this window. If the WDR instruction is not run inside the window limits, the microcontroller will be reset.

The WDT also has an Always-on mode. This mode is enabled by programming a fuse. In Always-on mode, application software can not disable the WDT.

A protection mechanism is used to prevent unwanted enabling, disabling or change of WDT settings.

10. PMIC - Programmable Multi-level Interrupt Controller

10.1 Overview

XMEGA A1 has a Programmable Multi-level Interrupt Controller (PMIC). All peripherals can define three different priority levels for interrupts; high, medium or low. Medium level interrupts may interrupt low level interrupt service routines. High level interrupts may interrupt both low- and medium level interrupt service routines. Low level interrupts have an optional round robin scheme to make sure all interrupts are serviced within a certain amount of time.

A Non-Maskable Interrupt (NMI) can detect oscillator failure.

10.2 Interrupt vectors

When an interrupt is serviced, the program counter will jump to the interrupt vector address. The interrupt vector is the sum of the module or peripherals base address and the specific interrupt's offset address. The base addresses for the XMEGA A1 device is shown in Table 10-1. Offset addresses for each interrupt available in the peripheral are described for each manual in the manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 10-1.

Table 10-1. Reset and Interrupt Vectors

Program Address (Base Address)	Source	Interrupt Definition
0x000	RESET	
0x002	IVEC_XOSCF_INT_vect	Crystal Oscillator Failure Interrupt vector (NMI)
0x004	IVEC_PORTC_INT_base	Port C Interrupt base
0x008	IVEC_PORTR_INT_base	Port R Interruptbase
0x00C	IVEC_DMAC_INT_base	DMA Controller Interrupt base
0x014	IVEC_RTC_INT_base	Real Time Counter Interrupt base
0x018	IVEC_TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	IVEC_TIMERC_INT_base	Timer/Counter C Interrupt base
0x030	IVEC_SPIC_INT_vect	SPI C Interrupt vector
0x032	IVEC_USARTC_INT_base	USART C Interrupt base
0x03E	IVEC_NVM_INT_base	Non-Volatile Memory INT base
0x042	IVEC_PORTB_INT_base	Port B INT base
0x046	IVEC_ACB_INT_base	Analog Comparator Port B INT base
0x04C	IVEC_ADCB_INT_base	Analog to Digital Converter Port B INT base
0x054	IVEC_PORTE_INT_base	Port E INT base
0x058	IVEC_TWIE_INT_base	Two-Wire Interface on Port E INT base
0x05C	IVEC_TIMERE_INT_base	Timer/Counter E Interrupt base
0x070	IVEC_SPIE_INT_vect	SPI E Interrupt vector
0x072	IVEC_USARTE_INT_base	USART E Interrupt base

Table 10-1. Reset and Interrupt Vectors (Continued)

Program Address (Base Address)	Source	Interrupt Definition
0x07E	IVEC_PORTD_INT_base	Port D INT base
0x082	IVEC_PORTA_INT_base	Port A INT base
0x086	IVEC_ACA_INT_base	Analog Comparator Port A INT base
0x08C	IVEC_ADCA_INT_base	Analog to Digital Converter Port A INT base
0x094	IVEC_TWID_INT_base	Two-Wire Interface on Port D INT base
0x098	IVEC_TIMERD_INT_base	Timer/Counter D Interrupt base
0x0AC	IVEC_SPID_INT_vector	SPI D Interrupt vector
0x0AE	IVEC_USARTD_INT_base	USART D Interrupt base
0x0BA	IVEC_PORTQ_INT_base	Port Q INT base
0x0BE	IVEC_PORTH_INT_base	Port H INT base
0x0C2	IVEC_PORTJ_INT_base	Port J INT base
0x0C6	IVEC_PORTK_INT_base	Port K INT base
0x0CE	IVEC_PORTF_INT_base	Port F INT base
0x0D2	IVEC_TWIF_INT_base	Two-Wire Interface on Port F INT base
0x0D6	IVEC_TIMERF_INT_base	Timer/Counter F Interrupt base
0x0EA	IVEC_SPIF_INT_vector	SPI F Interrupt base
0x0EC	IVEC_USARTF_INT_base	USART F Interrupt base

11. I/O Ports

11.1 Introduction

The XMEGA A1 has flexible General Purpose I/O (GPIO) Ports. A port consists of up to 8 pins, ranging from pin 0 to pin 7. The ports implement several functions, including interrupts, synchronous/asynchronous input sensing and configurable output settings. All functions are individual per pin, but several pins may be configured in a single operation.

11.2 I/O configuration

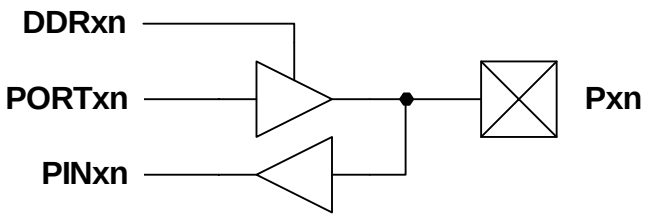
All port pins have programmable output configuration. In addition, all GPIO pins have inverted I/O. For an input, this means inverting the signal between the port pin and the pin register. For an output, this means inverting the output signal between the port register and the port pin. Some port pins also have configurable slew rate limitation to reduce electromagnetic emission.

The configuration options include:

- **Push-pull**
- **Pull-down resistor**
- **Pull-up resistor**
- **Bus keeper**
- **Inverted I/O**
- **Slew rate limitation**

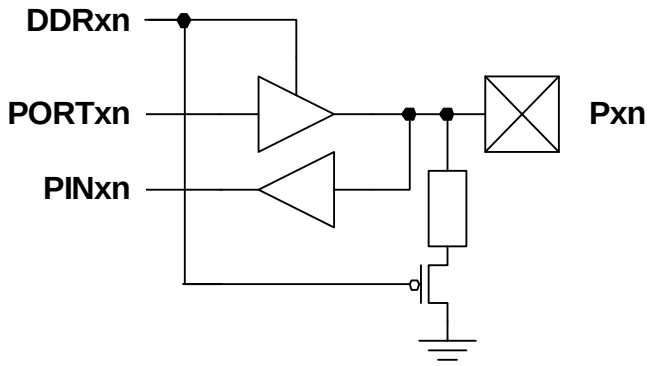
11.3 Push-pull

Figure 11-1. I/O configuration - Totem-pole



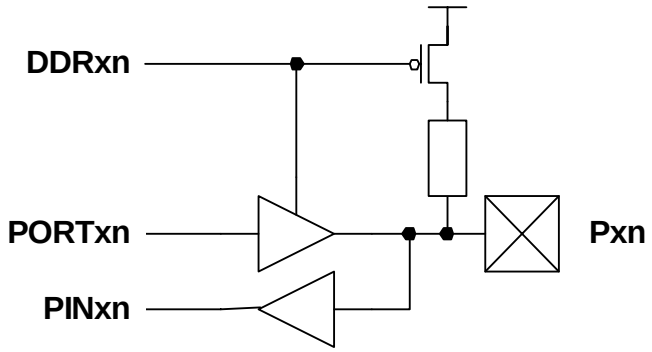
11.4 Pull-down

Figure 11-2. I/O configuration - Totem-pole with pull-down (on input)



11.5 Pull-up

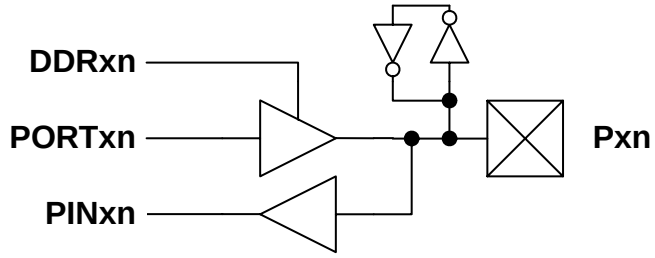
Figure 11-3. I/O configuration - Totem-pole with pull-up (on input)



11.6 Bus-keeper

The bus-keeper's weak output produces the same logical level as the last output level. It acts as a pull-up if the last level was '1', and pull-down if the last level was '0'.

Figure 11-4. I/O configuration - Totem-pole with bus-keeper



11.7 Others

Figure 11-5. Output configuration - Wired-OR with optional pull-down

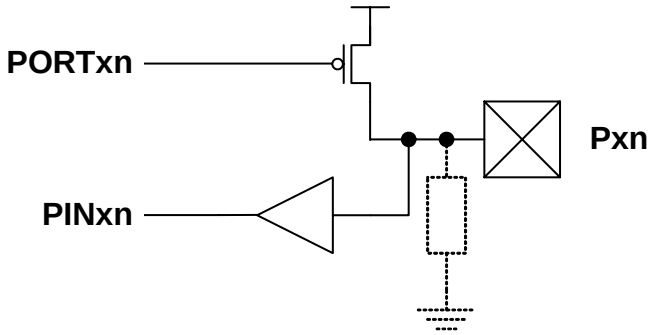
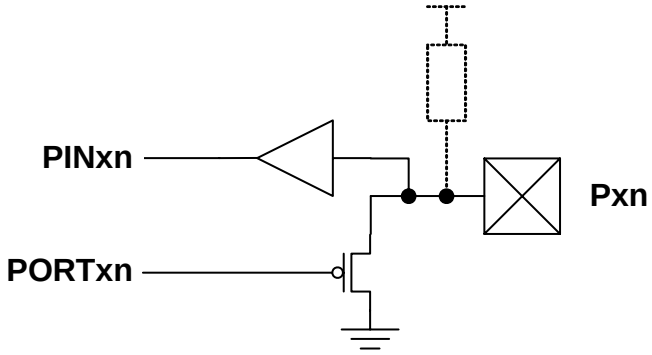


Figure 11-6. I/O configuration - Wired-AND with optional pull-up



11.8 Port Interrupt

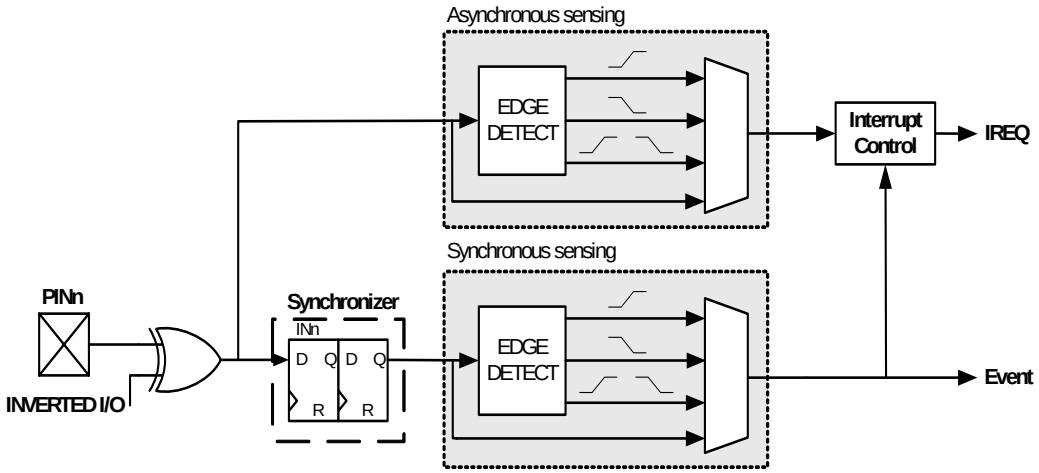
Ports can have pin-change interrupts and external interrupts. Each port supports being the source of two interrupts, and each pin may be configured individually or grouped. Each of the interrupts may be given a specific priority and given specific sense configuration.

11.9 Input sensing

- **Sense both edges**
- **Sense rising edges**
- **Sense falling edges**
- **Sense low level**

The basic input sensing may be synchronous or asynchronous and is built on the configuration shown in Figure 11-7 on page 22.

Figure 11-7. Input sensing system overview



In addition, all GPIO pins may be configured as inverted I/O, meaning that the pin value is inverted before sensing.

12. T/C - 16-bits Timer/Counter

12.1 Features

- 4 Timer/Counter 0 (Timer0)
- 4 Timer/Counter 1 (Timer1)
- True 16-bit Design
- Double Buffered Timer Period Setting
- Compare or Capture Channels are Double Buffered
- 4 Combined Compare or Capture (CC) Channels in Timer0
- 2 Combined Compare or Capture (CC) Channels in Timer1
- Waveform Generation:
  - Single Slope Pulse Width Modulation
  - Dual Slope Pulse Width Modulation
  - Frequency Generation
- Input Capture:
  - Input Capture with Noise Cancelling
  - Frequency capture
  - Pulse width capture
  - 32-bit input capture
- Event Counter with Direction Control
- Timer Overflow and Timer Error Interrupts and Events
- One Compare Match or Capture Interrupt and Event per CC Channel
- Supports DMA Operation
- Hi-Resolution Extension (Hi-Res)
- Advanced Waveform Extension (AWeX)

12.2 Overview

XMEGA A1 has 8 Timer/Counters. 4 are of type Timer0 and 4 of type Timer1. The difference between Timer0 and Timer1 type is that Timer0 has 4 Compare/Capture channels, and Timer1 only has 2. In addition, Timer0 may have an Advanced Waveform Extension (AWeX), that is not available in Timer1.

The Timer/Counters (T/C) are 16-bit and can count any clock, event or input signal in the microcontroller. A programmable prescaler is available to get a useful T/C resolution. Updates of Timer and Compare registers are double buffered to ensure glitch free operation. Using Compare channels many different waveforms can be generated, single slope PWM, dual slope PWM and frequency generation.

The Hi-Resolution Extension can be enabled to increase the waveform generation resolution by 2 bits (4x). This is available for all Timer/Counters.

The Input Capture has a noise canceller to avoid incorrect capture of the T/C. Any input pin or event in the microcontroller can be used to trigger the capture.

A wide range of interrupt or event sources are available, including T/C overflow, Compare match and Capture for each timer and CC channel.

PORTC, PORTD, PORTE and PORTF each has one Timer0 and one Timer1. Notation of these timers are TimerC0, TimerC1, TimerD0, TimerD1, TimerE0, TimerE1, TimerF0, and TimerF1.

13. AWeX – Advanced Waveform Extension

13.1 Features

- **4-DTI Units (8-pin)**
- **8-bit Resolution**
- **Separate High and Low Side Dead-Time Setting**
- **Double Buffered Dead-Time**
- **Fault Protection (Event Controlled)**
- **Single Channel Multiple Output Operation (for BLDC control)**
- **Double Buffered Pattern Generation**

13.2 Overview

The Advanced Waveform Extention (AWeX) provides extra features to the Timer/Counter in Waveform Generation (WG) modes. The AWeX enables easy and robust implementation of for example advanced motor control (AC, BLDC, SR, and Stepper) and power control applications.

Any WG output from the Timer/Counter 0 are split into a complimentary pair of outputs when any AWeX features is enabled. These output pairs go through a Dead-Time Insertion (DTI) unit that enables generation of the non-inverted Low Side (LS) and inverted High Side (HS) of the WG output with dead time insertion between LS and HS switching. The DTI output will override the normal port value according to the port override setting. Optionally the final output can be inverted by using the invert I/O (INVEN) bit setting for the port pin (Pxn).

The Pattern Generation unit can be used to generate a synchronized bit pattern on the port it is connected to. In addition, the waveform generator output from the Compare Channel A can be distributed to and override all the port pins. When the Pattern Generator unit is enabled the DTI unit is bypassed.

The Fault Protection unit is connected to the Event System, enabling any event to trigger a fault condition that will disable the AWeX output.

The AWeX is only available on TimerC0 and TimerE0.

14. RTC - Real-Time Counter

14.1 Features

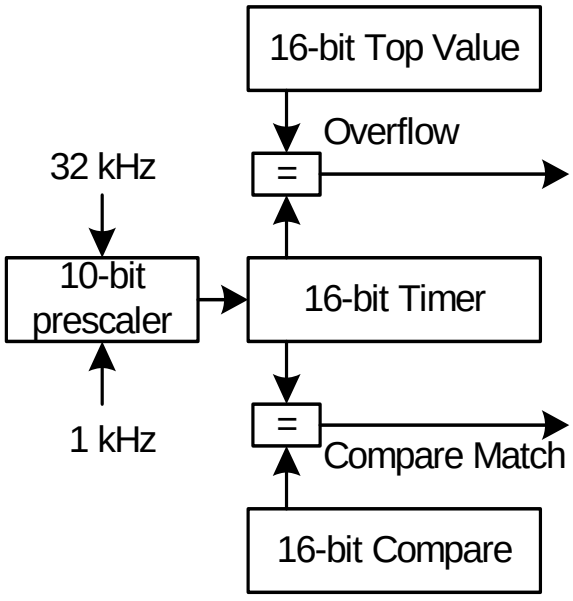
- **16-bit Timer**
- **Flexible Tick resolution ranging from 1 Hz to 32 kHz**
- **1 Compare register**
- **1 Top Value register**
- **Clear timer on Overflow or Compare Match**
- **Overflow or Compare Match event and interrupt generation**

14.2 Overview

The XMEGA A1 includes a Real-time Counter (RTC). It should be clocked by an 32.768 kHz crystal oscillator. The RTC may also be clocked by the internal 32 kHz RC- or crystal oscillators, or an external clock signal. See Figure 14-1 on page 25.

A wide range of Resolution and Time-out periods can be configured using the RTC. With a maximum resolution of 30.5 µs, time-out periods range up to 2000 seconds. With a resolution of 1 second, maximum time-out period is over 18 hours (65536 seconds).

Figure 14-1. Real-time Counter overview



15. TWI - 2-wire Serial Interface

15.1 Features

- 4 Identical TWI peripherals
- Simple yet Powerful and Flexible Communication Interface
- Both Master and Slave Operation Supported
- Device can Operate as Transmitter or Receiver
- 7-bit Address Space Allows up to 128 Different Slave Addresses
- Multi-master Arbitration Support
- Up to 400 kHz Data Transfer Speed
- Slew-rate Limited Output Drivers
- Noise Suppression Circuitry Rejects Spikes on Bus Lines
- Fully Programmable Slave Address with General Call Support
- Address Recognition Causes Wake-up when in Sleep Mode
- I^2C and System Management Bus (SMBus) compliant

15.2 Overview

The 2-wire Serial Interface (TWI) is a bi-directional bus with only two lines, the clock (SCL) and the data (SDA). The protocol makes it possible to interconnect up to 128 individually addressable devices. Since it is a multi-master bus, one or more devices capable of taking control of the bus, can be connected.

The only external hardware needed to implement the bus is a single pull-up resistor for each of the TWI bus lines. Mechanisms for resolving bus contention are inherent in the TWI protocol.

PORTC, PORTD, PORTE, and PORTF each have one TWI. Notation of these peripherals are TWIC, TWID, TWIE, and TWIF.

16. SPI - Serial Peripheral Interface

16.1 Features

- 4 Identical SPI peripherals
- Full-duplex, Three-wire Synchronous Data Transfer
- Master or Slave Operation
- LSB First or MSB First Data Transfer
- Seven Programmable Bit Rates
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Wake-up from Idle Mode
- Double Speed (CK/2) Master SPI Mode

16.2 Overview

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between different devices. Devices can communicate using a master-slave scheme, and data are transferred both to and from the devices simultaneously.

PORTC, PORTD, PORTE, and PORTF each have one SPI. Notation of these peripherals are SPIC, SPID, SPIE, and SPIF.

17. USART

17.1 Features

- 8 Identical USART peripherals
- Full Duplex Operation (Independent Serial Receive and Transmit Registers)
- Asynchronous or Synchronous Operation
- Master or Slave Clocked Synchronous Operation
- High-resolution Arithmetic Baud Rate Generator
- Supports Serial Frames with 5, 6, 7, 8, or 9 Data Bits and 1 or 2 Stop Bits
- Odd or Even Parity Generation and Parity Check Supported by Hardware
- Data OverRun Detection
- Framing Error Detection
- Noise Filtering Includes False Start Bit Detection and Digital Low Pass Filter
- Three Separate Interrupts on TX Complete, TX Data Register Empty and RX Complete
- Multi-processor Communication Mode
- Double Speed Asynchronous Communication Mode
- IrDA

17.2 Overview

The Universal Synchronous and Asynchronous serial Receiver and Transmitter (USART) provides highly flexible serial communication device. The frame format can be customized to support a wide range of standards, and the USART implements different error detection.

PORTC, PORTD, PORTE, and PORTF each have two USARTs. Notation of these peripherals are USARTC0, USARTC1, USARTD0, USARTD1, USARTE0, USARTE1, USARTF0, USARTF1.

17.3 IRCOM - IR Communication Module

- IrDA 1.4 Compatible
- Supporting baud rates up to 115.2 kbps
- Selectable pulse modulation scheme
  - 3/16 of baud rate period
  - Fixed pulse period, 8-bit programmable
- Flexible 8-bit input filtering

IrDA is only available on one USART at the time.

18. ADC - 12-bit Analog to Digital Converter

18.1 Features

- **Two ADCs with 12-bit resolution**
- **2 Msps conversion rate**
- **Signed- and Unsigned conversions**
- **4 result registers with individual input channel control for each ADC**
- **16 single ended inputs**
- **16x8 differential inputs**
- **Gain of 1, 2, 4, 8, 16, 32 or 64**
- **Selectable accuracy of 8- or 12-bit.**
- **Built-in Gain Calibration**
- **Internal- or External Reference selection**
- **Event triggered conversion for accurate timing**
- **DMA transfer of conversion results**
- **Interrupt/Event on compare result**

18.2 Overview

The XMEGA A1 devices has two Analog to Digital Converters (ADC), see Figure 18-1 on page 30. The two ADC modules can be operated simultaneously, individually or synchronized.

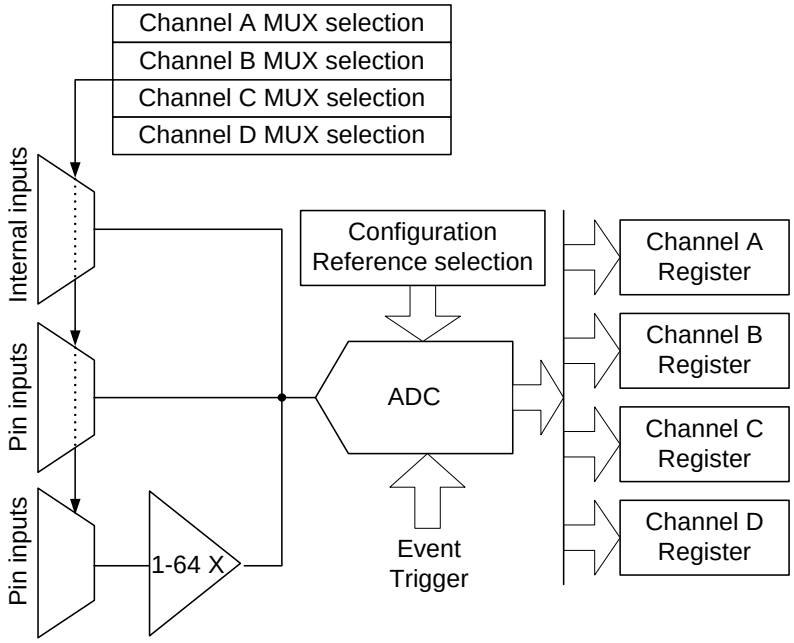
The ADC converts analog voltages to digital values. The ADC has 12-bit resolution and is capable of converting up to 2 million samples per second. The input selection is flexible, and both single-ended and differential measurements can be done. The ADC can provide both signed and unsigned results, and an optional gain stage is available to increase the dynamic range of the ADC.

This is a Successive Approximation Result (SAR) ADC. A SAR ADC measures one bit of the conversion result at a time. The ADC has a pipeline architecture. This means that a new analog voltage can be sampled and a new ADC measurement started while other ADC measurements are ongoing.

ADC measurements can either be started by application software or an incoming event from another peripheral in the device. Four different result registers with individual channel selection (MUX registers) are provided to make it easier for the application to keep track of the data. It is also possible to use DMA to move ADC results directly to memory or peripherals.

Both internal and external analog reference voltages can be used. A very accurate internal 1.0V reference is available, providing a conversion range from -0.5 to 0.5V in unsigned mode and -1.0 to 1.0V in signed mode.

Figure 18-1. ADC overview



Each ADC has 4 registers defining a MUX selection with a corresponding result register. This means that 4 channels may be sampled within 1.5 µs without any intervention by the application other than starting the conversion, and the result will be available in 4 data registers.

The ADC may be configured to make 8- or 12-bit results, reducing the conversion time (propagation delay) from 4 µs for 12-bit to 3 µs for 8-bit resolution.

ADC conversion results are provided left- or right adjusted with optional ‘1’ or ‘0’ padding. This eases calculation when the result is represented as a signed integer (signed 16-bit number).

PORTA and PORTB each have one ADC. Notation of these peripherals are ADCA and ADCB.

19. DAC - 12-bit Digital to Analog Converter

19.1 Features

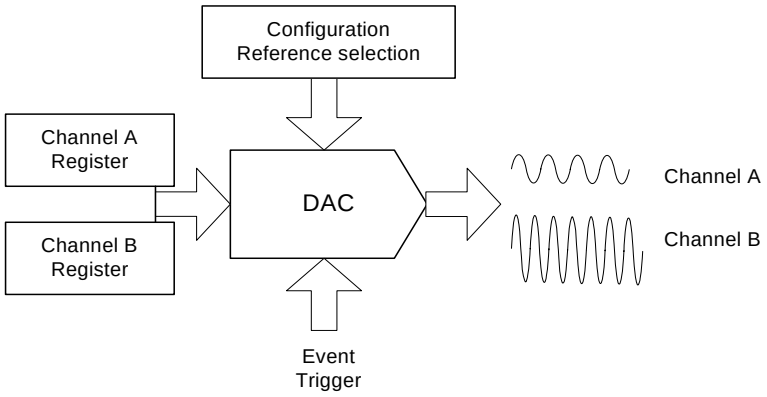
- **Two DACs with 12-bit resolution**
- **Up to 1 Msps conversion rate**
- **Flexible conversion range**
- **Multiple trigger sources**
- **1 continuous time or 2 Sample and Hold (S/H) outputs for each DAC**
- **Built-in offset and gain calibration**
- **High drive capabilities**
- **DAC Power reduction mode**

19.2 Overview

The XMEGA A1 features two 12-bit, 1 Msps DAC with built-in calibration of offset and gain, see Figure 19-1 on page 31.

A DAC converts a digital value into an analog signal. The DAC may use the bandgap reference voltage as upper limit for conversion, but it is also possible to use the supply voltage or any applied voltage in-between. An external reference input is shared with the ADC reference input.

Figure 19-1. DAC overview



Each DAC has one continuous output with high drive capabilities for both resistive and capacitive loads. It is also possible to split the continuous time channel into two Sample and Hold (S/H) channels; each with separate data conversion registers.

A DAC conversion may be started from the application software by writing the data conversion registers. The DAC may also be configured to do conversions triggered by the Event System to have regular timing independent of the application. DMA may be used for transferring data from memory location to DAC data registers.

A DAC power reduction mode can be enabled to reduce power consumption.

The DAC has a built-in calibration system that removes offset and gain error.

PORTA and PORTB each have one DAC. Notation of these peripherals are DACA and DACB.

20. AC - Analog Comparator

20.1 Features

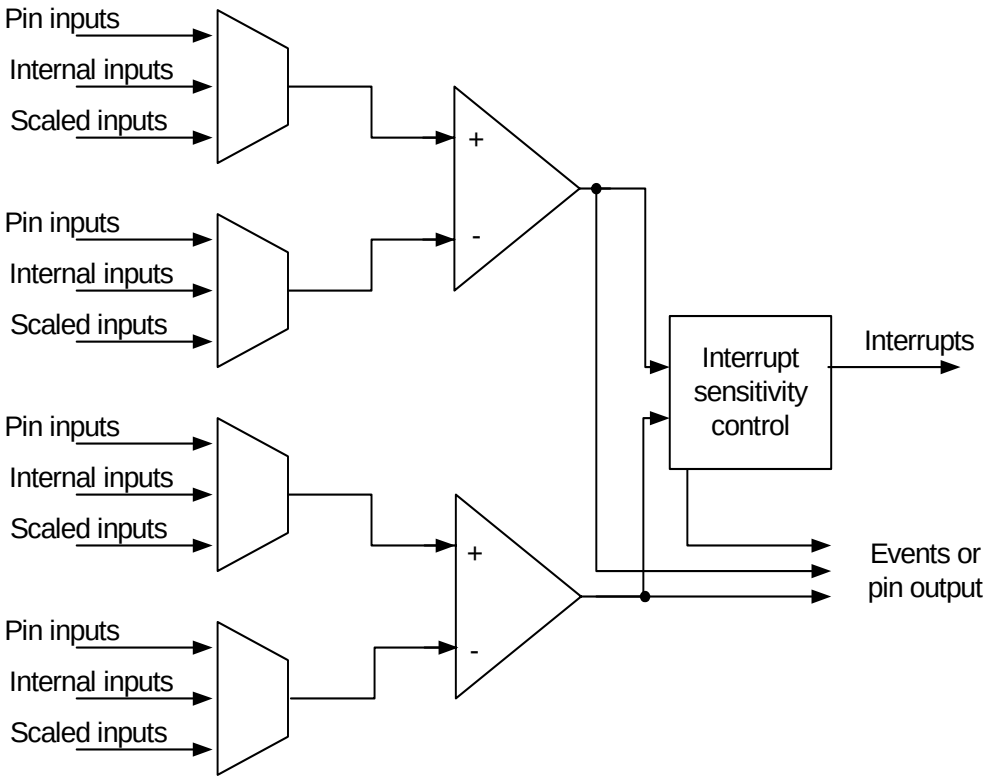
- 4 Analog Comparators
- Selectable Power vs. Speed
  - 20 µA/500 ns active current consumption/propagation delay or
  - 130 µA/30 ns active current consumption/propagation delay
- Selectable hysteresis
  - 0, 20 mV, 50 mV
- Analog Comparator output available on pin
- Flexible Input Selection
- Basic interrupt and event generation on
  - Rising edge
  - Falling edge
  - Toggle
- Window function interrupt and event generation on
  - Signal above window
  - Signal inside window
  - Signal below window

20.2 Overview

The XMEGA A1 features four Analog Comparators (AC). An Analog Comparator compares two voltages, and the output indicates which input is largest.

PORTA and PORTB each have one AC. Notations are ACA0, ACA1, ACB0, and ACB1.

Figure 20-1. Analog comparator overview



20.3 Input Selection

The Analog comparators are organized in pairs, one pair in each analog port.

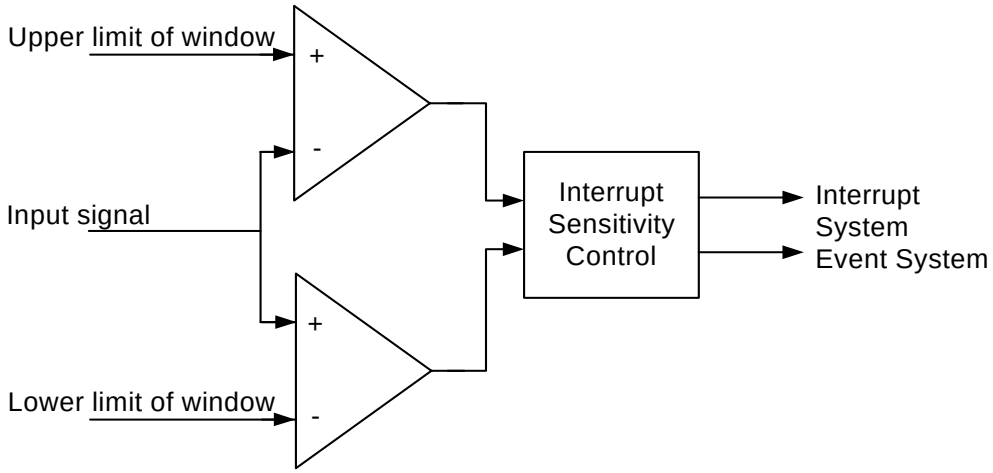
The Analog comparators have a very flexible input selection and the two comparators grouped in a pair may be used to realize a window function. One pair of analog comparators is shown in Figure 20-1 on page 33.

- **Input selection from pin**
  - **Pin 0, 1, 2, 4, 6 selectable to positive input of analog comparator**
  - **Pin 0, 1, 3, 5, 7 selectable to negative input of analog comparator**
- **Internal signals available on both analog comparator inputs**
  - **Bandgap Reference voltage**
  - **Output from 12-bit DAC**
- **6-bit scale down of VCC, available on both analog comparator inputs**

20.4 Window Function

The window function is realized by connecting the inputs of the two analog comparators in a pair as shown in Figure 20-2 on page 34.

Figure 20-2. Analog comparator window function



21. OCD - On-chip Debug

21.1 Features

- Complete Program Flow Control
  - Symbolic Debugging Support in Hardware
  - Go, Stop, Reset, Step into, Step over, Step out, Run-to-Cursor
- 1 dedicated program address breakpoint or symbolic breakpoint for AVR studio/emulator
- 4 Hardware Breakpoints
- Unlimited Number of User Program Breakpoints
- Uses CPU for Accessing I/O, Data, and Program
- Non-Intrusive Operation
  - Uses no hardware or software resources
- High Speed Operation
  - No limitation on frequency of TCK versus system clock frequency

21.2 Overview

The XMEGA A1 has an On-chip debug (OCD) system that - in combination with Atmel's development tools - provides all the necessary functions to debug an application.

22. Program, Debug and Test Interfaces

22.1 Features

- **JTAG Interface (IEEE std. 1149.1 compliant)**
- **PDI - Program and Debug Interface (Atmel proprietary 2-pin interface)**
- **Boundary-scan capabilities according to the IEEE Std. 1149.1 (JTAG)**
- **Access to the OCD system**
- **Programming of Flash, EEPROM, Fuses and Lock Bits**

22.2 Overview

The JTAG and PDI are the physical interface to access the programming and debug facilities. The PDI uses one dedicated pin together with the Reset pin, no general purpose pins are used. When JTAG is ussed it makes use o four general purpose pins.

22.3 JTAG interface

The JTAG physical layer handles the basic low-level serial communication over four I/O lines named TMS, TCK, TDI, and TDO. It complies to the IEEE Std. 1149.1 for test access port and boundary scan.

22.4 PDI - Program and Debug Interface

The PDI is an Atmel proprietary protocol for communication between the microcontroller and Atmel's development tools.

23. Pinout

The pinout of XMEGA A1 is shown in “Block Diagram/Pinout” on page 2.

23.1 Alternate Port Functions

In addition to general I/O functionality, some port pins have alternate functions as described in this section. See “Block Diagram/Pinout” on page 2 and specific module datasheets for complete information.

23.1.1 Operation/Power Supply

VCC	Digital supply voltage
AVCC	Analog supply voltage
GND	Ground

23.1.2 Analog functions

ACxy	Analog Comparator input port x pin y
ADCxy	Analog to Digital Converter input port x pin y
DACxy	Digital to Analog Converter output port x pin y
AREFx+	Positive Analog Reference port x
AREFx-	Negative Analog Reference port x

23.1.3 EBI functions

Ax	Address	
Dx	Data	
_CSx	Chip Select	
ALEx	Address Latch Enable pin x	(SRAM)
_RE	Read Enable	(SRAM)
_WE	External Data Memory Write	(SRAM /SDRAM)
Bx	Bank Address	(SDRAM)
_CAS	Column Access Strobe	(SDRAM)
CKE	SDRAM Clock Enable	(SDRAM)
CLK	SDRAM Clock	(SDRAM)
DQM	Data Mask Signal/Output Enable	(SDRAM)
_RAS	Row Access Strobe	(SDRAM)

23.1.4 Timer functions

OCxn	Output Compare Channel x for Timer n
_OCxn	Inverted Output Compare Channel x for Timer n
ICxn	Input Capture Channel x for Timer n

23.1.5 Communication functions

SCL	Serial Clock for TWI
SDA	Serial Data for TWI
XCK0	Transfer Clock for USART n
RxD0	Receiver Data for USART n
TxD0	Transmitter Data for USART n
_SS	Slave Select for SPI
MOSI	Master Out Slave In for SPI
MISO	Master In Slave Out for SPI
SCK	Serial Clock for SPI

23.1.6 Oscillators

TOSCx	Timer Oscillator pin x
XTALx	Input/Ouptut to inverting Oscillator

23.1.7 DEBUG/SYSTEM functions

TEST	Test pin
PROG	Programming pin
RESET	Reset pin
PDI_CLK	Program and Debug Interface Clock
PDI_DATA	Program and Debug Interface Data
TCK	JTAG Test Clock
TDI	JTAG Test Data In
TDO	JTAG Test Data Out
TMS	JTAG Test Mode Select

24. Electrical Characteristics - TBD

24.1 Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin with respect to Ground	-0.5V to V_{CC}+0.5V
Maximum Operating Voltage	3.6V
DC Current per I/O Pin	20.0 mA
DC Current V_{CC} and GND Pins	200.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

24.2 DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 1.8V to 3.6V (unless otherwise noted)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage, except XTAL1 pin					V
V_{IL1}	Input Low Voltage, XTAL1 pins					V
V_{IH}	Input High Voltage, except XTAL1 pin					V
V_{IH1}	Input High Voltage, XTAL1 pin					V
V_{OL}	Output Low Voltage					
V_{OH}	Output High Voltage					
I_{IL}	Input Leakage Current I/O Pin					µA
I_{IH}	Input Leakage Current I/O Pin					µA
R_{RST}	Reset Pull-up Resistor					kΩ
R_{PU}	I/O Pin Pull-up Resistor					kΩ
I_{CC}	Power Supply Current	Active 32 MHz				mA
		Active 20 MHz				mA
		Active 8MHz				mA
		Idle 32 MHz				mA
		Idle 20 MHz				mA
	Power-down mode	WDT disabled				µA
		WDT slow sampling				µA
		WDT fast sampling				

Note: 1. “Max” means the highest value where the pin is guaranteed to be read as low
2. “Min” means the lowest value where the pin is guaranteed to be read as high

24.3 ADC Characteristics – TBD

Table 24-1. ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution					LSB
	Integral Non-Linearity (INL)					LSB
	Differential Non-Linearity (DNL)					LSB
	Gain Error					LSB
	Offset Error					LSB
	Conversion Time					µs
	ADC Clock Frequency					MHz
	DC Supply Voltage					mA
	Source Impedance					Ω
	Start-up time					µs
AVCC	Analog Supply Voltage		VCC - 0.3		VCC + 0.3	V

Table 24-2. ADC Gain Stage Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Gain					
	Input Capacitance					pF
	Offset Error					mV
	Gain Error					%
	Signal Range					V
	DC Supply Current					mA
	Start-up time					# clk cycles

24.4 DAC Characteristics – TBD

Table 24-3. DAC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution					LSB
	Integral Non-Linearity (INL)					LSB
	Differential Non-Linearity (DNL)					LSB
	Gain Error					LSB
	Offset Error					LSB
	Calibrated Gain/Offset Error					LSB
	Output Range					V
	Output Settling Time					µs
	Output Capacitance					nF
	Output Resistance					kΩ
	Reference Input Voltage					V
	Reference Input Capacitance					pF
	Reference Input Resistance					kΩ
	Current Consumption					mA
	Start-up time					µs

24.5 Analog Comparator Characteristics – TBD

Table 24-4. Analog Comparator Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Offset					mV
	Hysteresis	No				mV
		Low				
		High				
	Propagation Delay	High Speed mode				ns
		Low power mode				
	Current Consumption	High Speed mode				µA
		Low power mode				
	Start-up time					µs

25. Typical Characteristics - TBD

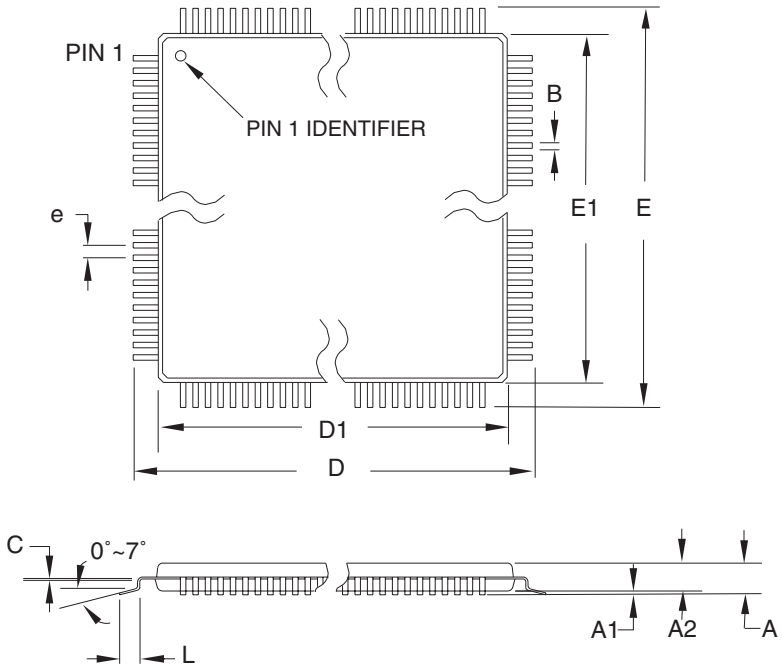
26. Register Summary - TBD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page

27. Packaging information

27.1 100A



COMMON DIMENSIONS
(Unit of Measure = mm)

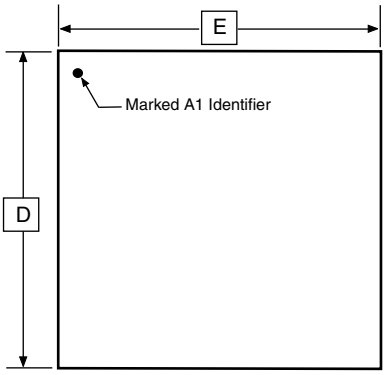
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

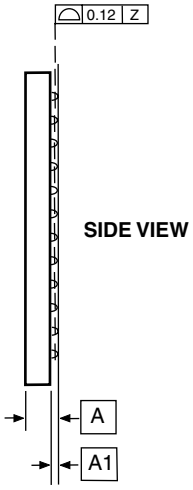
10/5/2001

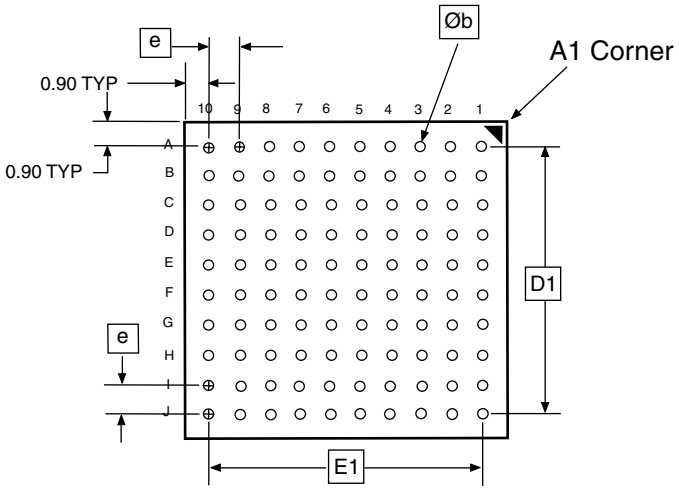
	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100A,** 100-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.5 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	C

27.2 100C



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.10	–	1.20	
A1	0.30	0.35	0.40	
D	8.90	9.00	9.10	
E	8.90	9.00	9.10	
D1	7.10	7.20	7.30	
E1	7.10	7.20	7.30	
Øb	0.35	0.40	0.45	
e	0.80 TYP			

5/25/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100C1**, 100-ball, 9 x 9 x 1.2 mm Body, Ball Pitch 0.80 mm Chip Array BGA Package (CBGA)	100C1	A

28. Datasheet Revision History

28.1 Rev A

1) Initial version.

Table of Contents

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
avr@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature