Features

- **Host Interface**
  - **ATAPI Compatible (ANSI ATA-1, ATA-2, ATA-3 and ATA-4 compliant) Host Mode**
  - **Ultra DMA Support (66 MB/sec)**
  - **High-current (12 mA) Drivers for Direct Connection to AT Cable (slew rate controlled)**
  - **256-byte Bidirectional Data FIFO to Improve Throughput**
- **Embedded Processor**
  - **ARM7TDMI™ RISC Processor**
  - **Open Processor Architecture Protects Firmware Investment**
  - **Wide Selection of Development Tools from ARM® and Third-party Vendors**
  - **1-Mbyte External Flash Interface for Code/Data**
  - **16-Kbyte Internal SRAM for Data**
- **Buffer Manager**
  - **Supports SDRAM up to 32 Mbytes (16M x 16)**
  - **DRAM Bandwidth of up to 160 Mbytes/sec (burst)**
  - **Priority Buffer Arbiter**
- **Read Channel Interface**
  - **Nibble Interface Speed (code cell rate): 40 MHz (160 Mbs, DVD 5X)**
  - **EFM (8/14) and EFM+ (8/16) Demodulation**
- **Write Channel Interface**
  - **Serial Interface Speed (code cell rate): DVD 2X**
  - **EFM (8/14) and EFM+ (8/16) Modulation**
  - **DVD-R Pre-pit Decoder with Error Detection and Correction**
  - **DVD+RW ADIP Decoder with Error Detection and Correction**
  - **CD-R/RW ATIP Decoder with Error Detection**
- **Error Correction Logic**
  - **DVD Data Block Error Detection and Correction**
  - **DVD EDC Error Detection**
  - **DVD IEC Header Error Detection and Correction**
  - **All CD Formats**
- **Lower Power Operation with 3.3V Core and 5V Tolerant I/Os**

Description

The Atmel AT78C1501 is a high-performance DVD/CD ATAPI Ultra DMA66 Interface Controller, designed to interface to the AT78C1502 DVD Servo Controller, the AT78C1503 DVD Read Channel and the AT78C1504 Automatic Laser Power Control (ALPC). The interface controller (AT78C1501) contains ARM® and AVR® microcontrollers, buffer management, error correction code (ECC) and encoder/decoder (ENDEC) for DVD and CD. Also included are a writeable control store for timing generation and an on-board frequency synthesizer to generate system frequencies from one crystal. ATA66/ATAPI66 and I2S interfaces are provided.

The major functions of the AT78C1501 include data format encoding/decoding, error detection/correction, buffer management, ATAPI host interface and serial interface master. The AT78C1501 also includes an embedded ARM7 RISC Core to perform all system (drive) microprocessor functions and an embedded AVR RISC core to perform internal data path and buffer management control.

The AT78C1501 disk formats include DVD-ROM, DVD-RAM (Read/Write), CD-ROM, CD-R (Read/Write), CD-RW (Read/Write), DVD-R (Read/Write), DVD-RW (Read/Write), and DVD+RW (Read/Write).

DVD/CD ATAPI Controller

AT78C1501

Rev. 2049A–DVD–07/02

Figure 1. DVD System Block Diagram

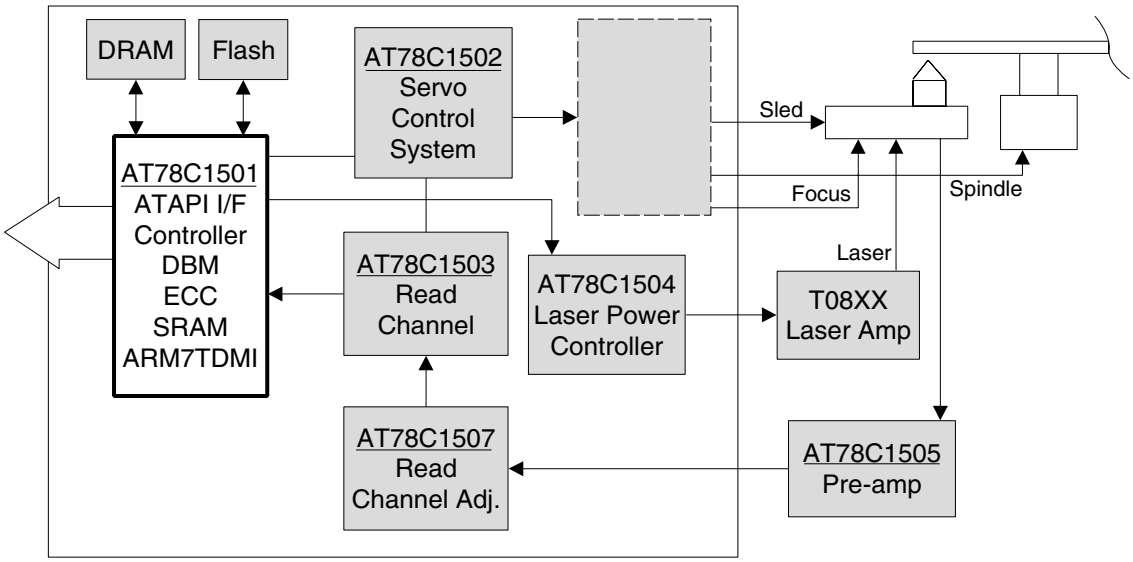
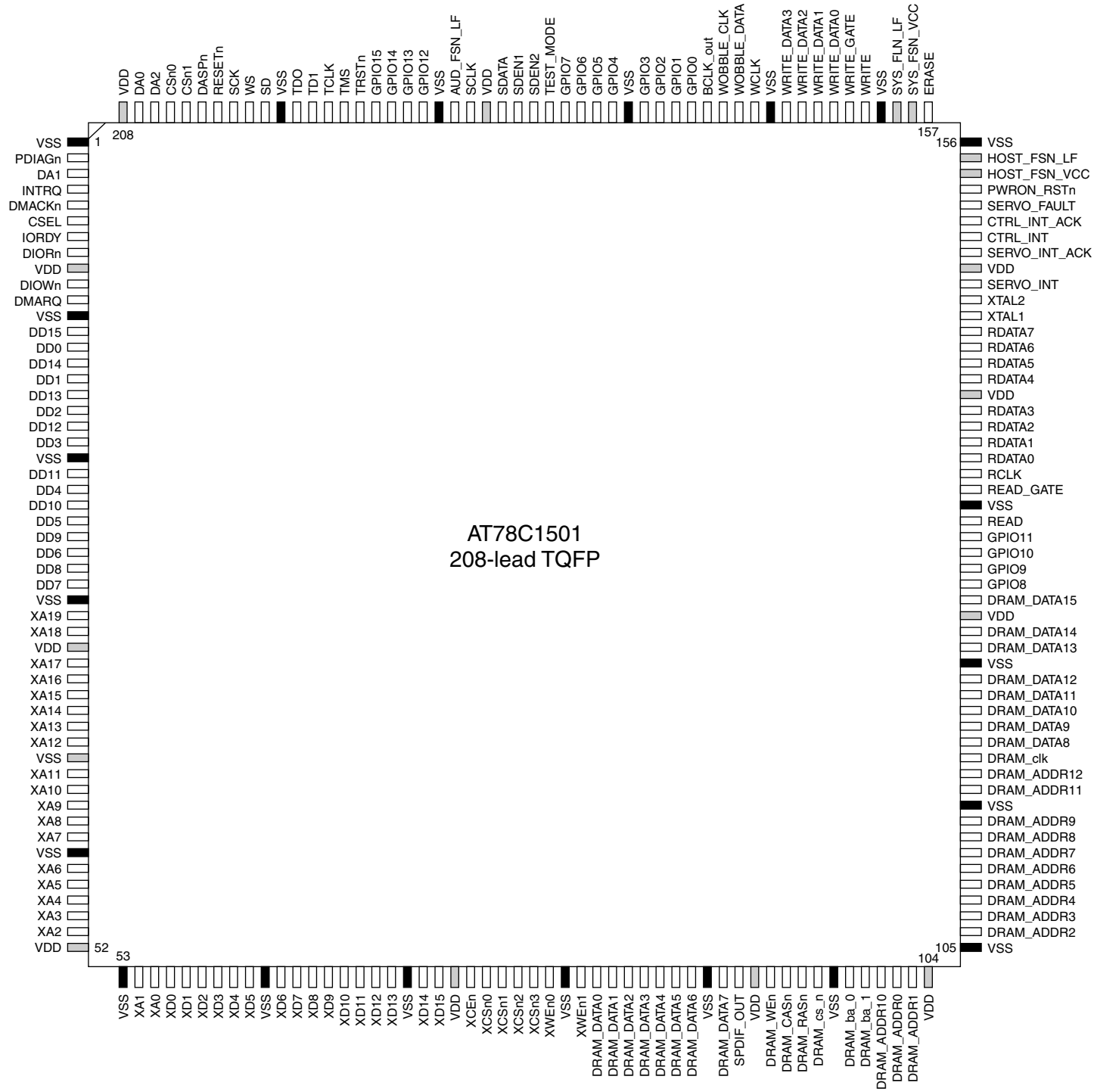


Table 1. DC Parameters

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	
I_{CC}	Operating Current			500	mA	Note 1

Note: 1. Values listed are advance information and are likely to change as production silicon is characterized.

Figure 2. Pin Assignment



Pin Definitions

General I/O Pin List

Table 1. General I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
XTAL1	145	I	Crystal Input
XTAL2	146	B	Crystal I/O
PWRON_RSTn	153	I	Power On Reset: This signal is used to initialize all logic in the controller including the ARM7 and AVR cores.
TEST_MODE	181	I	RAM Test Mode: This signal is used by the chip tester to place all embedded memory cells in BIST mode for test.
GPIO[0]	172	P	General Purpose I/O
GPIO[1]	173	P	
GPIO[2]	174	P	
GPIO[3]	175	P	
GPIO[4]	177	P	
GPIO[5]	178	P	
GPIO[6]	179	P	
GPIO[7]	180	P	
GPIO[8]	128	P	
GPIO[9]	129	P	
GPIO[10]	130	P	
GPIO[11]	131	P	
GPIO[12]	189	P	
GPIO[13]	190	P	
GPIO[14]	191	P	
GPIO[15]	192	P	
BCLK_out	171	O	Processor Clock Output: This signal is the ARM7 and AVR core clock. It can be used as the clock input to the servo chip.
SYS_FSN_VCC	158	I	System FSN VCC: This is the power supply pin for the system frequency synthesizer.
SYS_FSN_LF	159	O	System FSN Loop Filter: This signal is the loop filter pin for the system frequency synthesizer.
HOST_FSN_VCC	154	I	Host FSN VCCc: This is the power supply pin for the host frequency synthesizer.
HOST_FSN_LF	155	O	Host FSN Loop Filter: This signal is the loop filter pin for the host frequency synthesizer.
AUD_FSN_LF	187	O	Audio FSN Loop Filter: This signal is the loop filter pin for the audio frequency synthesizer.

ATAPI Interface

The AT78C1501 supports the ATAPI CD-ROM specification (IDE CD-ROM Interface) and can drive IDE signals directly. The host interface contains a 12-byte command packet FIFO and IDE registers for transferring command and status data. The host interface also contains a data FIFO for transferring data from buffer DRAM to the host. The host interface contains the following pins:

Table 2. ATAPI Interface I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
CS0-	205	I	Device Chip Select 0: Chip select signal from host to select the Command Block registers.
CS1-	204	I	Device Chip Select 1: Chip select signal from host to select the Command Block registers.
DD[15] DD[14] DD[13] DD[12] DD[11] DD[10] DD[9] DD[8] DD[7] DD[6] DD[5] DD[4] DD[3] DD[2] DD[1] DD[0]	13 15 17 19 22 24 26 28 29 27 25 23 20 18 16 14	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	Device Data Bus: Bidirectional data bus between the host and the device. The lower eight bits are used for 8-bit register transfers. Data transfers are 16 bits wide.
DASP-	203	I/O	Device Active or Slave Present: This is a time-multiplexed signal that indicates that a device is active or that Device 1 is present.
DA[2] DA[1] DA[0]	206 3 207	I	Device Address: This is the 3-bit binary coded address asserted by the host to access a register or data port in the device.
DMACK-	5	I	DMA Acknowledge: This signal shall be used by the host in response to DMARQ- to initiate DMA transfers.
DMARQ-	11	O	DMA Request: This signal, used for DMA data transfers between the host and device, shall be asserted by the device when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK, i.e., the device shall wait until the host asserts DMACK, before negating DMARQ and reasserting DMARQ, if there is more data to transfer.
INTRQ	4	O	Device Interrupt: This signal is used by the selected device to interrupt the host system. When the nIEN bit is cleared to “0” and the device is selected, INTRQ shall be enabled through a tristate buffer. When the nIEN bit is set to “1” or the device is not selected, the INTRQ signal shall be in a high impedance state.

Table 2. ATAPI Interface I/O Pin List (Continued)

Pin Name	Pin #	Pin Type	Pin Description
DIOR- HDMARDY- HSTROBE	8	I	Device I/O Read: This is the strobe signal asserted by the host to read device registers or the data port. Host DMA Ready: This signal is a flow control signal for Ultra DMA data in bursts. This signal is asserted by the host to indicate to the host that the device is ready to receive Ultra DMA data in bursts. The host may negate HDMARDY- to pause an Ultra DMA data in burst. Host Strobe: This signal is the data in strobe from the host for an Ultra DMA data out burst. Both the rising and falling edge of HSTROBE latch the data from DD[15:0] into the device. The host may stop generating DSTROBE edges to pause an Ultra DMA data out burst.
IORDY DDMARDY- DSTROBE	7	O	Device I/O Ready: This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request. Device DMA Ready: This signal is a flow control signal for Ultra DMA data out bursts. This signal is asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data out bursts. The device may negate DDMARDY- to pause an Ultra DMA data out burst. Device Strobe: This signal is the data in strobe from the device for an Ultra DMA data in burst. Both the rising and falling edge of DSTROBE latch the data from DD[15:0] into the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.
DIOW- STOP	10	I	Device I/O Write: This is the strobe signal asserted by the host to write device registers or the data port. STOP: STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.
PDIAG-	2	O	Device Passed Diagnostics: This signal shall be asserted by Device 1 to indicate to Device 0 that it has completed diagnostics.
CSEL	6	I	Cable Select: Used to select Ddevice 0 or 1.
RESET-	202	I	Device Reset: This signal, referred to as hardware reset, shall be used by the host to reset the device.

JTAG/ICE Interface

The JTAG/ICE Interface is used as the in-circuit emulator for the ARM7TDMI Processor.

Table 3. JTAG/ICE Interface I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
TMS	194	I	Test Mode Select
TDI	196	I	Test Data Input
TCK	195	I	Test Clock
TDO	197	O	Test Data Output
TRST	193	I	Test Reset

Disk Read Interface

The Disk Read Interface connects the DVD/CD Read Channel device to the controller.

Table 4. Disk Read Interface I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
RCLK	135	I	Recovered Clock: This is the recovered data rate clock from the read channel. This clock is used for the sync detection logic as well as the WCS programmable state machine.
RDATA[0] RDATA[1] RDATA[2] RDATA[3] RDATA[4] RDATA[5] RDATA[6] RDATA[7]	136 137 138 139 141 142 143 144	I I I I I I I I	Recovered Data: This is the recovered data from the disk. This is used by the sync detection and ENDEC to recover the user data on the disk.
READ	132	O	Read Mode: This signal is used to place the ALPC in read mode.
READ_GATE	134	O	Read Gate: This signal is used by the read channel to lock the PLL to the recovered data instead of the synthesizer.
WOBBLE_CLK	169	I	Wobble Clock: Recovered wobble clock from read channel. This clock is used for the ADIP, ATIP and PRE-PIT decoder state machines. This clock is also used to clock the WCS programmable state machine during write operations.
WOBBLE_DATA	168	I	Wobble Data: Recovered wobble data from read channel. This is used to decode the ADIP, ATIP and PRE-PIT data.

Disk Write Interface

The Disk Write Interface connects the DVD/CD Write device to the controller.

Table 5. Disk Write Interface I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
WCLK	166	I	Write Clock: Bit clock used to generate the NRZI data stream to the ALPC. This clock originates from the recovered wobble clock in the read channel, which is then multiplied up to the bit rate in the ALPC.
WRITE_DATA[0] WRITE_DATA[1] WRITE_DATA[2] WRITE_DATA[3]	163 164 165 166	O O O O	Write Data: This is the NRZI data stream from the controller to the ALPC.
WRITE	161	O	Write Mode**:** This signal is used to place the ALPC in write mode.
WRITE_GATE	162	O	Write Gate: This signal is used by the ALPC to allow writing to the disk.
ERASE	157	O	Erase Mode: This signal indicates that the ALPC should use the erase power level between write pulse trains. This is used for any rewritable disk format. (DVD-RW, CD-RW, DVD+RW).

DRAM Interface

The DRAM Interface connects the controller to the buffer DRAM.

Table 6. DRAM Interface I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
DRAM_RASn	96	O	Row Address Strobe
DRAM_CASn	95	O	Column Address Strobe
DRAM_ADDR[0]	102	O	DRAM Buffer Address
DRAM_ADDR[1]	103	O	
DRAM_ADDR[2]	106	O	
DRAM_ADDR[3]	107	O	
DRAM_ADDR[4]	108	O	
DRAM_ADDR[5]	109	O	
DRAM_ADDR[6]	110	O	
DRAM_ADDR[7]	111	O	
DRAM_ADDR[8]	112	O	
DRAM_ADDR[9]	113	O	
DRAM_ADDR[10]	101	O	
DRAM_ADDR[11]	115	O	
DRAM_ADDR[12]	116	O	
DRAM_DATA[0]	83	I/O	DRAM Buffer Data
DRAM_DATA[1]	84	I/O	
DRAM_DATA[2]	85	I/O	
DRAM_DATA[3]	86	I/O	
DRAM_DATA[4]	87	I/O	
DRAM_DATA[5]	88	I/O	
DRAM_DATA[6]	89	I/O	
DRAM_DATA[7]	91	I/O	
DRAM_DATA[8]	118	I/O	
DRAM_DATA[9]	119	I/O	
DRAM_DATA[10]	120	I/O	
DRAM_DATA[11]	121	I/O	
DRAM_DATA[12]	122	I/O	
DRAM_DATA[13]	124	I/O	
DRAM_DATA[14]	125	I/O	
DRAM_DATA[15]	127	I/O	
DRAM_WEn	94	O	DRAM Write Strobe
DRAM_cs_n	97	O	DRAM Chip Select
DRAM_ba[0]	99	O	DRAM Bank Select
DRAM_ba[1]	100	O	
DRAM_clk	117	O	DRAM Clock

External Memory Interface

The External Memory Interface connects external program memory to the controller. The DVD RAM Servo device is also connected to this bus.

Table 7. External Memory Interface I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
XA[0]	55	O	External Address Bus: Address bus for external memory banks
XA[1]	54	O	
XA[2]	51	O	
XA[3]	50	O	
XA[4]	49	O	
XA[5]	48	O	
XA[6]	47	O	
XA[7]	45	O	
XA[8]	44	O	
XA[9]	43	O	
XA[10]	42	O	
XA[11]	41	O	
XA[12]	39	O	
XA[13]	38	O	
XA[14]	37	O	
XA[15]	36	O	
XA[16]	35	O	
XA[17]	34	O	
XA[18]	32	O	
XA[19]	31	O	
XD[0]	56	I/O	External Data Bus
XD[1]	57	I/O	
XD[2]	58	I/O	
XD[3]	59	I/O	
XD[4]	60	I/O	
XD[5]	61	I/O	
XD[6]	63	I/O	
XD[7]	64	I/O	
XD[8]	65	I/O	
XD[9]	66	I/O	
XD[10]	67	I/O	
XD[11]	68	I/O	
XD[12]	69	I/O	
XD[13]	70	I/O	
XD[14]	72	I/O	
XD[15]	73	I/O	
XCSn[0]	76	O	External Chip Select
XCSn[1]	77	O	
XCSn[2]	78	O	
XCSn[3]	79	O	
XWEn[0]	80	O	External Write Enable
XWEn[1]	82	O	
XOEn	75	O	External Output Enable

Servo Interface

The Servo Interface connects the servo device to the controller.

Table 8. Servo Interface I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
SERVO_INT	147	I	Servo Interrupt Input: Interrupt signal from the servo to the controller
SERVO_INT_ACK	149	O	Servo Interrupt Acknowledge: Interrupt acknowledge from the controller to the servo
CTRL_INT	150	O	Controller Interrupt Output: Interrupt signal from the controller to the servo
CTRL_INT_ACK	151	I	Controller Interrupt Acknowledge: Interrupt acknowledge from the servo to the controller
SERVO_FAULT	152	I	Servo Fault: Indicates that some kind of fault has occurred in the servo or read channel. This is used to gate off any disk write functions.

Serial Interface

The Serial Interface connects all slave devices to the controller.

Table 9. Serial Interface I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
SCLK	186	O	Serial Clock
SDATA	184	I/O	Serial Data
SDEN1	183	O	Serial Enable 1
SDEN2	182	O	Serial Enable 2

I2S Audio Interface

The I2S Audio Interface is a serial interface for external audio devices.

Table 10. I2S Audio Interface I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
SCK	201	O	Serial Clock
WS	200	O	Word Select
SD	100	O	Serial Data

Sony® Philips® Digital Audio Interface

The Sony Philips Digital Audio Interface is a standard digital interface for external audio devices.

Table 11. Sony Philips Digital Audio Interface I/O Pin List

Pin Name	Pin #	Pin Type	Pin Description
SPDIF_OUT	92	O	Sony Philips Digital Interface

Figure 3. Functional Pinout

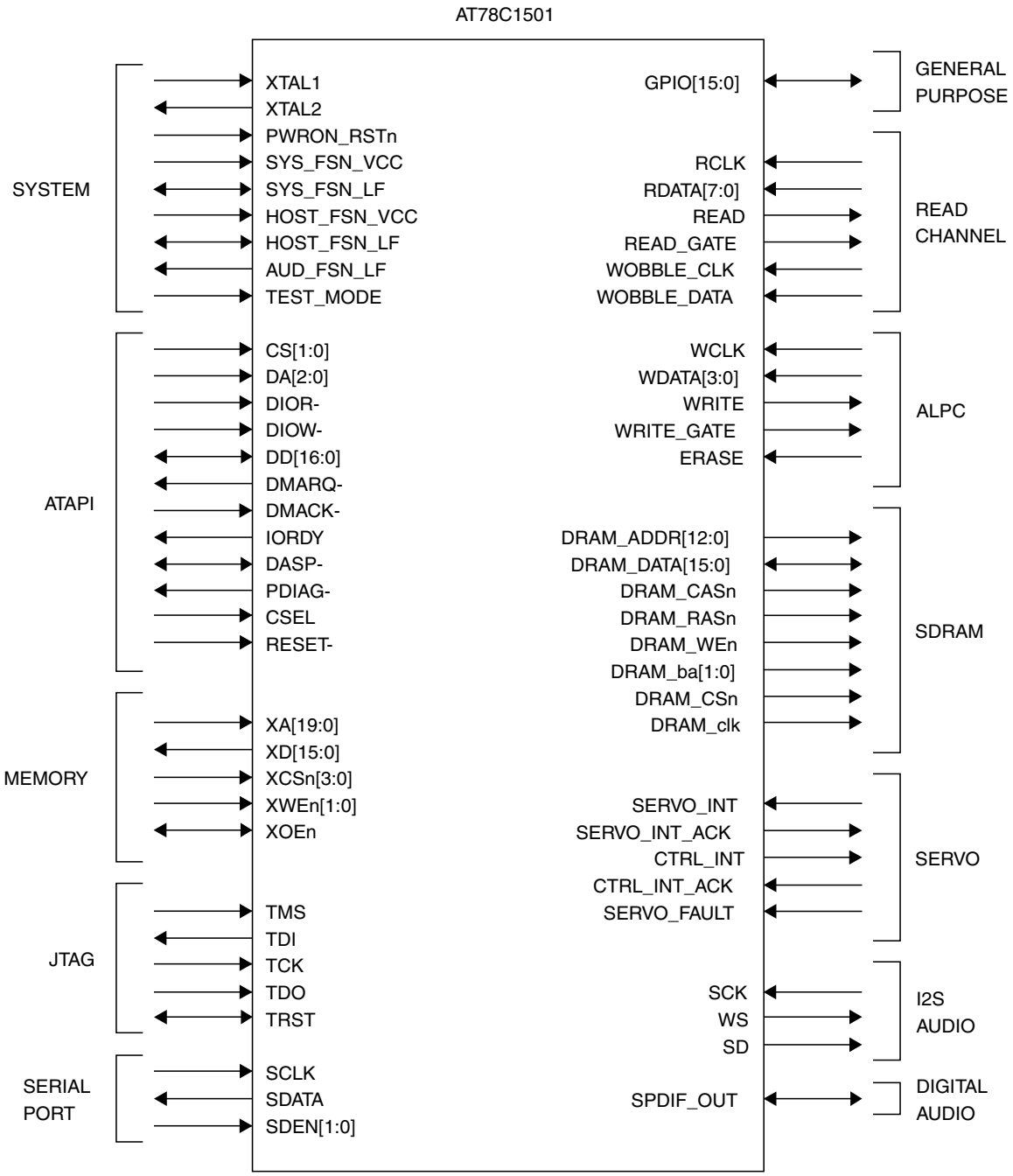
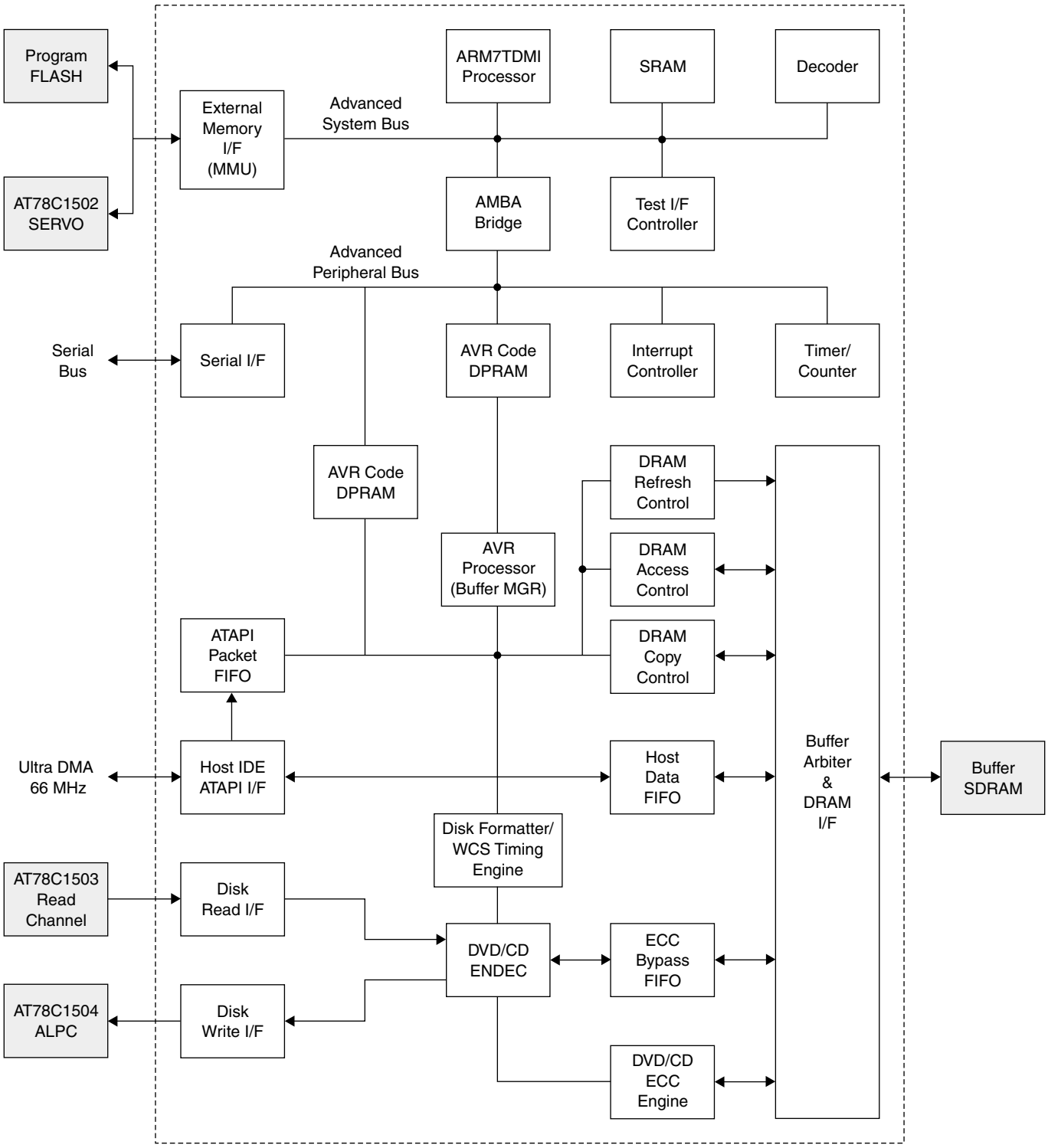


Figure 4. AT78C1501 Block Diagram



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