AT91EB40
Evaluation Board

User Guide

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Section 1

Overview

1.1 Scope

The AT91EB40 Evaluation Board enables real-time code development and evaluation. It supports the AT91x40 series with its various memory options.

This guide focuses on the AT91 Evaluation Board as an evaluation and demonstration platform:

1. Section 1 provides an overview.
2. Section 2 details the setup of the development board.
3. Section 3 describes the on-board software.
4. Section 4 gives the circuit description.

Following are two appendixes covering configuration links and memory data, and schematics including pin connectors.

1.2 Deliverables

The evaluation board is supplied with a DB9 plug to DB9 socket straight through serial cable to connect the target evaluation board to a PC. There is also a bare power lead with a 2.1 mm jack on one end for connection to a bench power supply.

To use the evaluation board the user needs to provide a host computer and a debugging system.

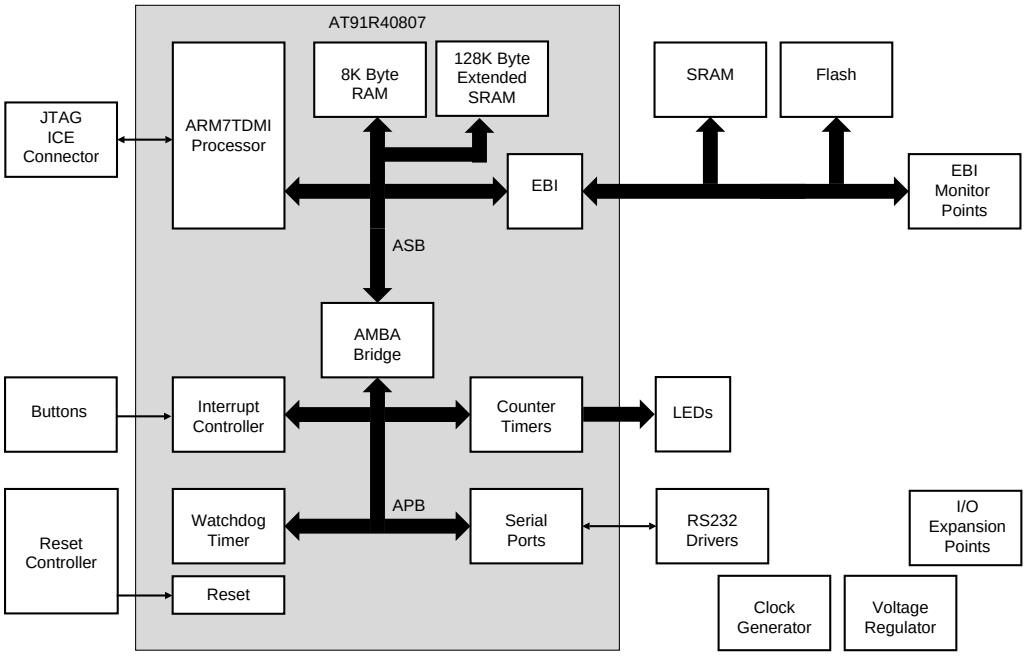
1.3 The AT91EB40 Evaluation Board

The board consists of an AT91R40807 together with several peripherals:

- Two serial ports
- Reset button
- Three applicative buttons (FIQ, TIOB0, IRQ0)
- Three LEDs (TIOA0, TIOA1, TIOB0)
- 512K bytes 16-bit SRAM (upgradable to 2048K bytes)
- 128K bytes 16-bit Flash (of which 64K bytes is available for user software)
- 20-pin JTAG interface connector

If required, user-defined peripherals can also be added to the board. See Section 5, “Appendix A – Configuration Links and SRAM Bank 1” on page 5-1 for details.

Figure 1-1. AT91EB40 Block Diagram



Section 2

Setting Up the AT91EB40 Evaluation Board

2.1 Electrostatic Warning

The AT91EB40 Evaluation Board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

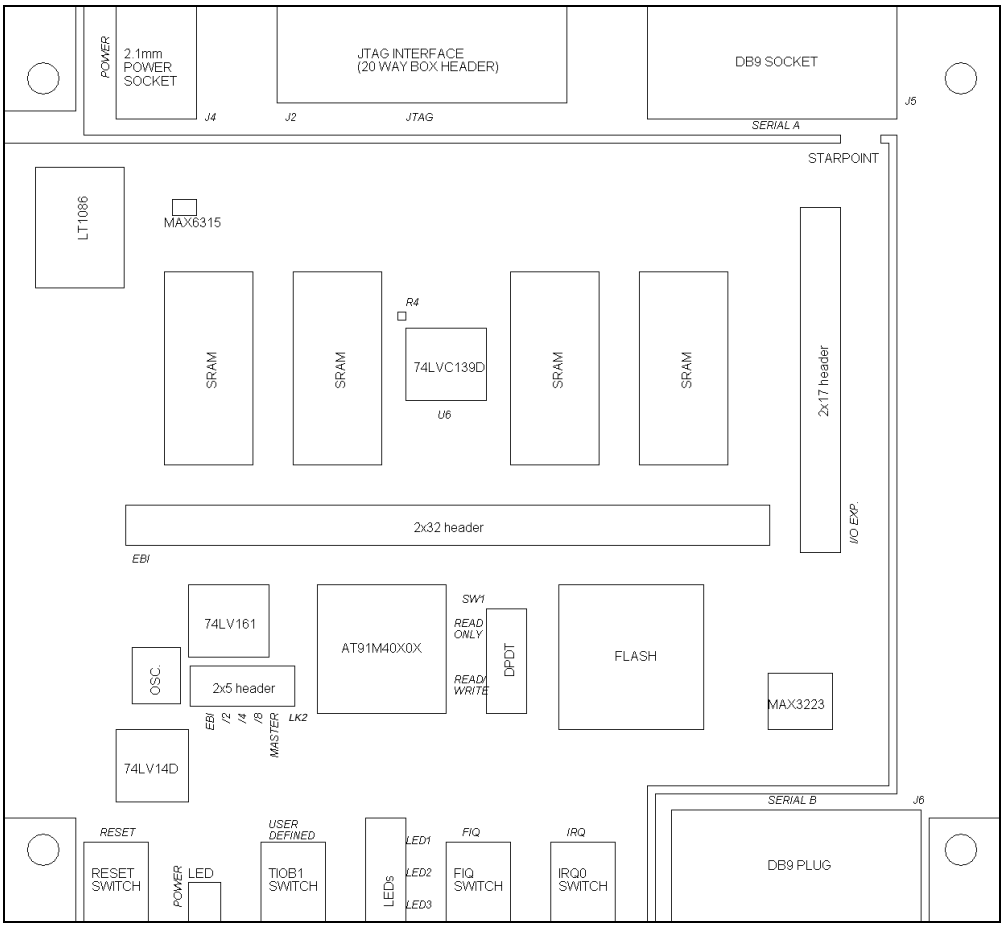
Requirements in order to set up the AT91EB40 Evaluation Board are:

- the AT91EB40 Evaluation Board itself
- DC power supply capable of supplying 7.5V to 9V @ 500 mA (not supplied)

2.3 Layout

Figure 2-1 shows the layout of the AT91EB40 Evaluation Board.

Figure 2-1. Layout of the AT91EB40 Evaluation Board



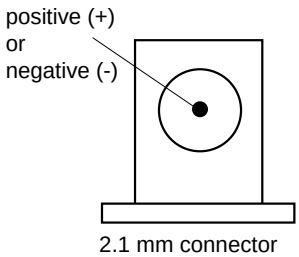
2.4 Jumper Settings

LK2 is used to select the clock frequency and by default, is set to 32,768 MHz. For more information about this jumper and the various surface mount links, see Section 5, “Appendix A – Configuration Links and SRAM Bank 1” on page 5-1.

2.5 Powering Up the Board

DC power is supplied to the board via the 2.1 mm socket (J4) shown below in Figure 2-2. The polarity of the power supply is not critical. The minimum voltage required is 7V.

Figure 2-2. 2.1 mm Socket



The board has a voltage regulator providing +3.3V. The regulator allows the input voltage to be from 7V to 9V. When you switch the power on, the red LED marked “POWER” will light up. If it does not, switch off and check the power supply connections.

2.6 Measuring Current Consumption on the AT91R40807

The board is designed to generate the whole power supply of the AT91 device, and only the AT91 device, through the wirelink WL2. This feature enables measurements to be made of the current consumption of the AT91 device.

2.7 Testing the AT91EB40 Evaluation Board

Connect the straight cable between Serial A and Serial B. With the FIQ button depressed, power-up the board, or generate a reset. The three LEDs (green, amber, red) light up. Release the FIQ. The three LEDs go off and then blink once.

Press the TIOB1 button. The red LED lights up. Release the TIOB1. The red LED goes off. If the board has 512K bytes SRAM, the green LED blinks twice. If the board has 2048K bytes SRAM, the green LED blinks four times.

Press the FIQ button. The amber LED lights up. Release the FIQ. The amber LED goes off and the green LED blinks four times. If the green LED blinks twice and then the red LED blinks twice, the straight cable is not connected.

Press the IRQ0 button. The amber and red LEDs light up. Release the IRQ0. The LEDs go off and the green LED blinks twice.

Section 3

The On-board Software

3.1 Flash Memory Organization

The Flash memory is an AT29LV1024 (64K x 16). It is arbitrarily located at the address 0x01000000 by the boot software. It has been split in two different spaces:

- 0x01000000 up to 0x0100FFFF = boot and Angel software
- 0x01010000 up to 0x0101FFFF = application software

The switch SW1 allows the signal “SW_A16” to be set (see Figure 6-3, “External Bus Interface”), which drives the bit A15 of the Flash part:

- “LOWER MEM” uses the bit A16 of the AT91R40807. The entire Flash can be reached by the AT91R40807, and the boot software at location 0x01000000 is executed at the reset.
- “UPPER MEM” uses the V_{CC}. Only the upper 64K can be reached, at the location defined by the application software executed at the reset.

It is important to note that the mapping defined by the boot software is the following:

- Flash at address 0x01000000
- SRAM at address 0x02000000

Nevertheless, when SW1 is set with “UPPER_MEM”, these addresses are under user application responsibility.

At delivery, the Flash is programmed with the following software:

- Boot from 0x01000000 up to 0x01001FFF
- Angel from 0x01002000 up to 0x0100FFFF
- Demo application from 0x01010000 up to 0101FFFF

3.1.1 Flash Write Access

The upper 64K of the Flash can be overwritten whatever the position of the switch SW1. This can also be done by using Angel rather than the EmbeddedICE.

The lower 64K are write-protected, whatever the position of the switch SW1. This is to prevent the boot and Angel software stored in the lower 64K bytes from being erased.

Nevertheless, it is always possible to make this space unprotected by setting a jumper or a link on the footprint J7.

Note: If the lower 64K are not protected, the user must be especially careful. Even though one of the features of the boot is the ability to restore Angel, it cannot be saved itself. Once it is overwritten, the only way to restore the Flash is to use an EmbeddedICE.

3.1.2 Boot Software

The boot software is started at the reset if SW1 is switched to “LOWER MEM”.

It first initializes the EBI, then executes the REMAP procedure, and then checks the state of the buttons:

- If the button FIQ is pressed, all the LEDs are lit and the Functional Test Software (FTS) is activated.
- If the button TIOB1 is pressed, the red LED is lit and the SRAM downloader is activated.
- If neither TIOB1 nor FIQ are pressed, the amber LED is lit and Angel is activated.

3.1.3 Functional Test Software (FTS)

The FTS is a part of the boot software that allows testing of the AT91EB40. It is started by the boot if the FIQ button is pressed at reset. At start of the FTS, the LEDs 1, 2 and 3 light up. The user must then release the FIQ button. The LEDs switch off and then blink once.

The FTS then waits for one of the following user actions on the buttons:

- If the TIOB1 button is pressed, the memory size is checked and the green LED blinks:
  - 1 = 256K bytes
  - 2 = 512K bytes
  - 3 = 1024K bytes
  - 4 = 2048K bytes
- If the FIQ button is pressed, the USART are tested:
  - Transfer one character from USART 0 to USART 0 (loopback mode)
  - Transfer one character from USART 1 to USART 1 (loopback mode)
  - Transfer one character from USART 0 to USART 1 (normal mode)
  - Transfer one character from USART 1 to USART 0 (normal mode)

  For each case, the green or the red LED blinks once following the positive or negative result of the test. Note that the second and third tests can succeed only if the straight serial cable (provided) is connected between Serial A and Serial B.
- If the IRQ0 button is pressed, the buses of the SRAM are tested:
  - Address bus
  - Data bus

  In each case, the green or the red LED blinks once following the positive or negative result of the test.

3.1.4 SRAM Downloader

The SRAM downloader is a part of the boot software and allows an application in the SRAM to be loaded at the address 0x02000000 when activated. It is started by the boot if the button TIOB1 is pressed at reset.

The procedure is as follows:

1. Connect the AT91EB40 to the host PC using either the straight serial cable (provided) on Serial A, or a crossed serial cable (not provided) on Serial B.
2. Set the clock frequency (LK2) to the desired frequency. Note that this directly determines the baud rate for the download (See Table 3-1).
3. Generate a power-on or a reset with the TIOB1 pressed down. Wait for the red LED to light up and then release the TIOB1 button.
4. Start the BINCOM utility available in the AT91 library on the host computer: Select the port and the baud rate for communications, then open the file to download and send it. Wait for the end of the transfer.
5. Press the button IRQ0 to terminate the download. The control is switched to the address 0x02000000.

Table 3-1 shows the relationship between the clock rate on the board and the serial baud rate.

Table 3-1. Clock Rate vs. Serial Baud Rate

Frequency	Serial A	Serial B
16 MHz	57600	19200
32 MHz (master)	115200	38400

Note that if the debugger is started through ICE while the SRAM downloader is on, then both serial channels are enabled.

3.1.5 Angel Monitor

The Angel monitor is located in the Flash from 0x01002000 up to 0x0100FFFF. It is started by the boot if neither TIOB1 nor FIQ are pressed at reset.

When Angel starts, it recopies itself into the SRAM in order to run faster. The SRAM used by Angel is from 0x02020000 to 0x02040000, i.e., the highest half of the SRAM.

The Angel on the AT91EB40 can be upgraded regardless of the version programmed on it.

Note that if the debugger is started through ICE while the Angel monitor is on, the Advanced Interrupt Controller (AIC) and the USART channel are enabled.

Section 4

Circuit Description

4.1 AT91EB40 Top Level

The top level schematic in Section 6, “Appendix B - Schematics” shows the blocks in the system (see Figure 6-1). Each block is described in the appropriate section below.

4.2 AT91R40807 Processor

This schematic shows the AT91R40807 (see Figure 6-7). The footprint is for a 100-pin TQFP package.

Wirelink (WL2) can be removed by the user to allow measurement of the current demand by the microcontroller.

4.3 I/O Expansion

The I/O expansion connector makes available to the user the general-purpose I/O (GPIO) lines, VDD and ground. Surface mount links 5, 6, 7, 8 and 9 are used to select between the I/O lines being used by the evaluation board or by the user via the I/O expansion connector. The connector is not fitted at the factory; however, the user can fit any 17 x 2 connector on a 0.1" (2.54 mm) pitch.

4.4 External Bus Interface

This schematic shows one AT29LV1024-15JC with a 128 KB 16-bit Flash and four 512K x 8 SRAM devices. See Figure 6-3.

Note: The AT91EB40 is fitted with four 128K x 8 SRAM devices.

The schematic also shows the bus expansion connector which, like the I/O expansion connector, is not fitted at the factory. The user can fit any 32 x 2 connector on a 0.1" (2.54 mm) pitch to gain access to the data, address, chip select, read/write, oscillator output and wait state pins. Pin 8 on this connector can be used to apply an external clock frequency to the board, assuming the clock select jumper is fitted accordingly (see Section 5). VDD and ground are also available on the connector.

Switch 1 shown on this schematic is used to select either read-only access of all locations in Flash or allow read/write access to the top 64K bytes. This is to prevent the Angel debug program, which is stored in the lower 64K bytes, from being erased.

4.5 Power, Crystal Oscillator and Clock Distribution

The system clock is derived from a single 32.768 MHz crystal oscillator. This is divided by a 4-bit binary counter to give alternate clock frequencies of 32.768 MHz divided by 2, 4 or 8. The system clock frequency is selected by fitting a jumper link in one position of the link field (LK2) and details of this can be found in Section 5. One position in LK2 selects an external oscillator to be applied via the expansion bus interface.

Note that the 4-bit binary counter is not fitted at the factory; this function is optional.

The voltage regulator provides 3.3V to the board and will light the red POWER LED when operating. Power can be applied via the 2.1 mm connector to the regulator in either polarity because of the diode rectifying circuit. The regulators can tolerate supply transients to 30V although they will shut down without damage if they overheat.

4.6 JTAG Interface, Reset, Interrupts and LEDs

An ARM®-standard 20-pin box header (J2) is provided to enable connection of an EmbeddedICE interface (using an EmbeddedICE to Multi-ICE adapter) or Multi-ICE interface to the JTAG inputs on the AT91. This allows code to be developed on the board without the use of system resources such as memory and serial ports.

The IRQ, FIQ and TIOB0 switches are debounced and buffered. A supervisory circuit has been included in the design to detect and consequently reset the board when the 3.3V supply voltage drops below 3.08V. It also provides a debounced reset signal.

The schematic also shows LEDs 1, 2 and 3, which are for general purpose use and are connected to timer (or I/O) pins TIOA0/P1, TIOA1/P4 and TIOB0/P2.

4.7 Serial Interface

Two 9-way D-type connectors (J5/6) are provided for serial port connection. Serial portA (J5) is used primarily for host PC communication and is a DB9 female connector. TXD and RXD are swapped so that a straight-through cable can be used. CTS and RTS are connected together, as are DCD, DSR and DTR.

Serial port B (J6) is a DB9 male connector with TXD and RXD obeying the standard RS-232 pinout. Apart from TXD, RXD and ground, the other pins are not connected.

RS-232 level conversion is provided by a MAX3223 device (U13) and associated bulk storage capacitors.

4.8 Layout Drawing

The layout diagram schematic shows an approximate floorplan for the board. This has been designed to give the lowest board area, while still providing access to all test points, links and switches on the board. See Figure 6-2.

The size is approximately 4.5 inches square with four mounting holes, one at each corner, into which feet are attached. The board has two signal layers and two power planes.

Section 5

Appendix A – Configuration Links and SRAM Bank 1

5.1 Jumpers (LK2)

The LK2 jumper is used to select the clock frequency. The frequency options are 32,768 MHz, 32.768 MHz divided by 2, 4 or 8, or an external clock applied via the expansion bus interface.

LK2

1	3	5	7	9
2	4	6	8	10
EBI	MAST	/2	/4	/8

Note that before using this function, the user must fit the 4-bit binary counter used to divide the 32.768 MHz clock.

5.2 Surface Mount Links (LK1, LK3 - 9)

By adding the I/O expansion and the bus expansion connectors, the user can add his own peripherals to the evaluation board. These peripherals may require more I/O lines than available while the board is in its default state. Extra I/O lines can be made available by disabling some of the on-board peripherals. This is done using the surface mount links detailed below. If these links need to be changed, a fine-tipped soldering iron is required. All links are 0R 0805 resistors unless stated otherwise.

LK1 should be left unaltered unless a memory upgrade is required. If this is the case, see the paragraph “Increasing Memory Size” on page 5-2.

LK1	Function
A-C	A18 is used as the chip select for SRAM Bank 1. Should be in this position for 128K x 8 SRAMs
B-C	A20 is used as the chip select for SRAM Bank 1. Should be in this position for 512K x 8 SRAMs

LK3	Function
A-C	Alternate boot mode NOT selected
B-C	Alternate boot mode selected

Note: Use a 10K resistor.

LK4	Function
A-C	RXD lines are set tri-state on the RS-232 transceiver so that the receiver signals to AT91 can be used for external I/O via the I/O connector.
B-C	Receive pins on AT91 used by on-board serial ports

Note: Use a 10K resistor.

LK5	Function
A-C	TXD0 connects to I/O connector
B-C	TXD0 connects to RS-232 Transceiver

LK6	Function
A-C	AT91 IRQ0 pin connects to I/O connector
B-C	AT91 IRQ0 input is from IRQ switch

LK7	Function
A-C	AT91 FIQ pin connects to I/O connector
B-C	AT91 FIQ input is from FIQ switch

LK8	Function
A-C	TXD1 connects to I/O connector
B-C	TXD1 connects to RS-232 Transceiver

LK9	Function
A-C	TIOB1 connects to I/O connector
B-C	AT91 TIOB1 input is from TIOB1 switch

5.3 Increasing Memory Size

The AT91EB40 is supplied with four 128K x 8 byte SRAM memories. If, however, the user needs more than 512K bytes of memory, the devices can be replaced with four 512K x 8 3.3V 15/20 ns SRAMs giving, in total, 2048K bytes. If this is done, LK1 must be moved to position B-C.

The user must either have 128K x 8 SRAMs or 512K x 8 SRAMs fitted in Bank 0 and, if desired, Bank 1. The two SRAM sizes cannot be mixed.

Section 6

Appendix B - Schematics

6.1 Schematics

The following schematics are appended:

- Figure 6-1. AT91EB40 Evaluation Board
- Figure 6-2. PCB Layout
- Figure 6-3. External Bus Interface
- Figure 6-4. JTAG Interface, Reset, Interrupts and LEDs
- Figure 6-5. I/O Expansion
- Figure 6-6. Power, Crystal Oscillator and Clock Distribution
- Figure 6-7. AT91R40807 in TQFP Package
- Figure 6-8. Serial Interface

The pin connectors are indicated on the schematics:

- J1 = EBI Expansion – External Bus Interface (Figure 6-3)
- J2 = JTAG Interface – JTAG Interface, Reset, Interrupts and LEDs (Figure 6-4)
- J3 = I/O Expansion – I/O Expansion (Figure 6-5)
- J5 = Serial A – Serial Interface (Figure 6-8)
- J6 = Serial B – Serial Interface (Figure 6-8)

Figure 6-1. AT91EB40 Evaluation Board

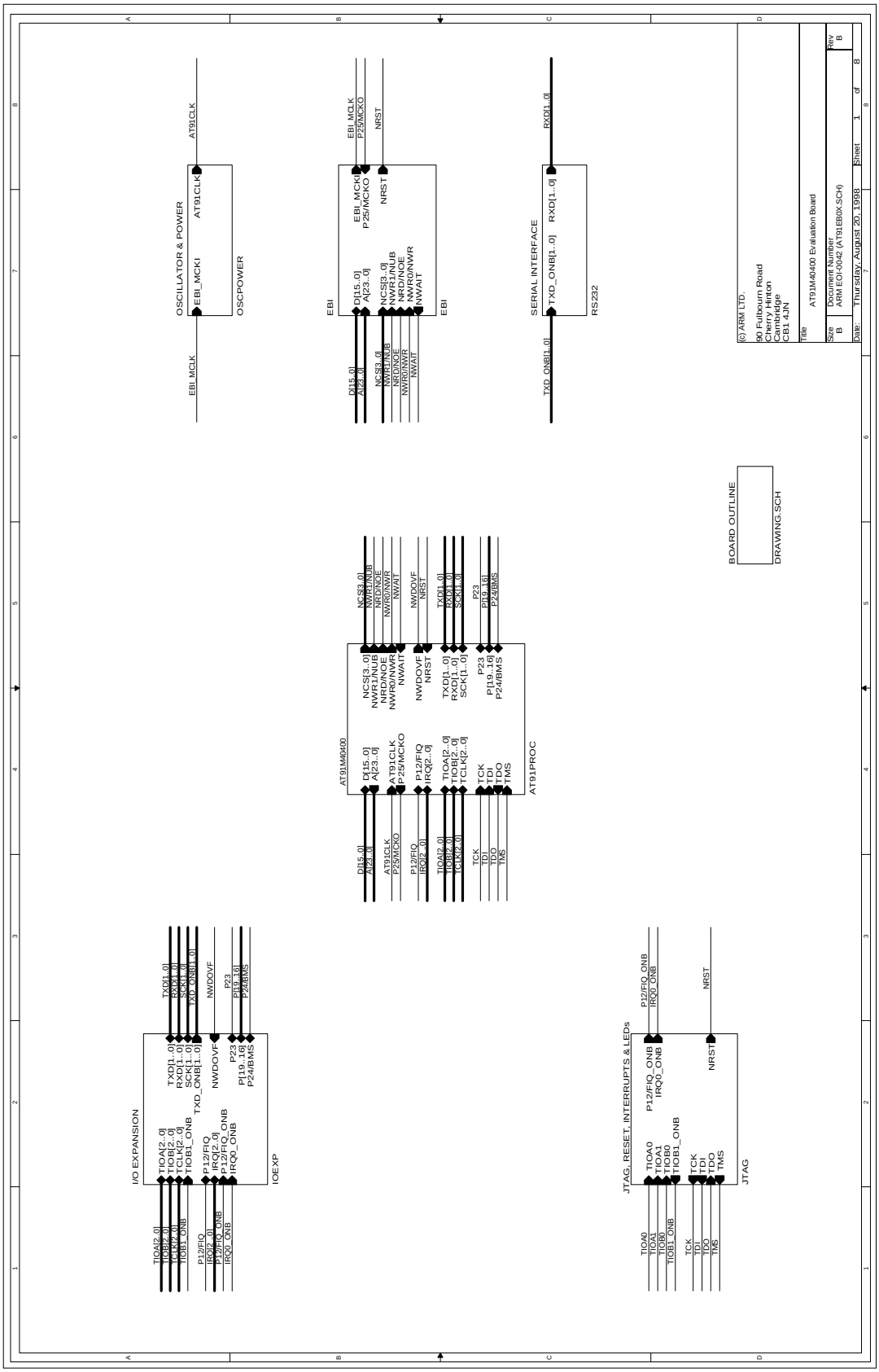


Figure 6-2. PCB Layout

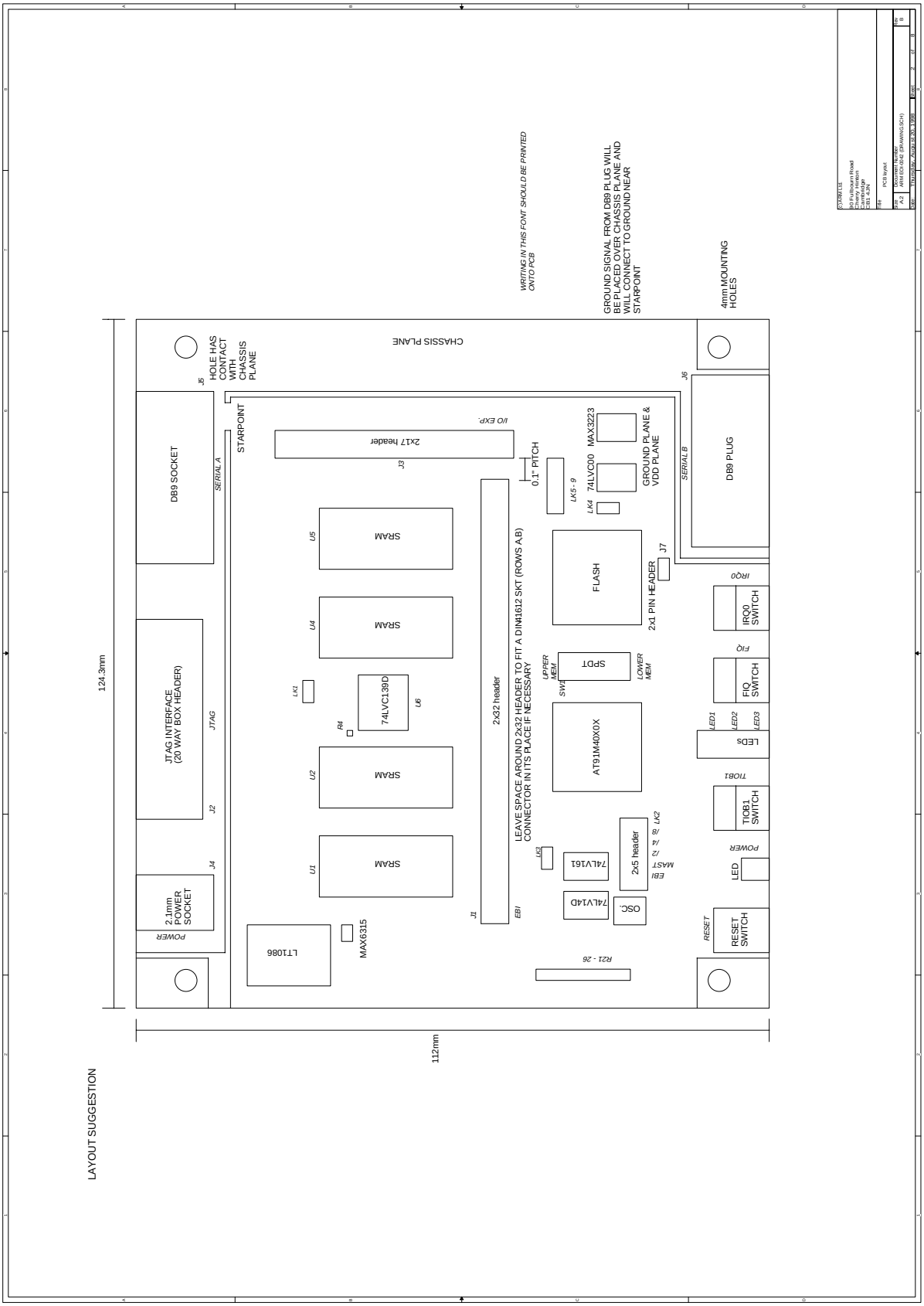


Figure 6-3. External Bus Interface

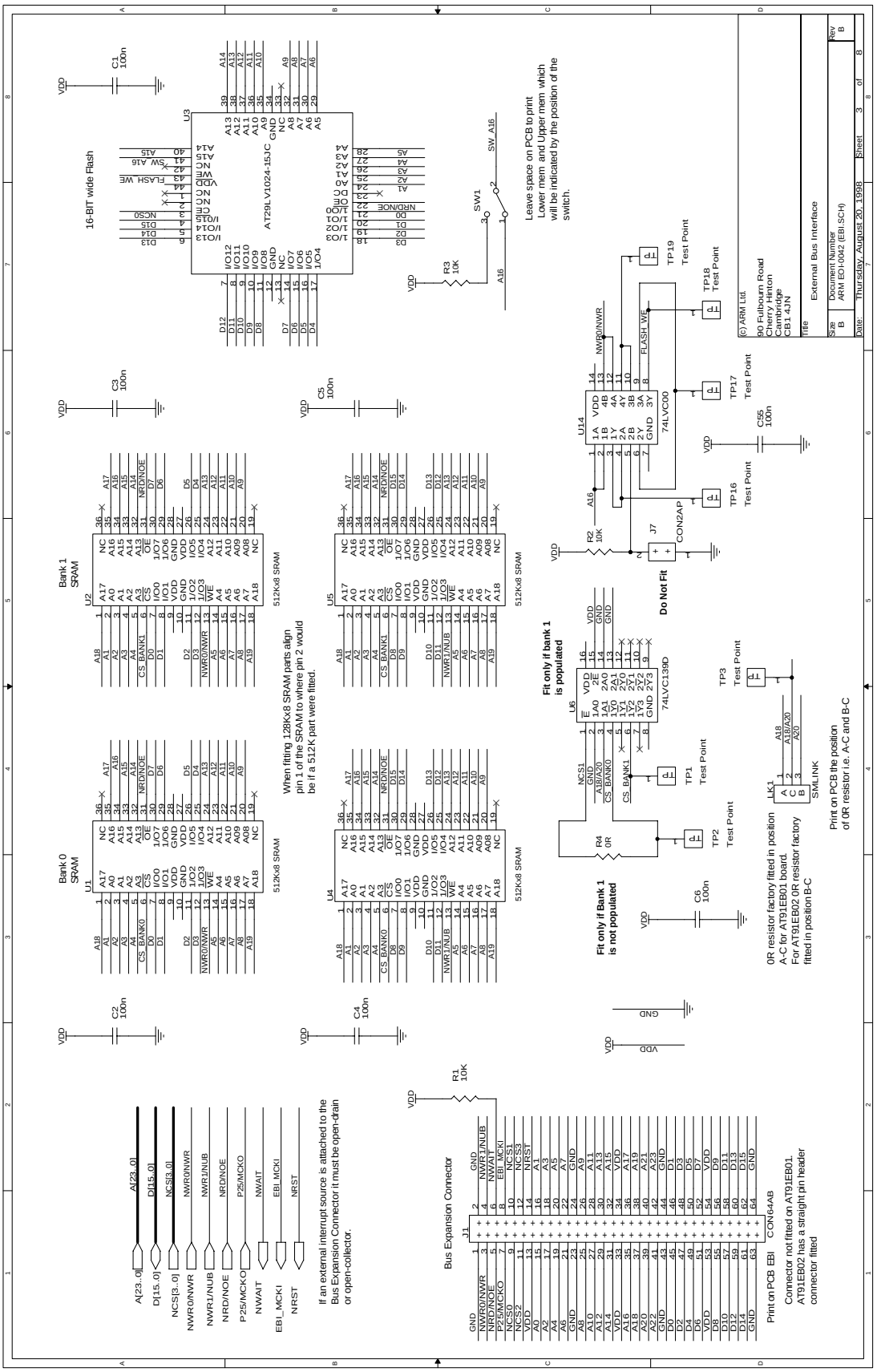


Figure 6-4. JTAG Interface, Reset, Interrupts and LEDs

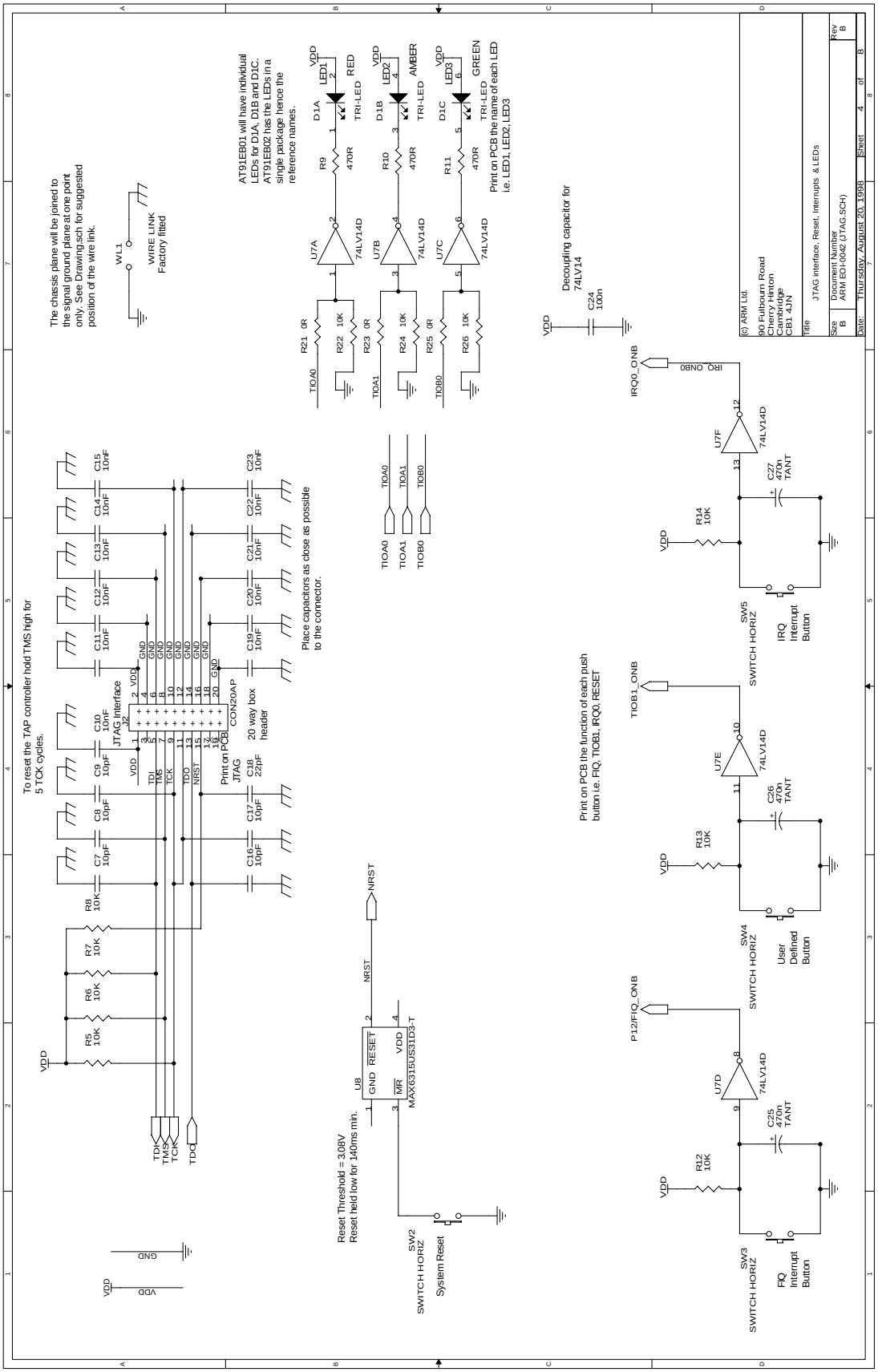


Figure 6-5. I/O Expansion

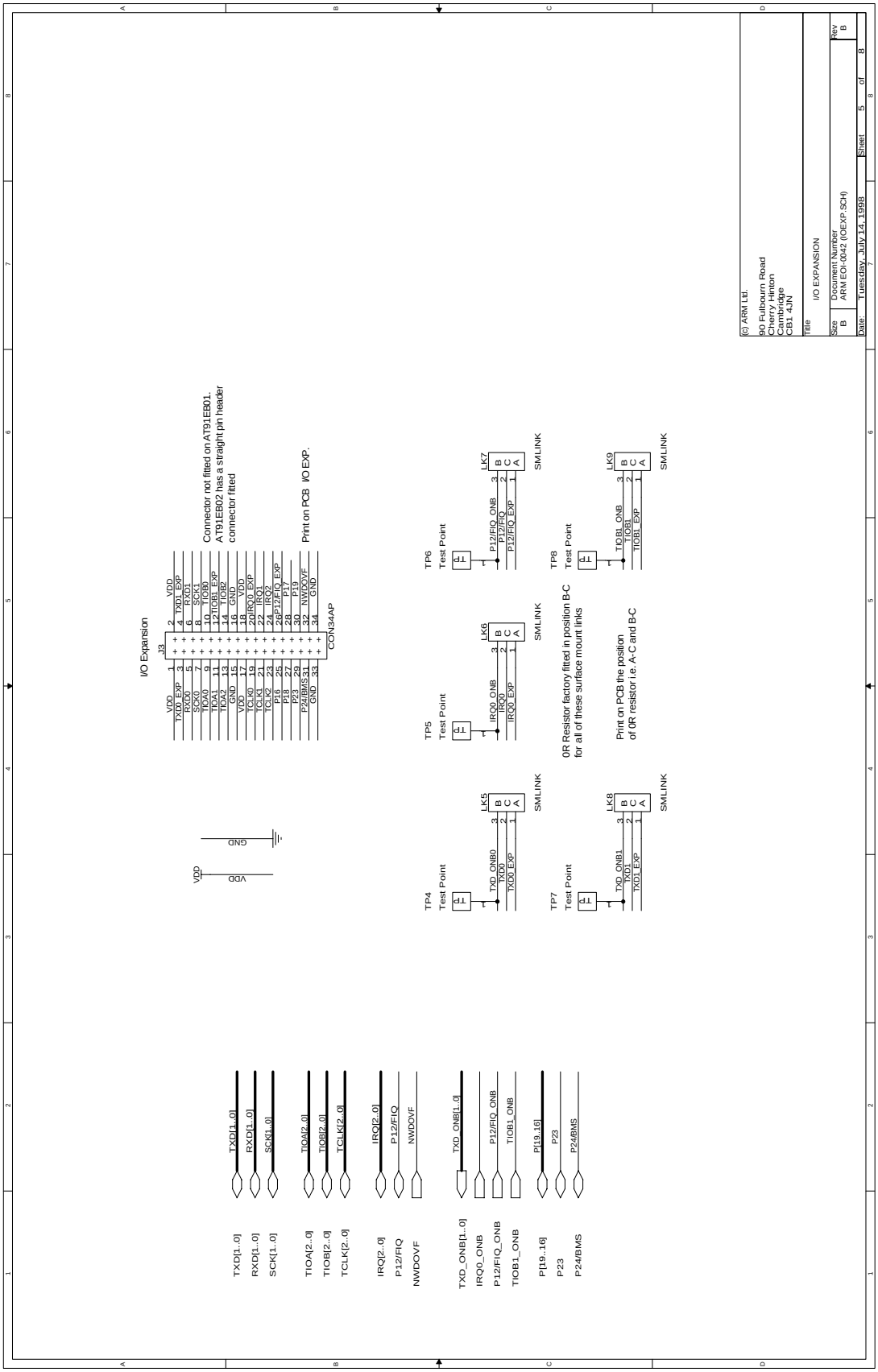


Figure 6-6. Power, Crystal Oscillator and Clock Distribution

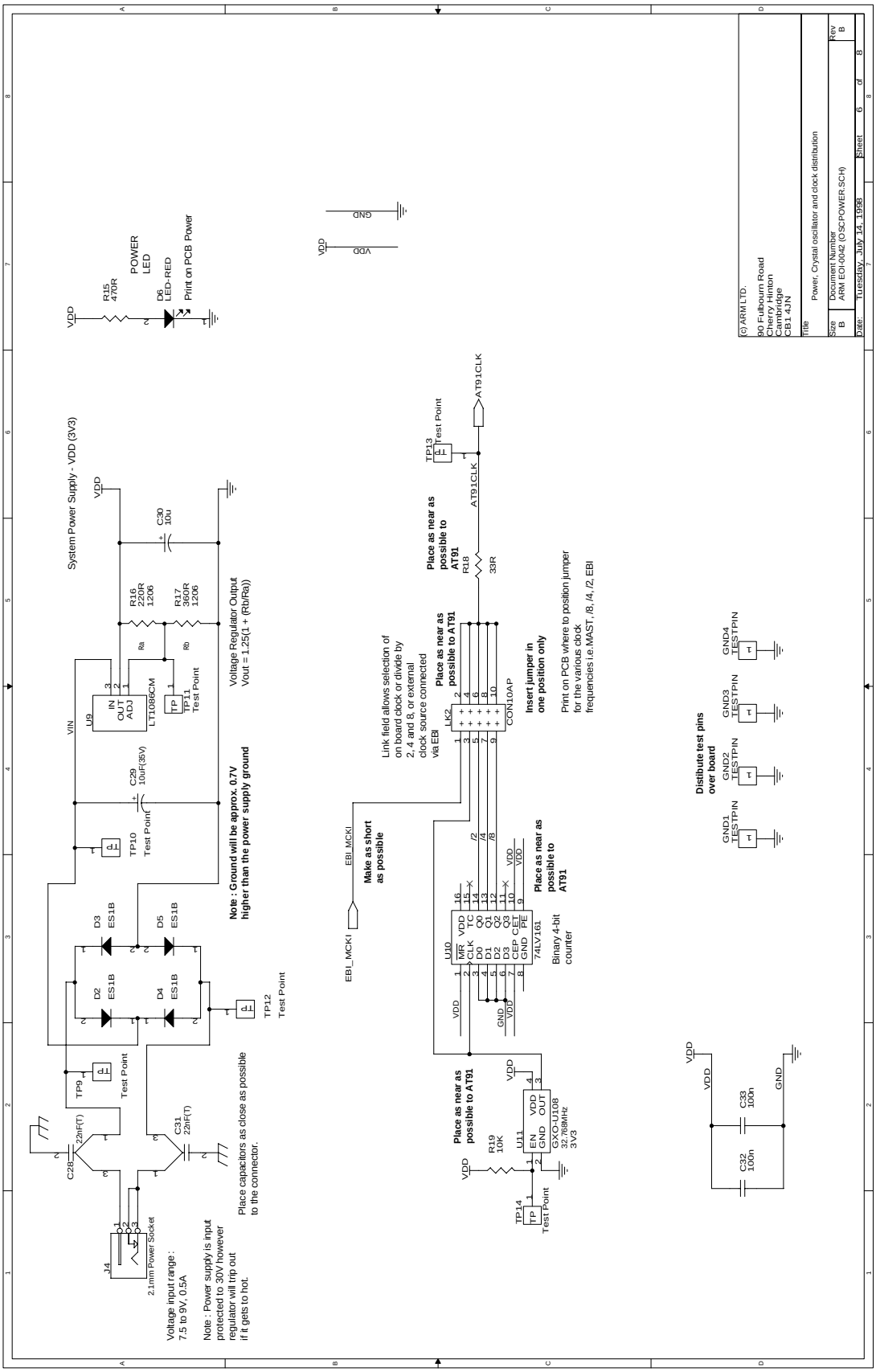


Figure 6-7. AT91R40807 in TQFP Package

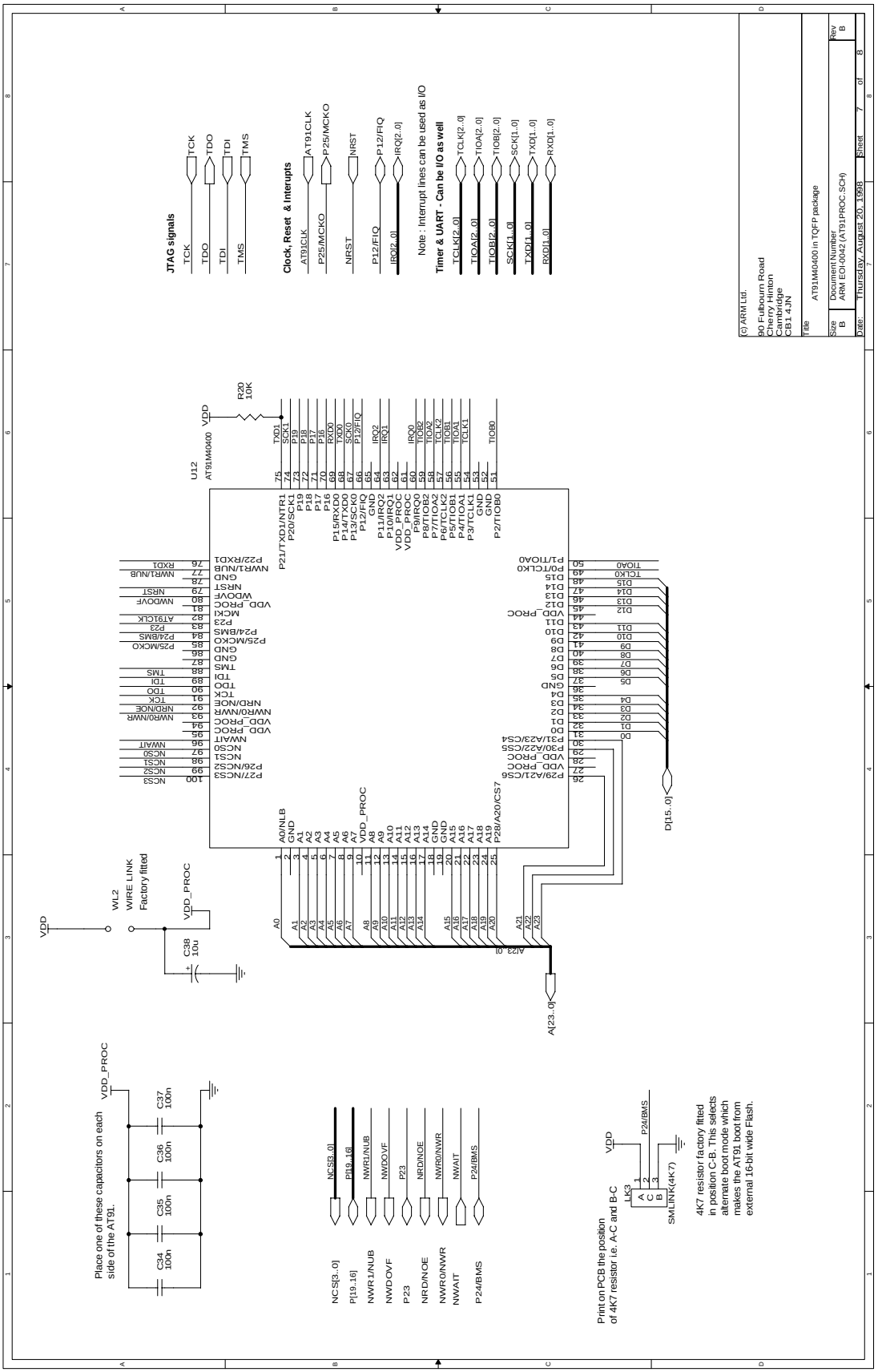
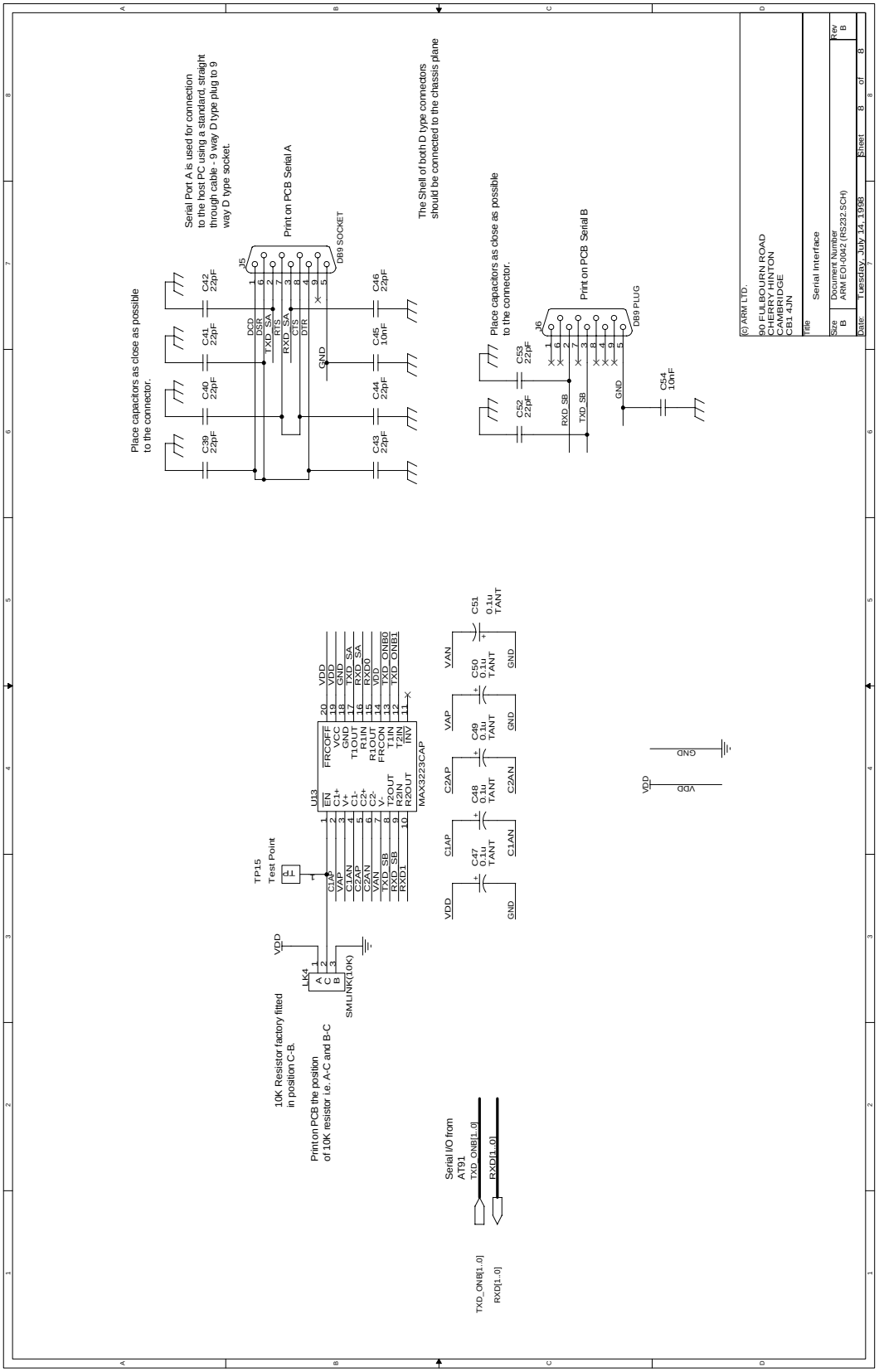


Figure 6-8. Serial Interface



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